Microelectronics Presentation Days

Europeanisation of Mil-Std-1553B Data Bus Products 1553 Remote Terminal IP core

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Context

Context

- The EUR1553 IP has been developed in the frame of the R&D ESA “Europeanisation of Mil Std 1553B Data bus Products”
- This R&D aims to develop:
  - A 1553B Remote Terminal ASIC
  - An 1553B Analog Transceiver ASIC
  - the evaluation of European source of 1553B Transformers (MicroSpire)
  - MCM integrating these products
- The current presentation deals with the 1553B Remote Terminal

Why an IP core and not an ASIC ?

History (1/2)

- The technology selected for this digital ASIC was ATMEL MG2RTP using a low cost MG2RT044P matrix.
- MG2RTP was manufactured at MHS Nantes.
- Then ATMEL has announced the end of life of the MG2RTP process (09/2008).
- At that time a review of alternative technologies has been made .

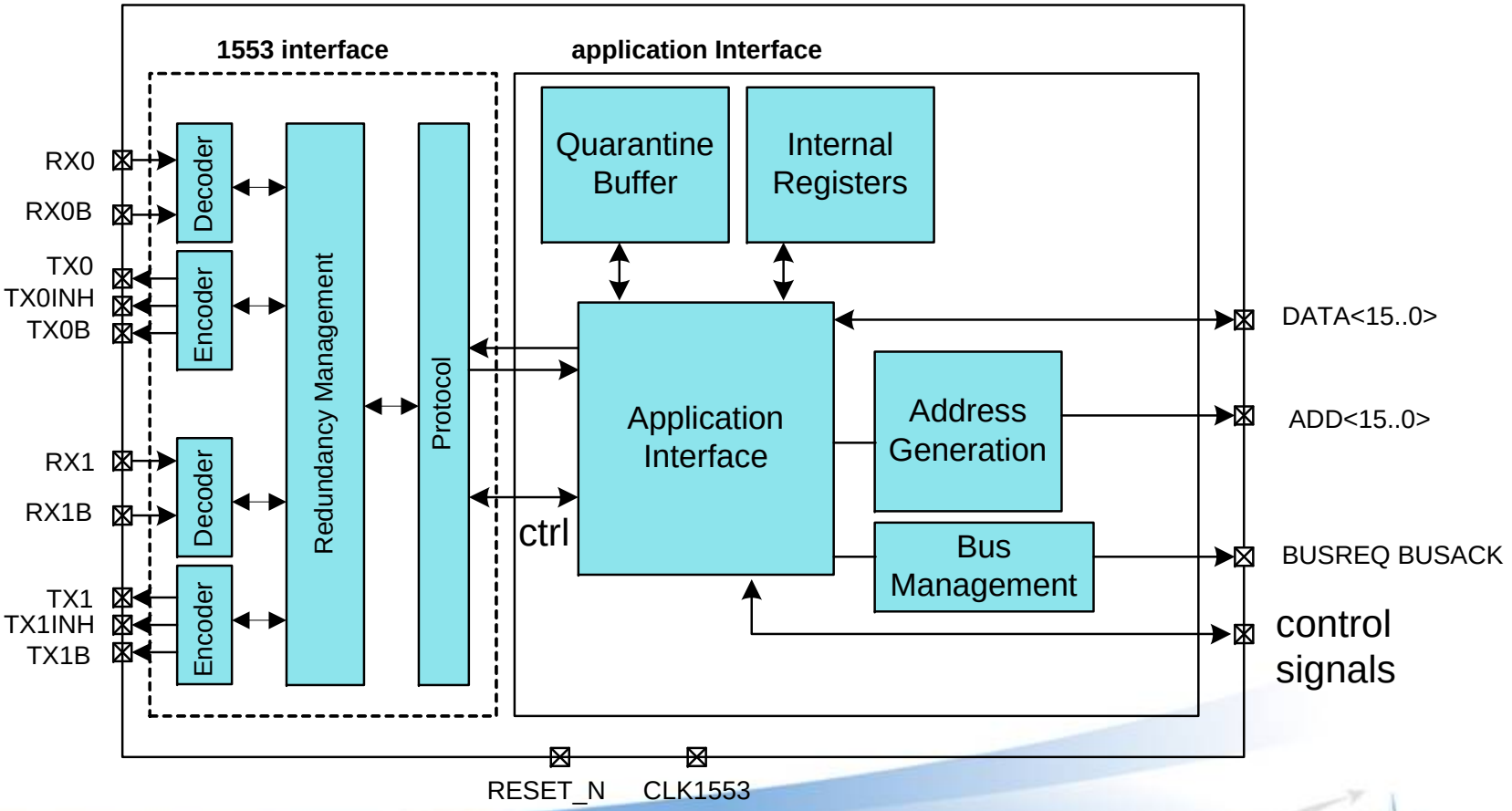
History (2/2)

- The following processes have been reviewed
  - ATMEL MH1RT
  - MHS 0,5 um -> no RT library, pereniality problems
  - XFAB 1 um SOI -> gate count too large
  - XFAB 0,6 um SOI -> LU insensitivity not proved
  - IHP 0,25 um -> no Hirel flow
- ATMEL MH1RT was a possible candidate but the part recurring cost would have exceeded an FPGA equivallent solution. Moreover ATMEL was not interested by having this product in their catalog as an ASSP.
- It has thus been decided to transform the ASIC into an IP

Characteristics of the IP Core

Block diagram of the IP core

- The RT53EUR is a classical dual bus Remote terminal

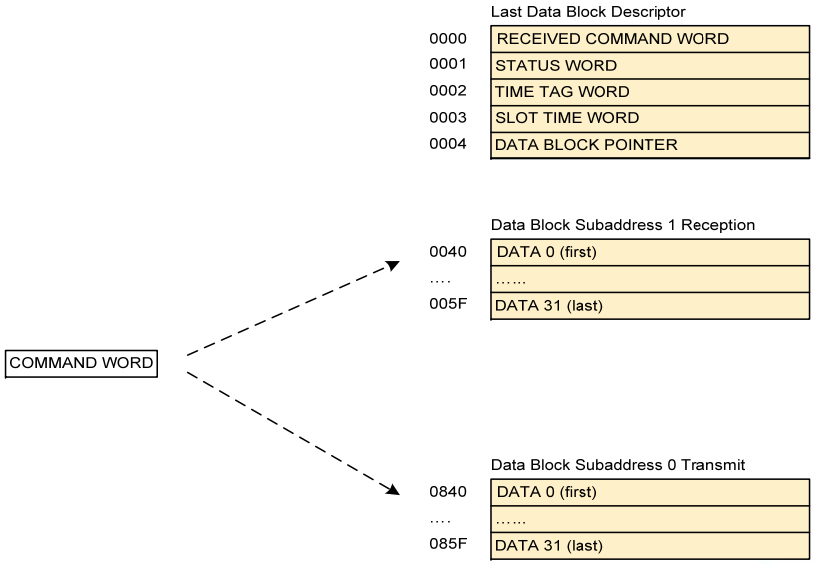


RT53EUR specific features

- The Clock of RT53EUR is configurable between 10 Mhz and 24 Mhz by step of 2 MHz.
- It is possible to legalize/illegalize and characterize all sub-addresses or mode codes
- RT53EUR generates a lot of internal interrupts : end of message, data received at a given sub-address, buffer full, new slot in the time tag
- Embedded wrap around function for testability purpose
- RT53EUR has 3 modes for the data management :
  - direct addressing
  - indirect addressing
  - circular buffer

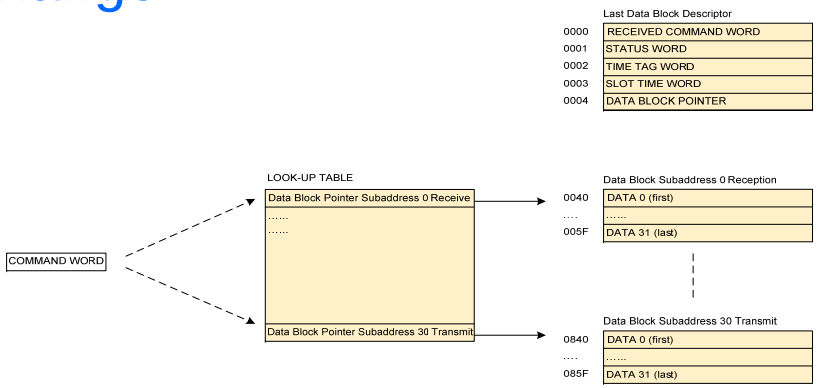
Direct addressing

- Data blocks addresses are dependant only on the message sub addresses
- A descriptor of the last exchange is stored at the end of the exchange
- This mode is compliant with ASP20/ASP55 used in Ariane5



Indirect Addressing

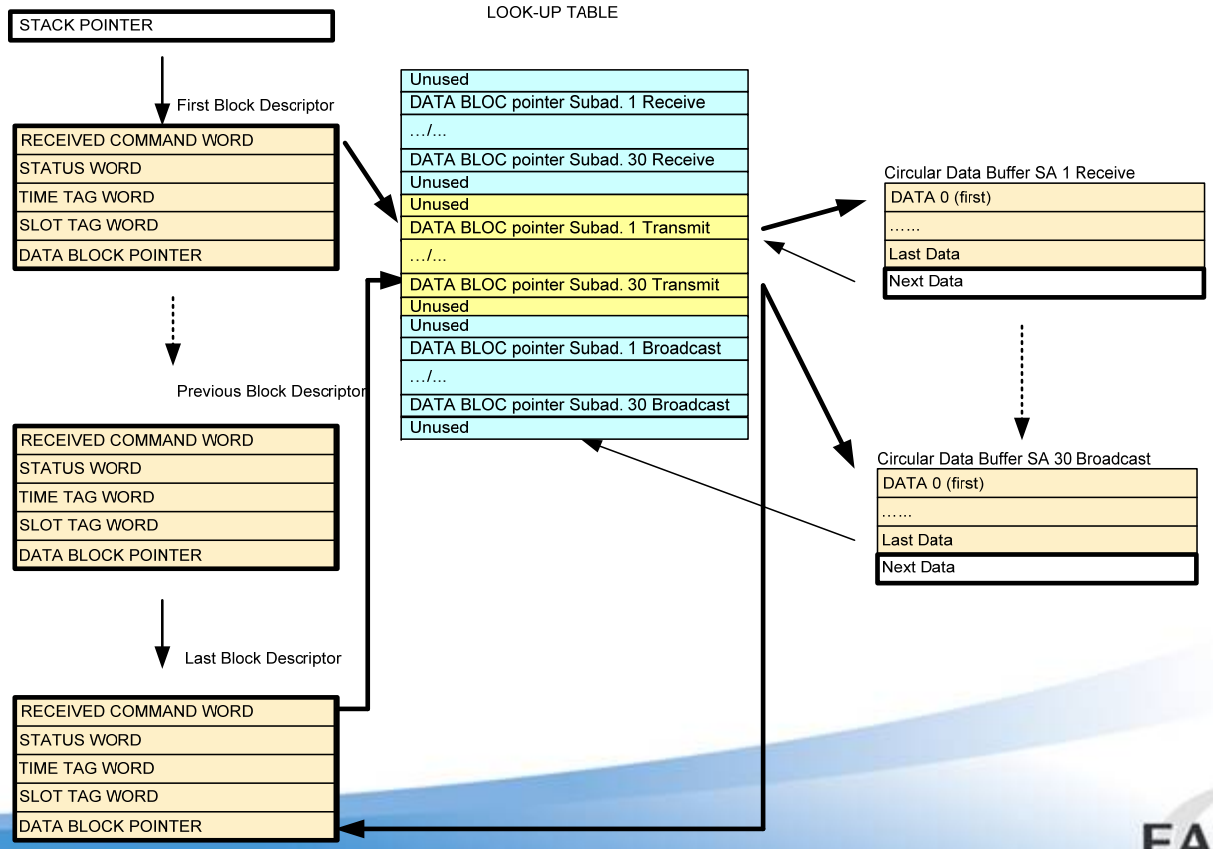
- Data blocks are dependant only on message sub addreses but an indirection is implemented by using a look-up table
- A descriptor of the last exchange is stored at the end of the exchange



- Data blocks are dependant only on message sub addreses but an indirection is implemented by using a look-up table

Indirect Stacked Addressing

- A descriptor of the last exchange is stored at the end of the exchange in a dual stack
- An updated look-up table provides the pointers to the circular buffers
- Data are stored in separated circular buffers for Subad and R/W.



RT53EUR features issued from ECSS group

- A real time clock is integrated managing 2 registers : time tag and time frame.
- It is possible to reset the time tag with the mode code synchronize with or without data word as requested by ECSS50-13 standard.
- EUR1553 uses 4 configuration registers
  - 1 : General configuration
  - 2 : Real Time Clock Configuration
  - 3 : Interruption Configuration
  - 4 : Application Interface configuration
- These 4 registers can be configured through 1553 (or Application Interface). This Configuration could be part of a configuration service discussed in ECSS.

Usage in FPGA/ASIC

- characteristics :
- ACTEL RTAX2000:
  - 12% of the FPGA + 1 Block RAM out of 64.
  - 24 MHz frequency reached easily
- ATMEL ATC18RHA
  - 1436 Flip flops (quarantine buffer of 32 w x 16 bits made with Flip flops)
  - 24 Mhz frequency reached easily
- IP has been validated using a Xilinx implementation
- VTP has been passed successfully

Availability

Availability & Support

- IP core is delivered with a data sheet and a user manual - contact ESA

- The support is ensured by Astrium ASE3 during 3 years : bug correction – improvement

Thank you – Questions ?