SYDERAL
Electronics and Software

Advanced Memory Controller IP Core
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MPD 2010

Microelectronics Presentation Days
March 30th to April 1st 2010

Outline

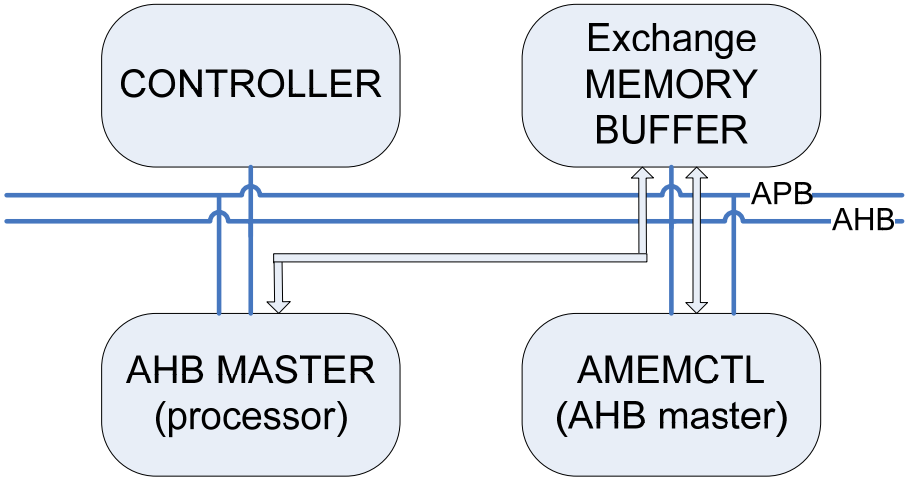
- IP Core Main Features and Typical Application
- Interfaces and Functions
- Memory Management
- Storage Protection Approach
- Implementation Status

IP Core Main Features

- Memory Controller IP For Solid State Mass Memories
- Block Based Data Transfer and Storage to Memory Banks
- Interface either Nand Flash or DDR2 SDRAM Devices or both
- Protect Stored Data Against Error Events

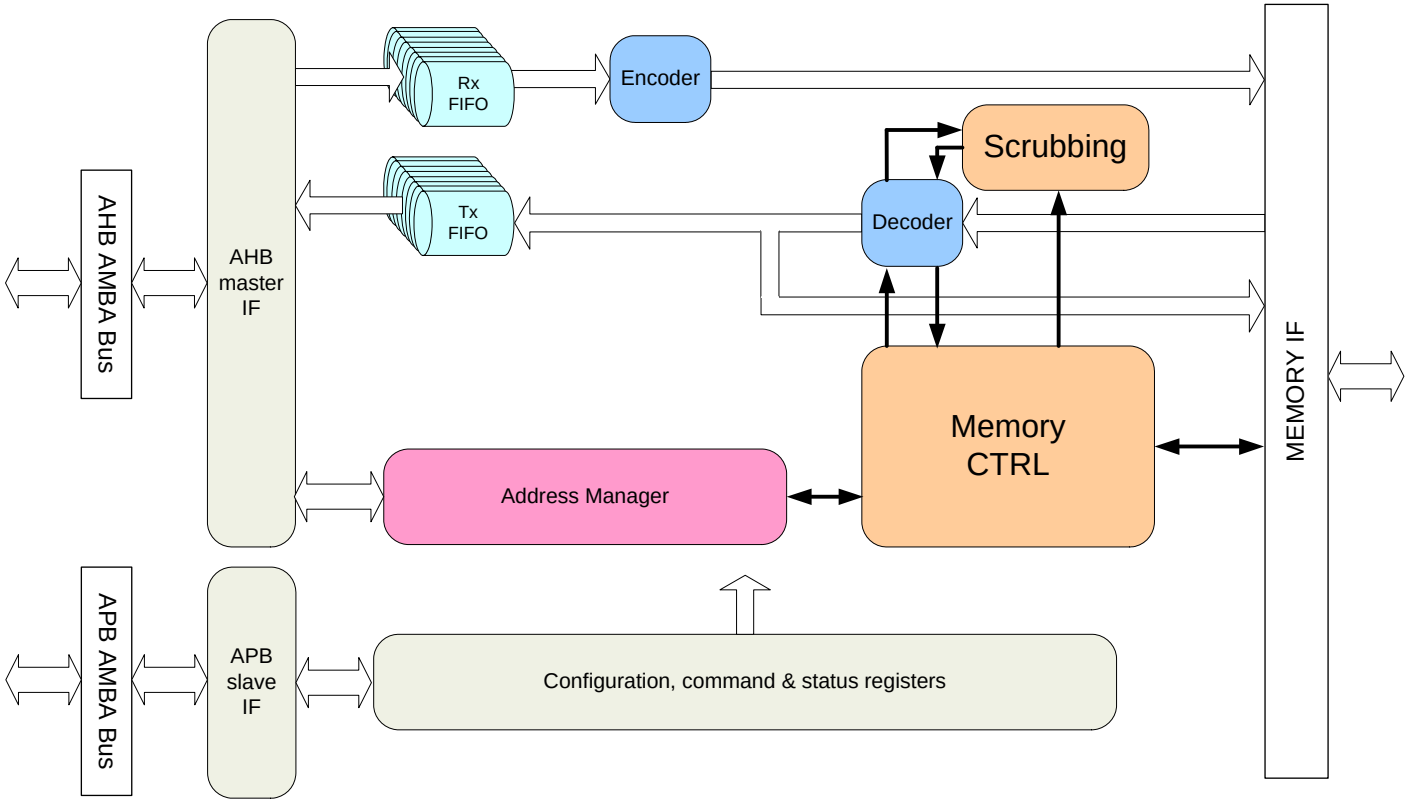
IP Core Typical Applcation

- Amba Bus Based System On Chip
- External Exchange Memory Buffer and Controller
- Direct Memory Access



Interfaces and Functions

- AMBA Bus Interface
- Memory Interface (Nand Flash / DDR2 SDRAM Physical Layers/both)
- RS Coding and Decoding
- Scrubbing
- Block Based Data Transfer



Memory Management

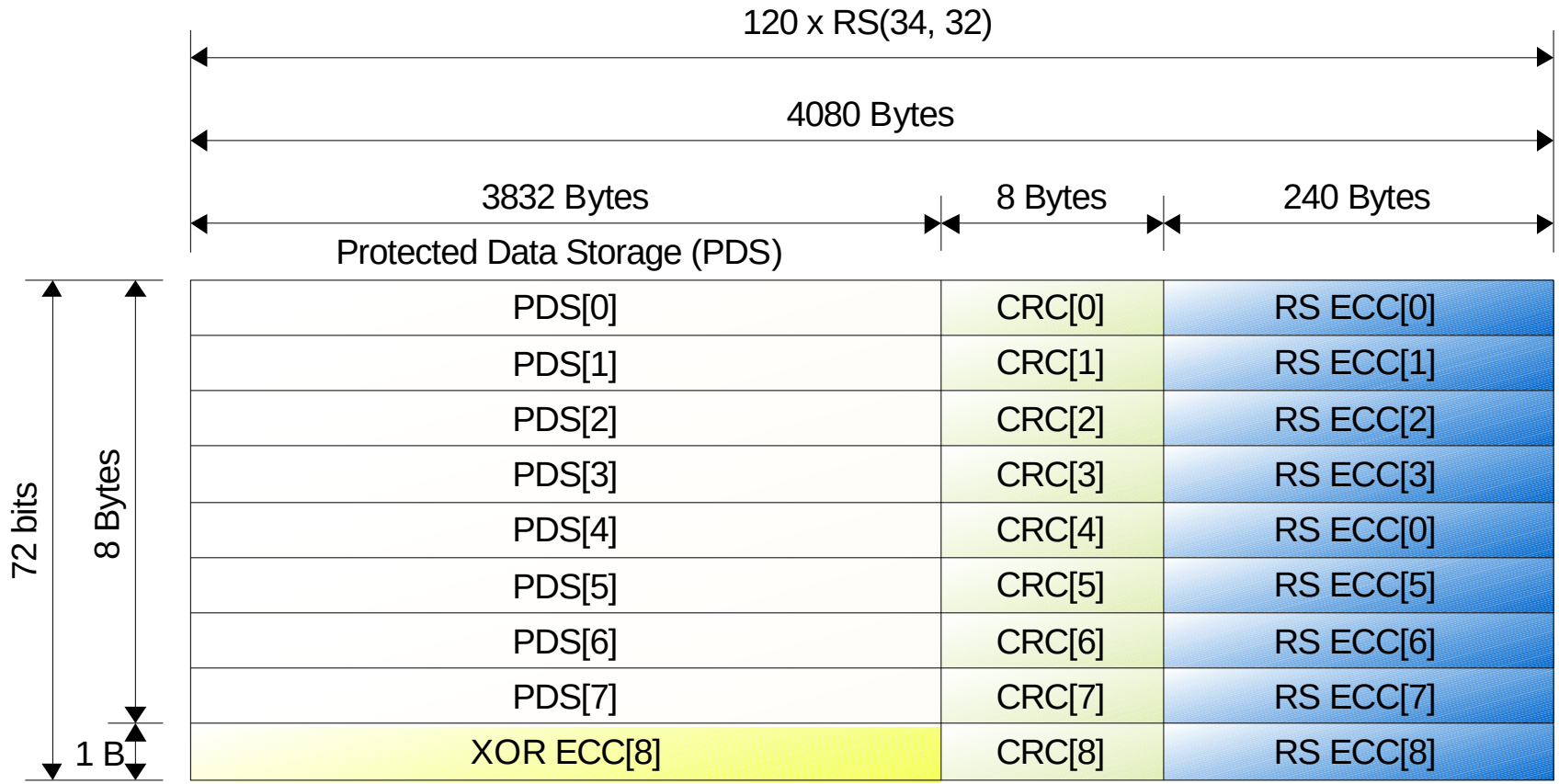
- Memory Devices Mode Management
  - ✓ Initialization
  - ✓ Auto-refresh/Self-refresh
  - ✓ Read/write(/erase) sequences
- Memory Testing (Blocks, Devices, Banks)
- Memory Scrubbing
- Event/status Reporting

Data Storage Protection

- Multiple bits error correction
- Non correctable errors detection
- Block Error Correcting Code based on RS(34, 32) Reed Solomon
- Erasure Correcting Code based on XOR Parity
- CRC based error detection
- Memory Scrubbing
- Recovery from one device failure data

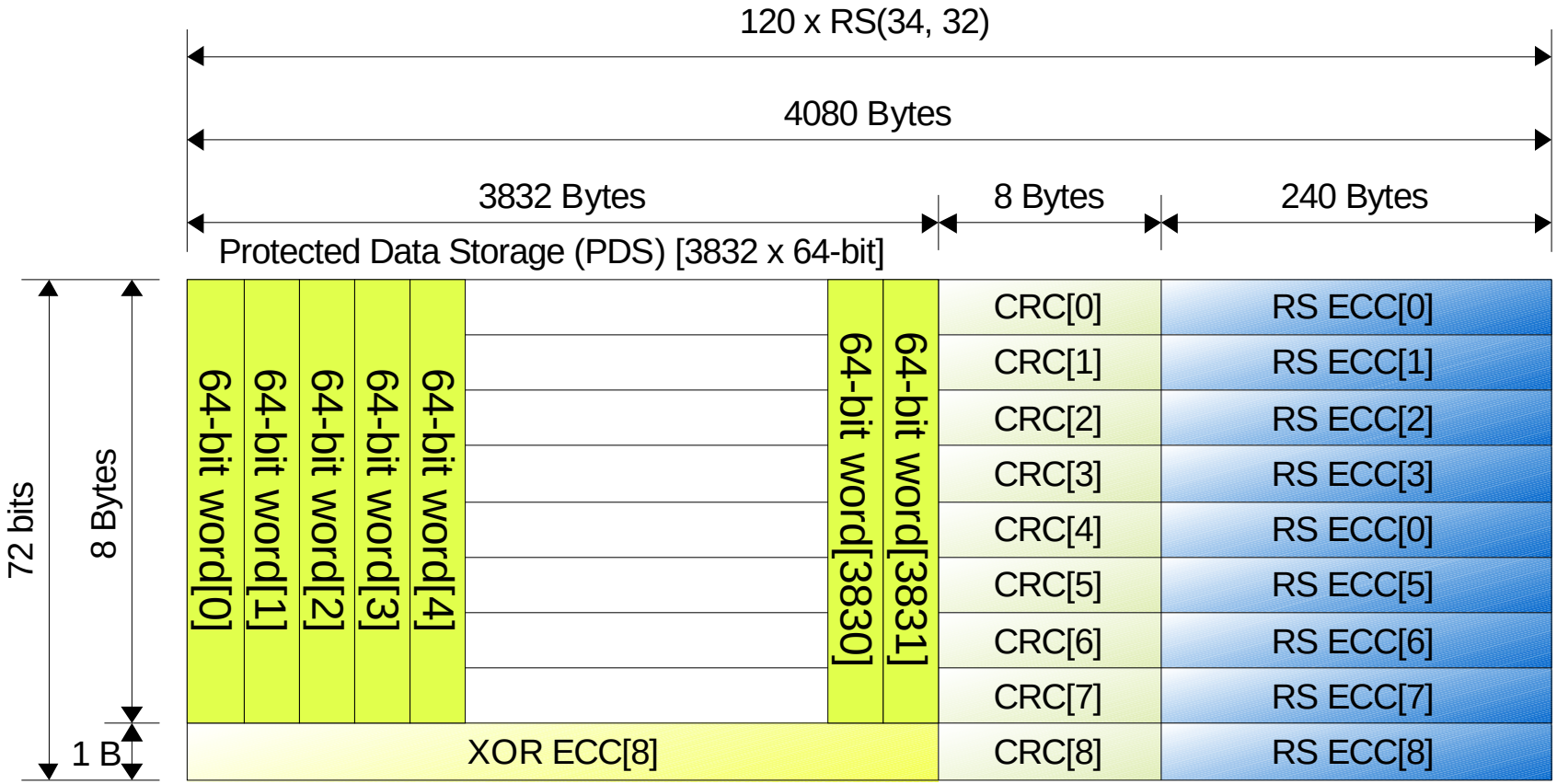
Data Storage Protection Example

Data Storage Protection Example



Data Storage Protection Example

29.9375 kB of Protected Data Storage
6 kB of Protecting Data Code
83.5% Storage utilization
Possible Interleaving Factors: 2, 3, 4, 5, 6, 8, 10, 12, 15, 20, 24, 30, 40, 60, 120



Development Status

- SRR completed
- Architectural design on going

Thanks
For Your Attention