ESA IP Cores
Present status and future plans

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Agenda

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Introduction

- What is an Intellectual Property (IP) core?
  - A reusable design in HDL format (VHDL, Verilog, etc).
  - ESA IP cores are "soft cores", i.e. technology independent.
    - Can be synthesized and targeted to any ASIC or FPGA technology.
- Why an IP Cores service by ESA?
  - Promote and consolidate the use of functions, protocols and/or architectures for space use (e.g. SpaceWire, CAN, TMTC, etc)
  - Counteract obsolescence and discontinuity of existing space standard ASICs
  - Facilitate the reuse of results from TRP/GSTP programs, thus reducing costs of large IC developments (e.g. Systems-on-Chip)
  - Centralize IP users' feedback to improve quality of existing IPs and identify future needs
  - *Not a profit-oriented service*

History and background

- ESA IP cores service originates from internal & external developments
  - Designs with high-reuse potential developed internally at ESTEC during late 90s – early 00s
    - CAN, LEON1/2, PTME, EDAC, etc
- IPRs granted to ESA for reuse and sublicensing externally developed VHDL designs (eg. SpWb, OBDH, etc)
- ESA contractors & non-ESA customers started requesting these designs for reuse in ESA contracts or private developments
- ESA Microelectronics Section, along with the Electrical Engineering Contracts Service, established the service in 2003, after a growing number of requests
  - Aim was to regulate & normalize the reuse of these designs

List of available IP Cores

- 14 IP Cores available

SpW-b	SpaceWire CODEC	**PTCD**	CCSDS Packet Telecommand Decoder. VHDL model of MA28140 chip by GEC-Plessey Semiconductors
SpW-RMAP	SpaceWire CODEC with RMAP support	**RT53EUR**	MIL-BUS-1553B Remote Terminal
SpW-AMBA	SpaceWire CODEC with AMBA interface	**OBDH**	On-Board Data Handling bus
LEON2-FT	32-bit microprocessor (SPARC-compliant)	**CUC-CTM**	CCSDS Unsegmented Code (CUC) & CCSDS Time Manager (CTM)
PTME	Packet Telemetry Encoder	**EDAC**	Error Detection And Correction Encoder/Decoder
CAN	Controller Area Network	**EVI32**	32-bit VMEbus interface for the ERC32 processor chip set
PDEC	CCSDS Packet Telecommand Decoder	**WIC**	Wavelet

- Deliverables with each IP core distribution
  - Documentation
  - VHDL source code
  - Testbenches
  - Simulation and synthesis scripts

New IP cores

- Ready for release (in 2Q10) :
  - RT53EUR
    - MIL-BUS-1553B Remote Terminal (Astrium Elancourt)
  - OCP-based IPs
    - LEON2-OCP (Magillem)
      - LEON2-FT model with OCP socket interfaces for the caches
    - SpW-OCP (Astrium SAS)
      - SpaceWire CODEC with OCP sockets
        - Based on SpW-AMBA from Astrium SAS
    - OCP-AMBA bridges (Magillem)
      - OCP-AHB and OCP-APB
        - Protocol translators between AMBA and OCP
  - IP-XACT XML wrappers for ESA IP Cores
    - Available for :
      - LEON2-FT (both AMBA and OCP versions)
      - SpW-AMBA / SpW-OCP
      - OCP-AMBA bridges
- Under development:
  - CANOpen (CAEN Aurelia)
  - Mass Memory Controller (Syderal)

Overview of ESA IP Cores service

- How to obtain an ESA IP core:
  - Get details about available IP cores (from ESA IP cores website)
  - Fill in and submit an IP request form
  - IP request screening and license preparation by ESTEC/ESA
    - Each IP core has different licensing conditions / restrictions!
  - Delivery of requested IP Core(s) to customer
- Pre-compiled simulation models available upon request (for evaluation purposes; no license required!)
- Details and information on ESA IP Cores webpage
  - http://www.esa.int/TEC/Microelectronics/SEMVWLV74TE_0.html
    Documents can be downloaded directly from the IP cores website

Licensing

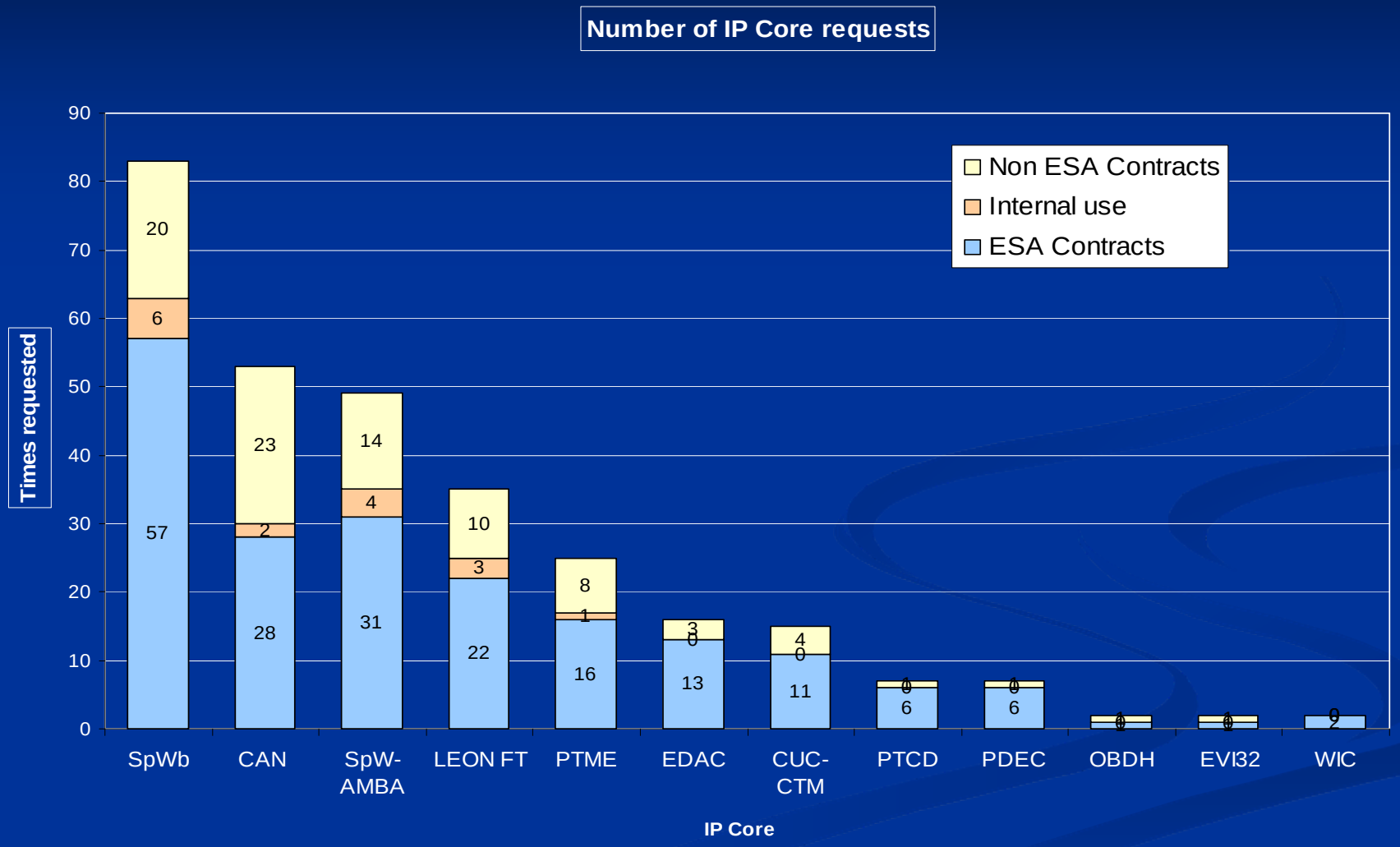
- General licensing terms & conditions
  - Non-transferable
  - Non-exclusive (except after explicit agreement)
  - Issued only within ESA member/participant states territory
  - R & D and/or commercial application
  - Peaceful, non-military application
- Specific terms and conditions
  - For ESA-funded activities => License appended to the contract (Contract Change Notice, CCN)
    - Limited to objectives, scope and duration of activity
    - Free of charge
  - For company-funded activities => Stand-alone license
    - Issued for licensee's "own purposes"
    - 5 years duration
    - Nominal fee
- Full licensing details and info on the website: http://www.esa.int/TEC/Microelectronics/SEM6SCV681F_0.html

Technical Support

- Due to limited resources, ESA cannot commit to systematic technical support
  - Limited to announcements of new releases, known and independently verified problems, etc.
  - Technical support mainly subcontracted externally
    - University of Dundee (SpaceWire-b)
    - Aeroflex Gaisler (LEON2-FT)
    - CAEN Aurelia (CAN)
  - Priority given to ESA-funded activities

- ESA IP Cores Users' Forum
  http://tech.groups.yahoo.com/group/ESA_IPCores/

Usage Statistics (April 2002 – March 2010)



Additional info: SpW-RMAP = Requested + delivered 7 times for use in ESA projects

ASIC/SoC developments (re)using ESA IP cores

- 10-port SpaceWire Router (SpW-10x) – Atmel AT7910E
- SpaceWire Remote Terminal Controller (SpW-RTC) – Atmel AT7913E
- General purpose SPARC V8 32-bit microprocessor for space (Atmel AT697E/F)
- Spacecraft-Controller-On-a-Chip (SCOC3) – FM expected May 2010
- Advanced Galileo/GPS ASIC (AGGA4)
- Multi-DSP/Microprocessor Architecture (MDPA)
- Deep Space Transponder (DST) – BepiColombo
- Scalable Multi-channel Communication Subsystem (SMCSs)
- More …

  - Further info on "SoC development activities" webpage: http://www.esa.int/TEC/Microelectronics/SEMRWGV681F_0.html

Space missions using ESA IP cores

TEC-EDM	29/03/2010	IP CORES											
		CAN	CUC-CTM	EDAC	EVI32	LEON2-FT	OBDH	PDEC	PTCD	PTME	SpaceWire-AMBA	SpaceWire-b	TOTALS
MISSIONS	GAIA					ASIC					X	X	3
	Geo MS	X	X	X	X		X	X	X	X	X	X	10
	Spanish Space Observation Satellite (CRISA 2003) - PAZ	X	X				X						3
	Foton M3	X						X	X				3
	BepiColombo	X	X	X		X, ASIC		ASIC		ASIC	X	X, ASIC	6
	Exomars	X				ASIC					X	X	3
	Sentinel-1	X									X	X,ASIC	3
	Sentinel-2			X									1
	Sentinel-3										X	ASIC	2
	EML	X										X	2
	ERB-2 (Erasmus Recording Binocular 2)	X										X	2
	WatSen											X	1
	Proba-2		X			X, ASIC				X			3
	Proba-3		X	X		ASIC		X	X	X	X	X	7
	Maser-10		X	X				X	X	X	X	X	7
	MHS-2 (?)											X	1
	NPAL (Mercury)											X	1
	AlphaSat			X		ASIC						X, ASIC	3
	Galileo	ASIC						ASIC		X, ASIC			3
	KaTE									X			1
	Smart-1									X			1
	ATV								X	X			2
	LisaPF									ASIC			1
	AlphaBus								X				1
	ADM-Aeolus							ASIC		ASIC			2
	SWARM					ASIC		ASIC		ASIC			3
	EarthCare					ASIC							1
	SmallGEO					ASIC							1
	ASTROsar (France)												
								ASIC		ASIC	ASIC		3
	TOTALS	9	6	6	1	9	3	9	6	8	9	14	

ESA activities on IP cores and System-Level Modeling

- SystemC TLM models of ESA IP cores
  - Already developed:
    - LEON2/3
      - Fully functional. Cycle accurate version being verified
  - Under development
    - SpaceWire (Qualtek)
    - Subset of GRLIB - MCTRL, AHB, MMU, GPTIMER, etc. (IDA Braunschweig)
    - Virtual Platform infrastructure (IDA Braunschweig)
  - Planned
    - CAN
    - Others?

Conclusions

- IP cores portfolio updated with new modifications, enhancements and additions (SystemC models, Virtual Platforms, OCP sockets); activities planned to extend ESAs IP cores library
- Many of these IP cores have already been used (or planned to be used) in:
  - Various ESA missions
  - As basis for research and developments in the areas of SoC technology, high level modelling and simulation, on chip interconnect architectures, etc.
- Existence and promotion of the ESA IP cores has greatly contributed to:
  - Shorten IC development times
  - Foster the adoption of new standardized communication protocols (SpW, CAN, CCSDS TM/TC) and LEON-based on-board computer architectures.

THANK YOU !

QUESTIONS ?