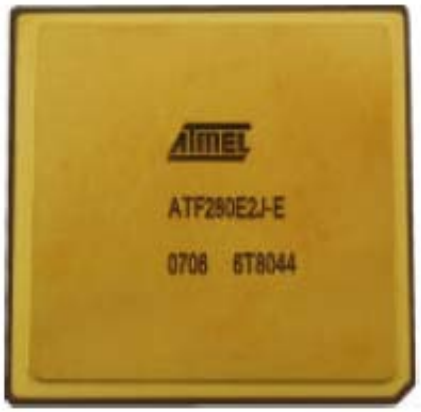
ESA SpW IP Core
in Atmel FPGA ATF280



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Summary

SIMBIO-SYS

- Context
  - Mission : Bepi-Columbo
  - Instrument : Simbio-Sys / Main Electronic (IAS)
  - Purpose : image compression
- Main Electronic – Simbio-Sys
  - Synoptics
  - Prototype boards
- SpaceWire in ATF280
  - RX clock recovery
  - Test design

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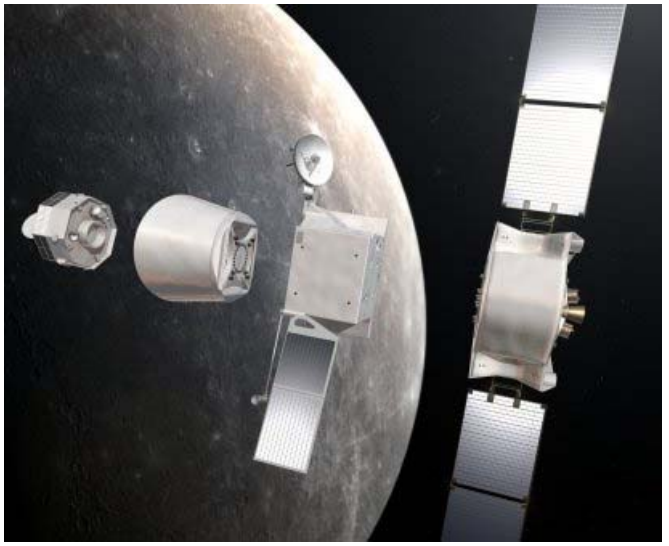
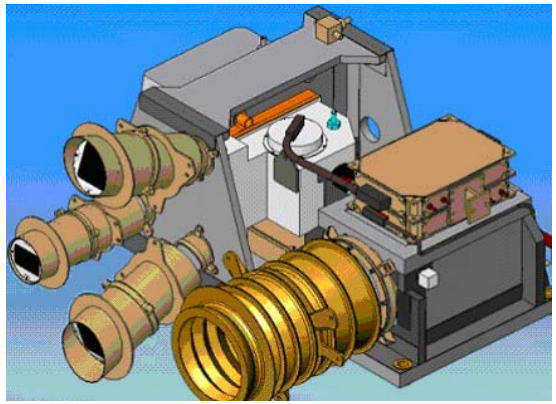
Context : Bepi-Columbo / SimbioSys

SIMBIO-SYS

- ESA (MPO) / JAXA (MMO) cooperation for Mercury exploration
- MPO = 11 instruments
- Simbio-Sys : Mercury surface study
  - HRIC : High Resolution Channel
  - STC : Stereo Channel
  - VIHI : Vis/NIR spectrometer
- IAS (Co-PI Simbio-Sys) in charge of Main Electronic (ME)
  - S/C interface
  - Cameras interface
  - Image compression (Y.Langevin algorythm)

  => ~70% of the data of MPO mission





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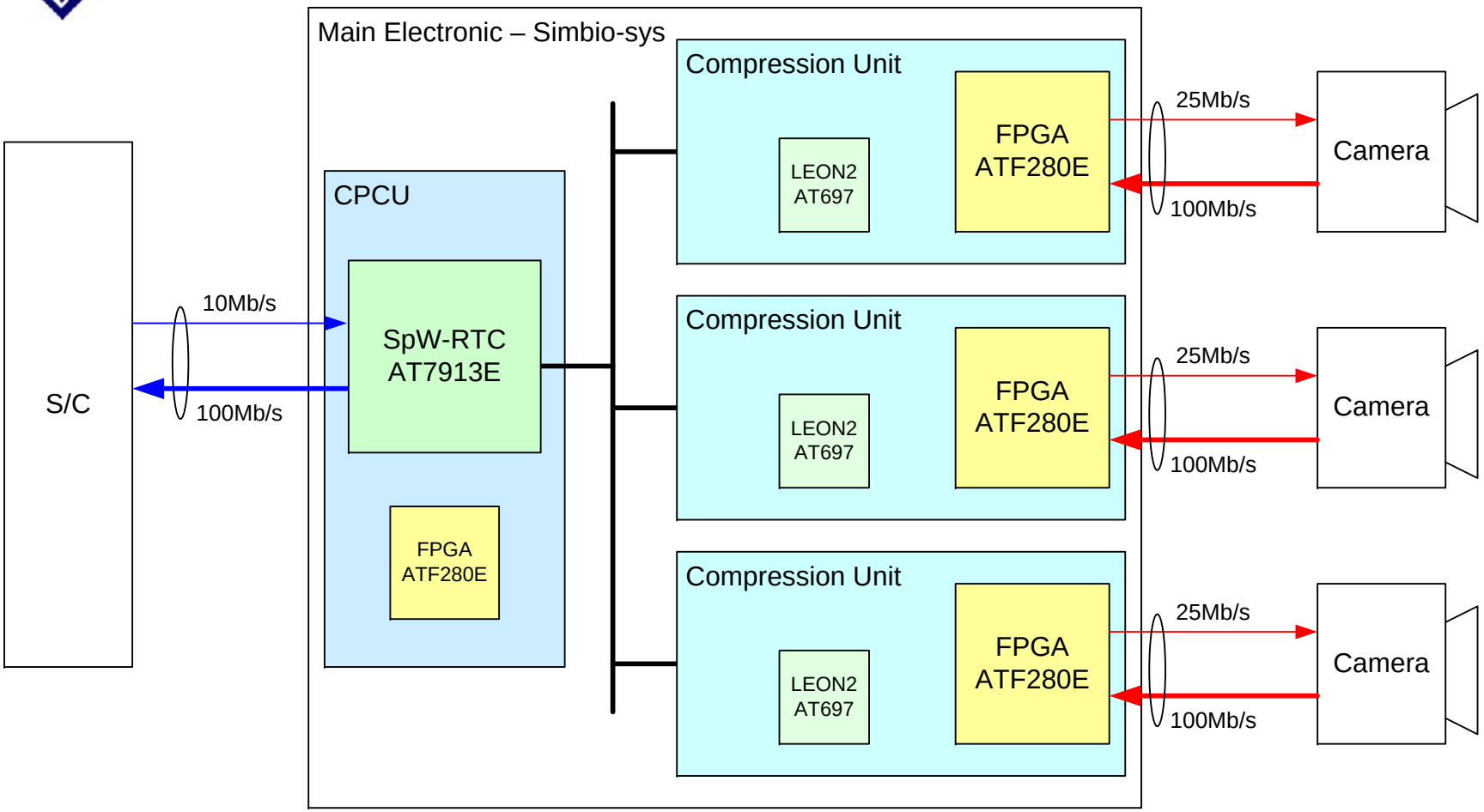
Main Electronic – Simbio-Sys

SIMBIO-SYS

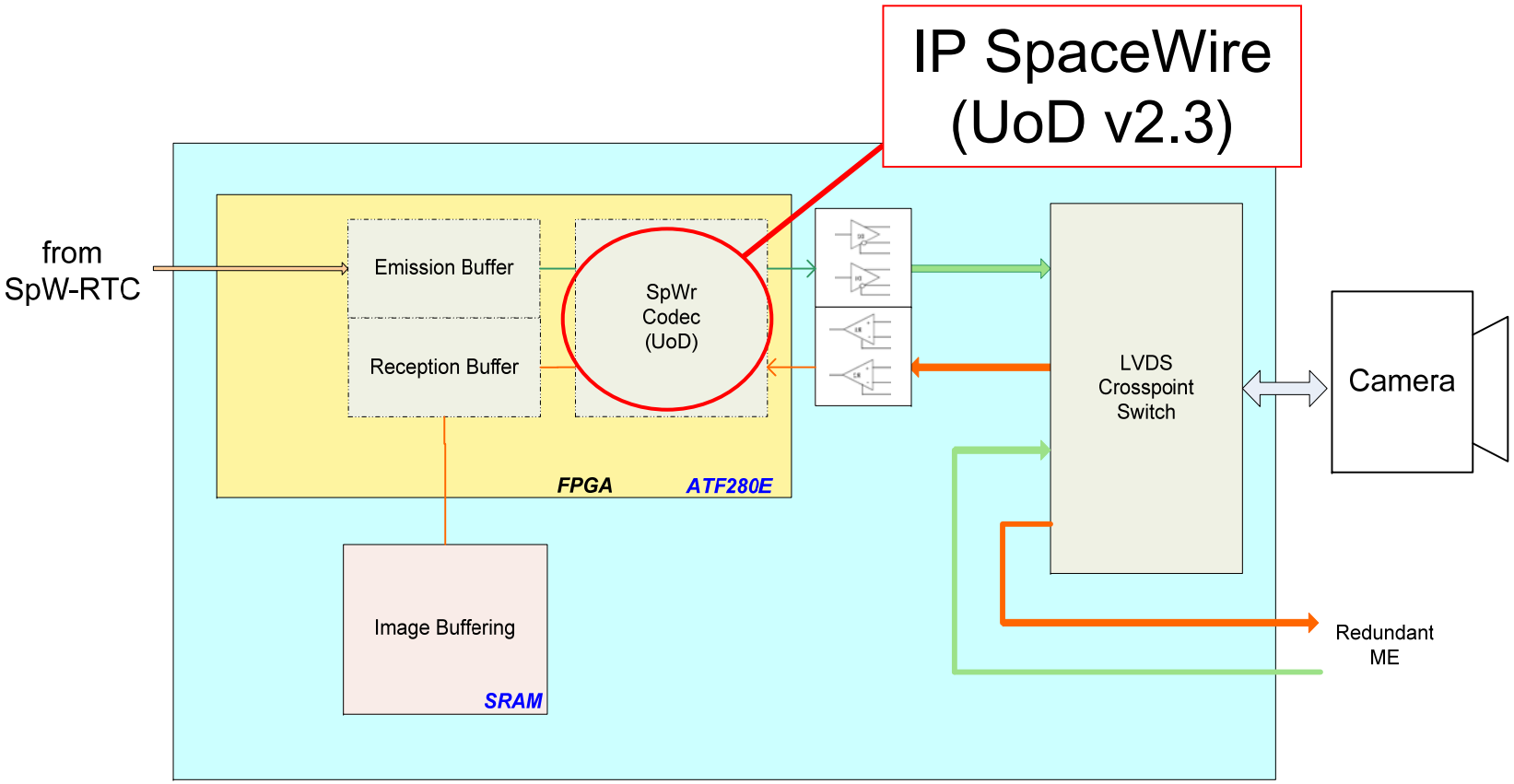
Overview



Main Electronic – Simbio-Sys

SIMBIO-SYS

SpaceWire on the CU side



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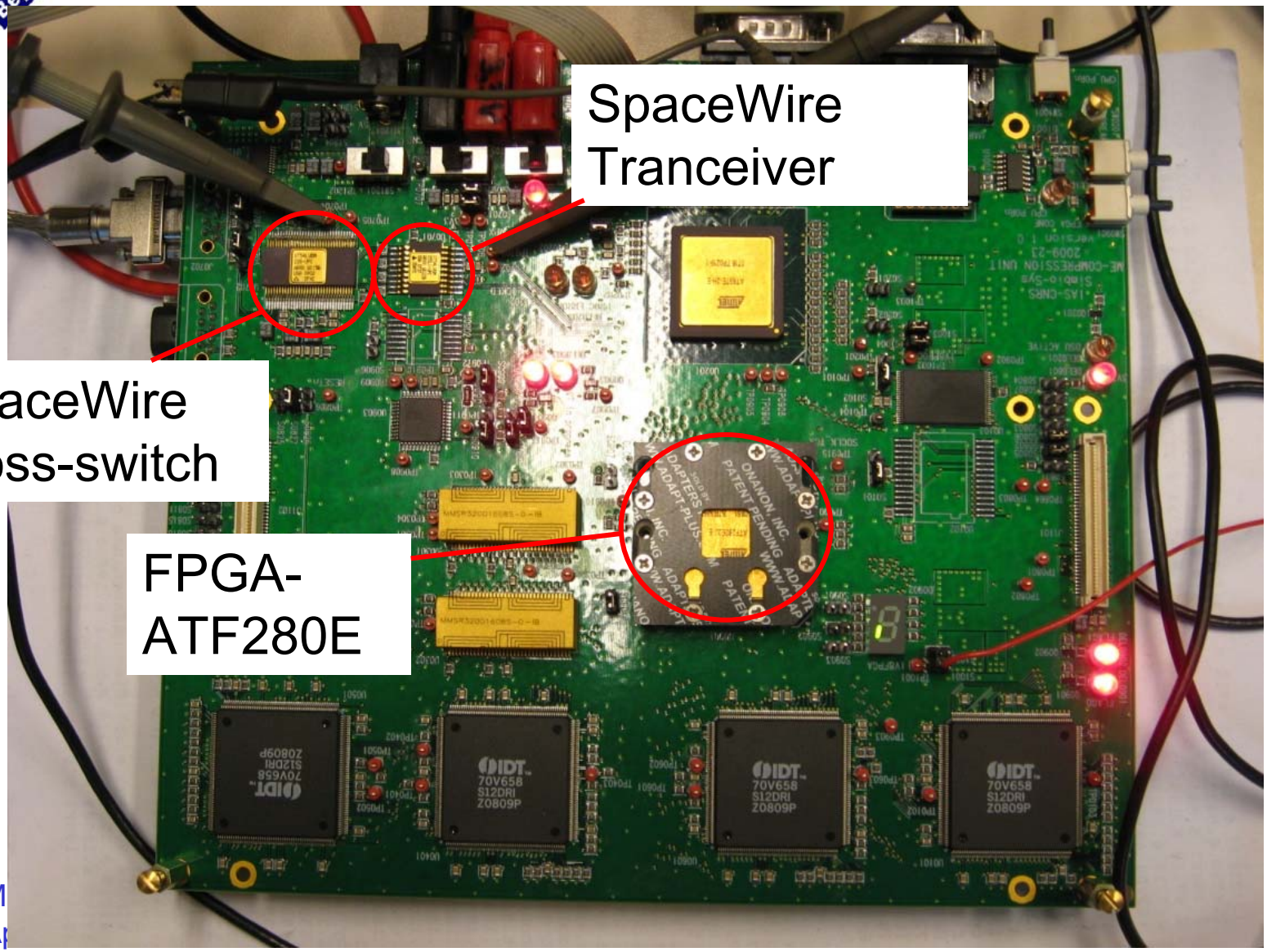
Main Electronic – Simbio-Sys

SIMBIO-SYS

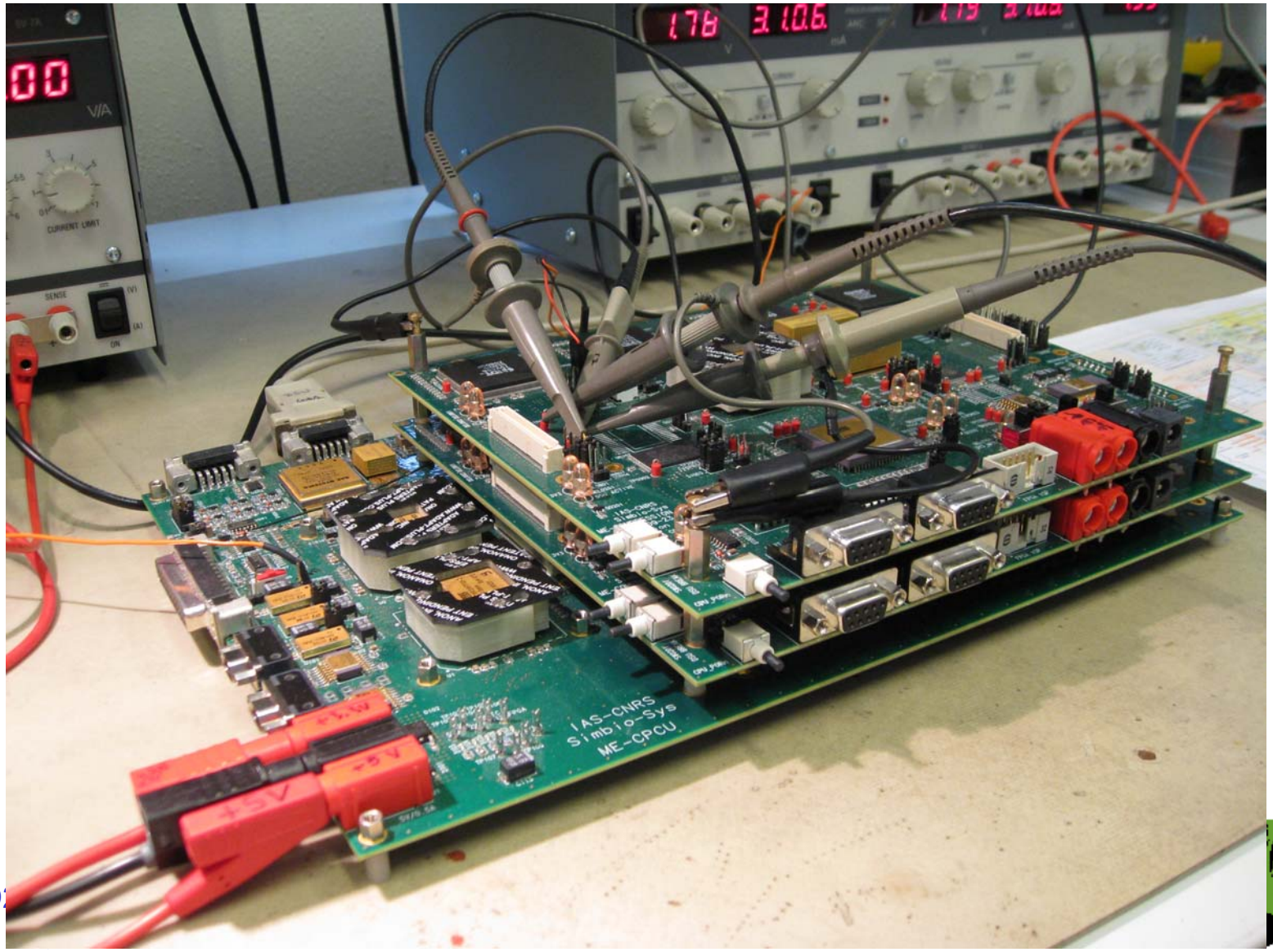
CU prototype board



Main Electronic – Simbio-Sys

SIMBIO-SYS

2xCU mezzanine plugged on the CPCU proto



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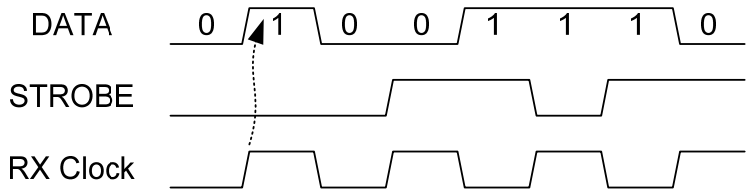
SIMBIO-SYS

Receive clock recovery & DATA sampling

- RX_CLK is generated by XOR-ing DATA and STROBE inputs



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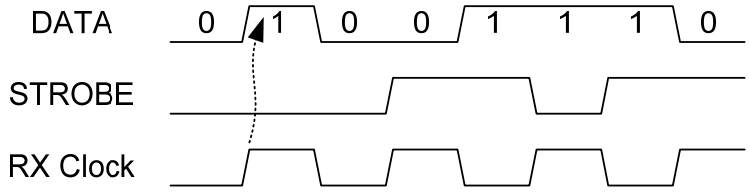
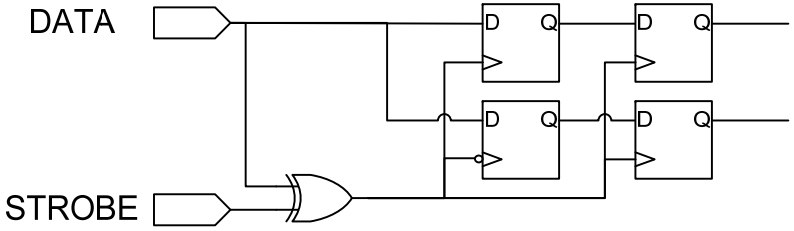


- DATA is sampled on rising and falling edge of RX_CLK



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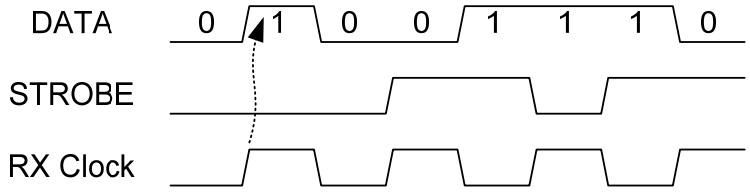

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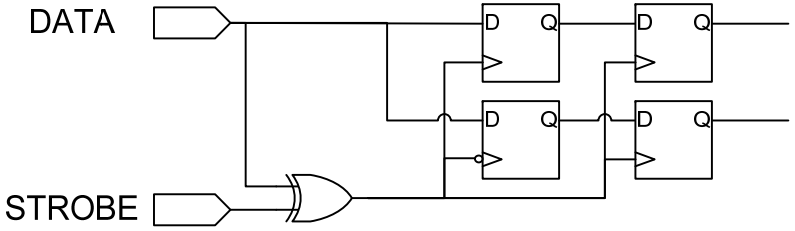
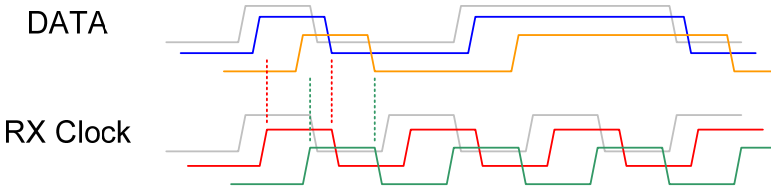


- In the real world, timings are very important !!!



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SIMBIO-SYS

Atmel IDS P&R tool

- RX_CLK is a “derived clock” in IDS
- Atmel’s tools cause troubles on some derived clock
  - →no way to Place&Route with “Timing Driven” option
  - →no Max frequency report for RX_CLK

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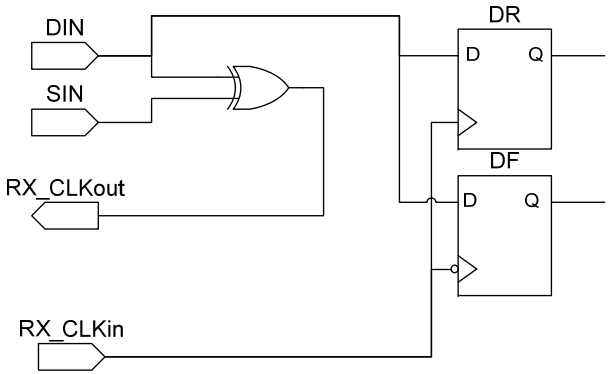

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Spacewire in ATF280E

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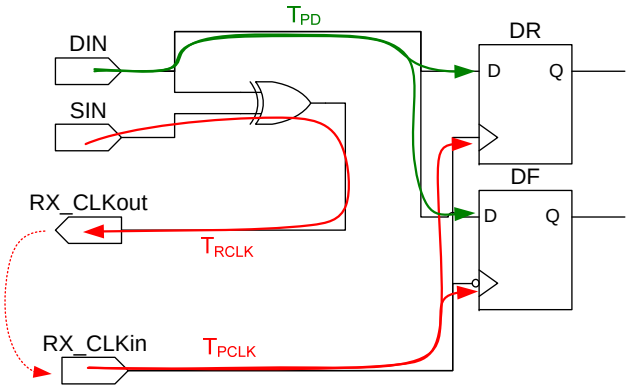


- RX_CLK timings (max of ATF280E characterization):

  DIN/SIN pads → RX_CLK_out :

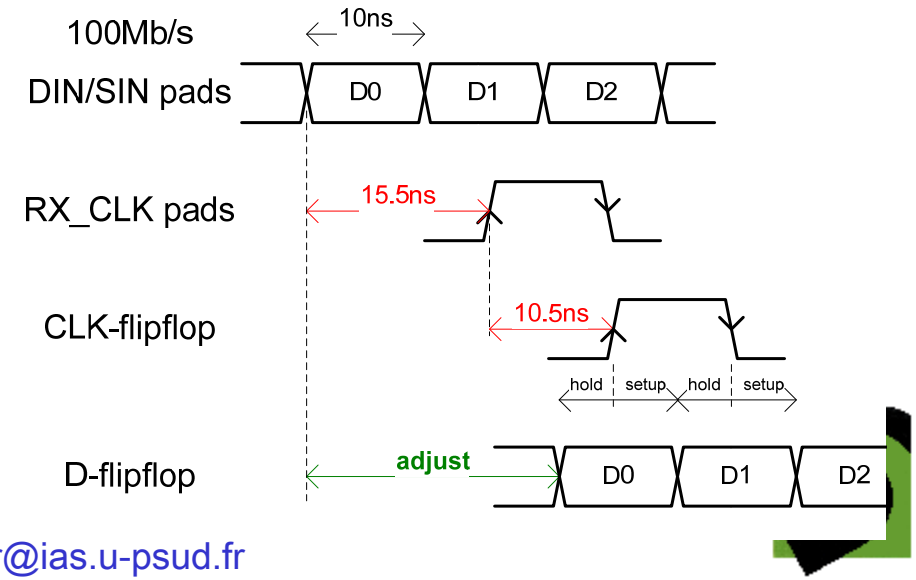
  $T_{RXCLKout}$ = ~15.5ns

  RX_CLK pad → CLK-input of registers :

  T_{PCLK} = ~10.5ns

  DIN/SIN pads → D-input of registers :

  T_{PD} = adjusted manually



MPD2010, ESTEC
April 1st, 2010

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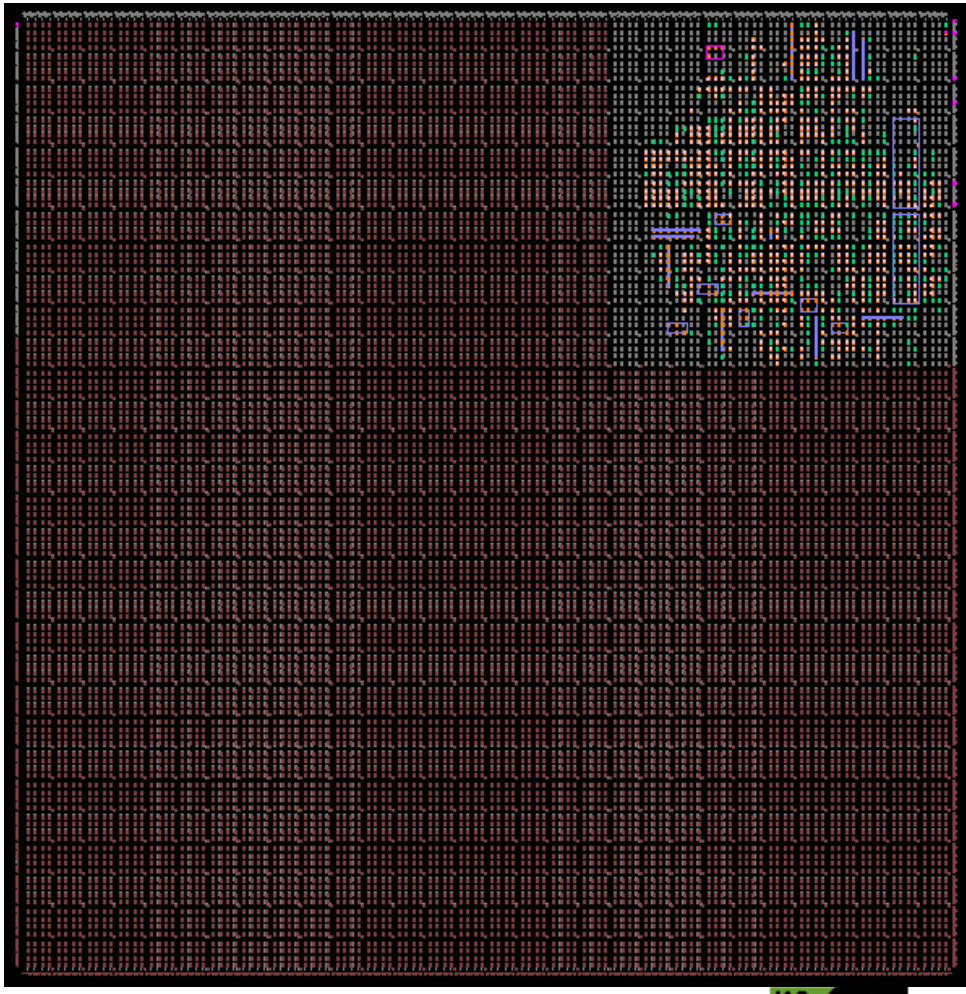
Spacewire in ATF280E

SIMBIO-SYS

Test design

- Simple design
- Only the IP Spacewire (UoD v2.3)
- Echo data from RX channel to TX channel
- System clock = 25MHz (→TX_CLK)
- RX FIFO 32 bytes
- Constrained area



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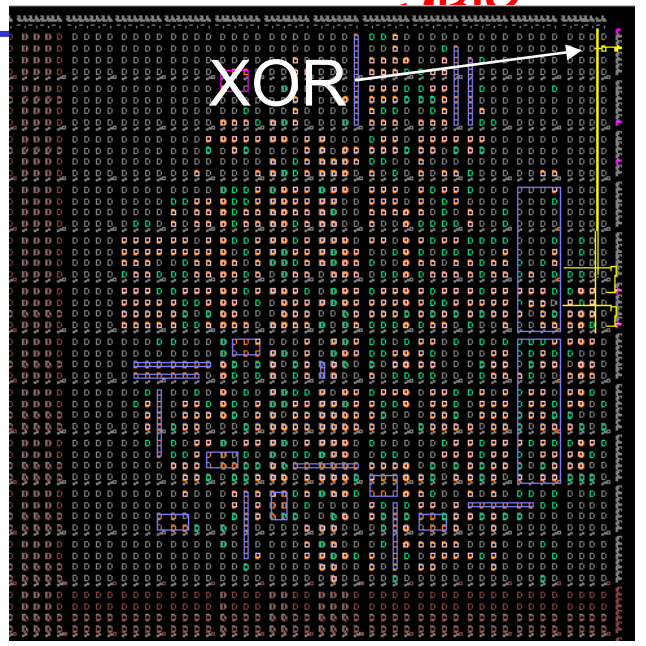
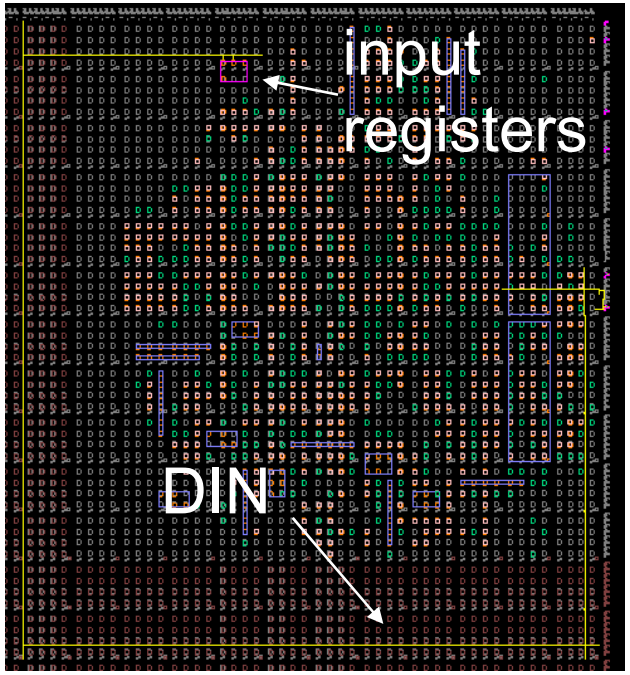
Spacewire in ATF280E

Test design





- To achieve best RX bit rate :
  - RX clock looped back outside FPGA
  - The signal between DIN data input PAD and the two input registers is delayed (manually routed) to respect the Setup/Hold timing with respect to the rising and falling edges of RX clock

- Performances :
  - Emission rate : 25Mbit/s
  - Reception rate : 120Mbit/s
  - FPGA area : 5%

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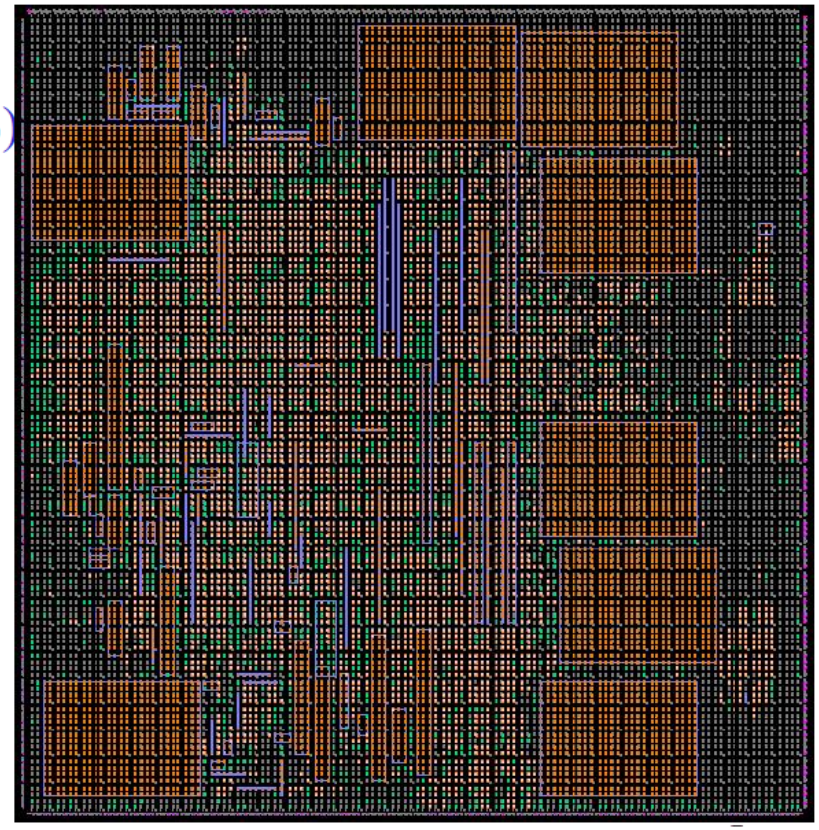
Spacewire in ATF280E

SIMBIO-SYS

- Complete design with WT,MMU and SpaceWire
- 10391/14400 Core Cells (72%)
  - –9313 Core Cells by netlist instances(64.5%)
  - –1078 Core Cells for routing (7.5%)
- Fmax = 7.55MHz
  (tested at 10MHz in laboratory)
- SpaceWire links :
  - –TX : 10Mb/s
  - –RX : 40Mb/s

(No effort done here to improve RX bit rate)



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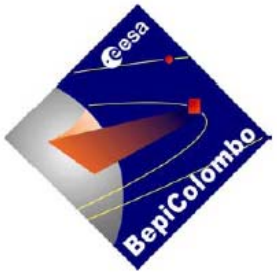

Spacewire in ATF280E

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Thank you for attention

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