EV10AS180 A new European 10-bit 1.5GSPS ADC for Space applications - *TRP ESA A05528*

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V. ROZAN
J.P. AMBLARD

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Agenda
A new 10-bit 1.5 Gsps ADC for Space applications EV10AS180

- e2v/BMS in brief
- ADC 10-bit 1.5GSps development
  - Context
  - Objectives & Challenges
  - Achievements
  - Performances obtained on First silicon
  - Reliability and Radiation Preliminary Evaluation
- Project Highlights
- Next steps: scope, objectives, schedule
- Conclusions

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e2v BMS Business Unit
Overview

Broadband Data Converters

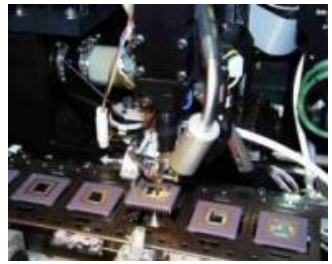
- Commercial & Industrial grade data converters: 8 -10bit/5Gsps to 12-bit/500Msps
- Military & Space grade data converters: 8-bit/1Gsps to 10-bit/2.2Gsps
- ASSPs and ASICs: commercial through space grades

Hi-Rel Microprocessors

- Hi-Reliability Microprocessors : 68K and Power Architecture
- Integrated & Communication Processors : QUICC and PowerQUICC families
- System Interconnect products: PCI Bridge / Memory Controllers, RapidIO switches

Assembly & Test Services

- Ceramic Package Design, Simulation, Characterization and Sourcing
- Ceramic Package Assembly, up to QML Class V quality grade,
- Test Engineering: test hardware and software development
- Production testing: wafer-level probing and package testing over temperature
- Long-term product support through foundry transfer or wafer banking



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e2v
Assembly & Test Capabilities

- One Stop Shop
- Specific services for customised solutions
  - **Assembly : Development & production**
    - **Ceramic package**
    - **Organic substrate (outsourced)**
  - **Test : Development & Production**
    - **Wafer / Dice (-55°C to +125°C)**
    - **Finished devices (-55°C to +125°C)**
    - **Burn-In**
- Global offer based on e2v Grenoble expertise
  - **Complex Digital Circuits - Microprocessors, Memories, Asics**
  - **High Frequency Data Converters and other RF transmission devices**
  - **Image Sensors - CCD, CMOS Sensors**

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Project Context

Fast, Low power, Broadband Rad hard ADC's
➔key enabling components in Space applications

- Requirements in Telecommunications (but also telemetry, GNSS, SAR)
  - Most of the telecommunication payloads will be **digitally processed**
  - **Need to process larger useful bandwidths**
  - Optimize the use of **scarce spectrum**
  - Best **operational flexibility** expected by operators and end-customers for new services

- For such systems designed in a tough competitive context, the European Space industry requires European Sourced advanced components (in particular **ADC & DAC**)
- In 2008, e2v was awarded by ESA contract to develop the 10-bit 1.5 GSps ADC for the Space industry, in partnership with end-users TAS & EADS Astrium (e.g specification and validation) and with support from CNES

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Objectives of the Project
A05528 TRP ESA Phase 1

- **Main Features**
  - 1.5 GSps guaranteed Conversion rate
  - **Low power** 1.7W in 1:2 DMUX mode
  - **L-Band** input Frequency up to 1.8GHz
  - **Integrated DMUX** (1:1, 1:2, 1:4)
  - Radiation Hardened #100kRad

- **Key Performances**
  - Single Tone performance @ Fs=1.5Gsps, -12 dBFS :
    - SFDR = -62 dBFS; ENOB =8.5-Bit; SNR = 55 dBFS at Fin= 750 MHz
    - SFDR = -60 dBFS; ENOB =8.2-Bit; SNR = 53 dBFS at Fin= 1800 MHz
  - Broadband performance:
    - NPR = 45 dB at -13dBFS *optimum loading factor in 1st Nyquist*
    - NPR = 43 dB at -13dBFS *optimum loading factor in L-band*

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Achievements of the Project
A05528 TRP ESA Phase 1

- ADC 10-bit 1.5GSps Die in B7HF200
- CI-CGA255 package
- Evaluation board EV10AS180GS-EB

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ADC 10-bit 1.5Gsps Die in B7HF200
Technology, Radiation & Reliability

- ADC designed in **B7HF200 SiGeC** from Infineon derived from B7HF
  - One of the fastest European technology (fT >200GHz)
  - With excellent & reliable modelling for simulation of performances
  - And proven reliability
- Full bipolar design strengthens the high level of radiation hardening
- Radiation & Reliability: Key Target values

Useful life tB	20 years
Early failure rate	20 dpm / 1000h
Radiation total dose	100 Krad (Si)
Latch up free	Up to 80 MeV-cm²/mg

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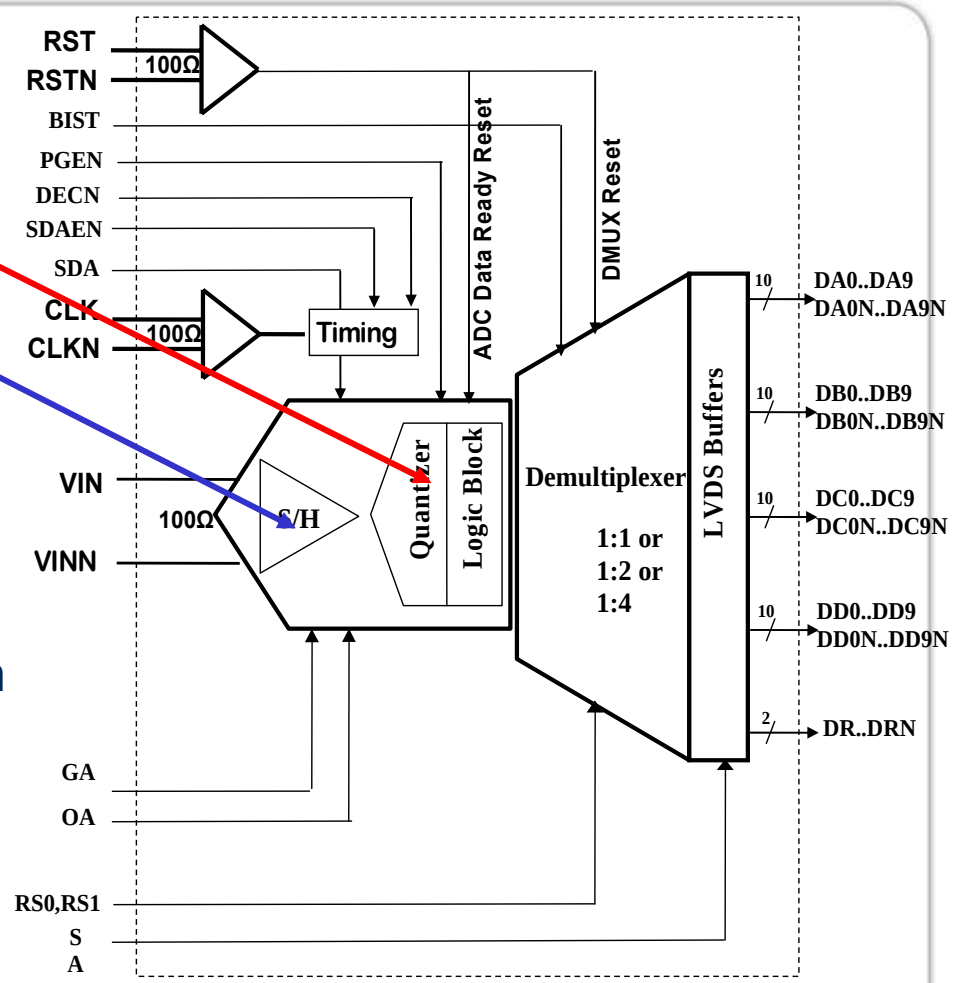
EV10AS180 *ADC 10-bit 1.5Gsps Die in B7HF200*
Architecture overview
Folding/interpolation
Low latency

- Broadband ADC Architecture based on:
  - **fast accurate** front-end Track & Hold,
  - followed by **fast settling Core** ADC featuring DC accuracy & low latency
- T/H front-end, a critical part of ADC
  - it needs to feature the requested **HF linearity** and **noise** characteristics
  - determines ADC input bandwidth and band flatness
- Low Power comes from an innovative architecture and fine design optimization
- **All key points where e2v unique world-class design and system expertise in fast broadband accurate ADC's are major assets**



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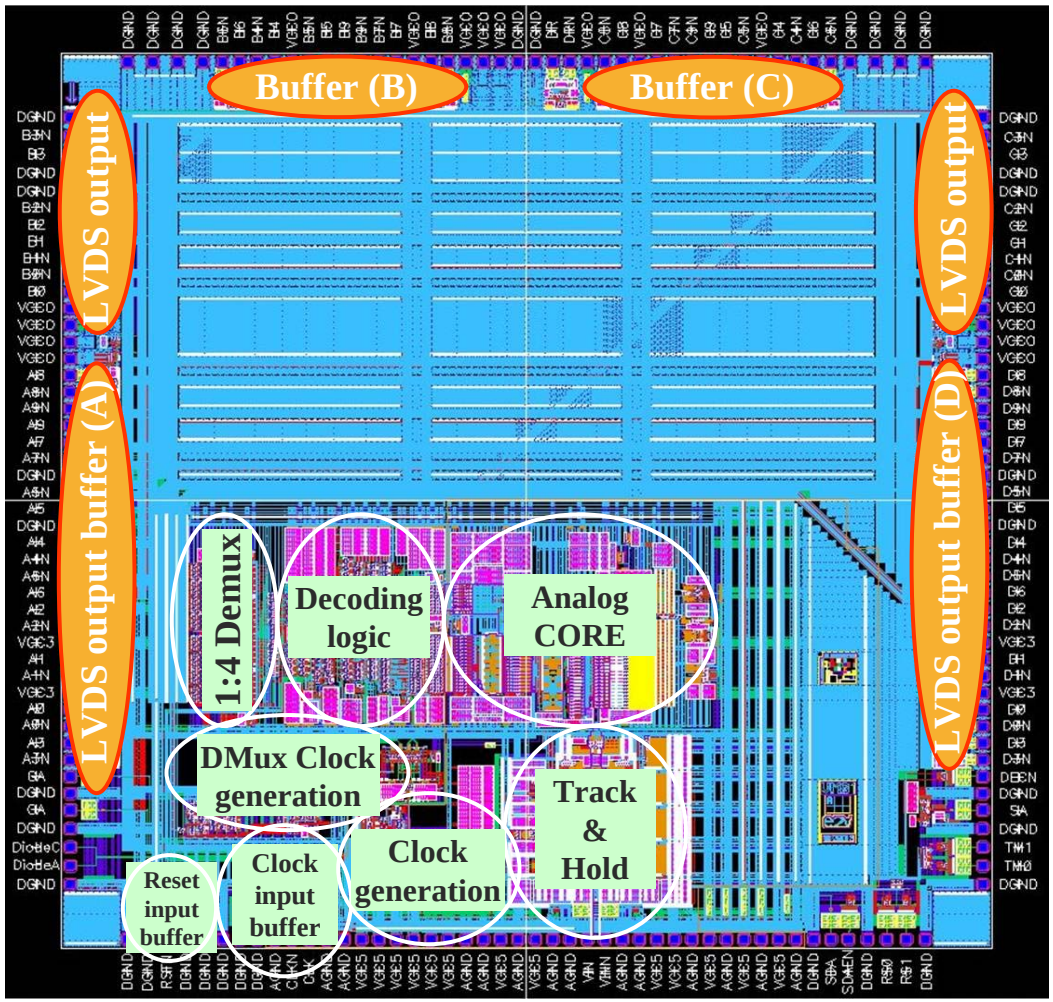
ADC 10-bit 1.5Gsps Die in B7HF200
Die Top Layout



CI-CGA255 package
Overview

- Package for the ADC 10-bit 1.5GSps w/ DMUX 1:4
  - Baseline
    - Ceramic package CI-CGA (LGA 255 + Column interposer)
    - Size 21X21mm² / Pin count: 255 / Pitch 1.27 mm / 2 decks
    - **Optimized for ADC dynamic and thermal performances for Space applications**
  - Objectives:
    - Minimal and predictable impact of package on ADC performances
    - Size in accordance with end-users needs
    - Compliant with Space level requirements
- Package Modelling
  - model extraction of the ADC package accesses, in particular the most critical ones, analogue input, clock input, data outputs
- Thermal behaviour
  - ADC Layout division into elementary cells with estimated power consumption
  - Identification of the Hot Spots & critical temperature gradients, if any
  - Layout correction if necessary

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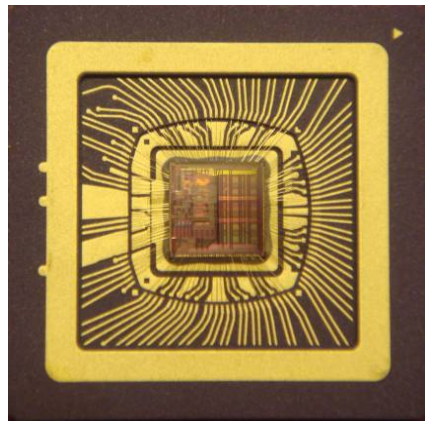
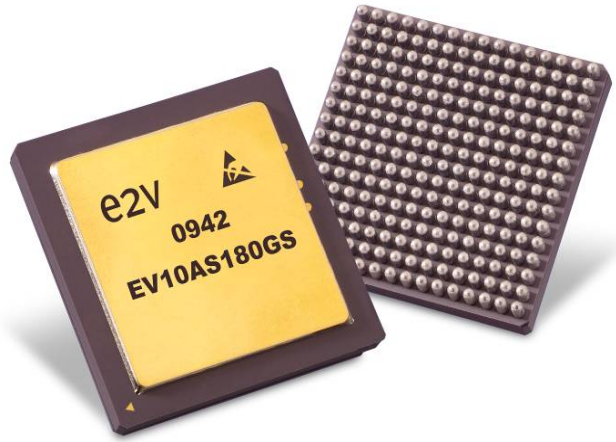
CI-CGA255 package
Status and achievements

- CI-CGA255 validated package
  - Electrical behaviour & modelling
  - Thermal behaviour
- Compatible with DAC





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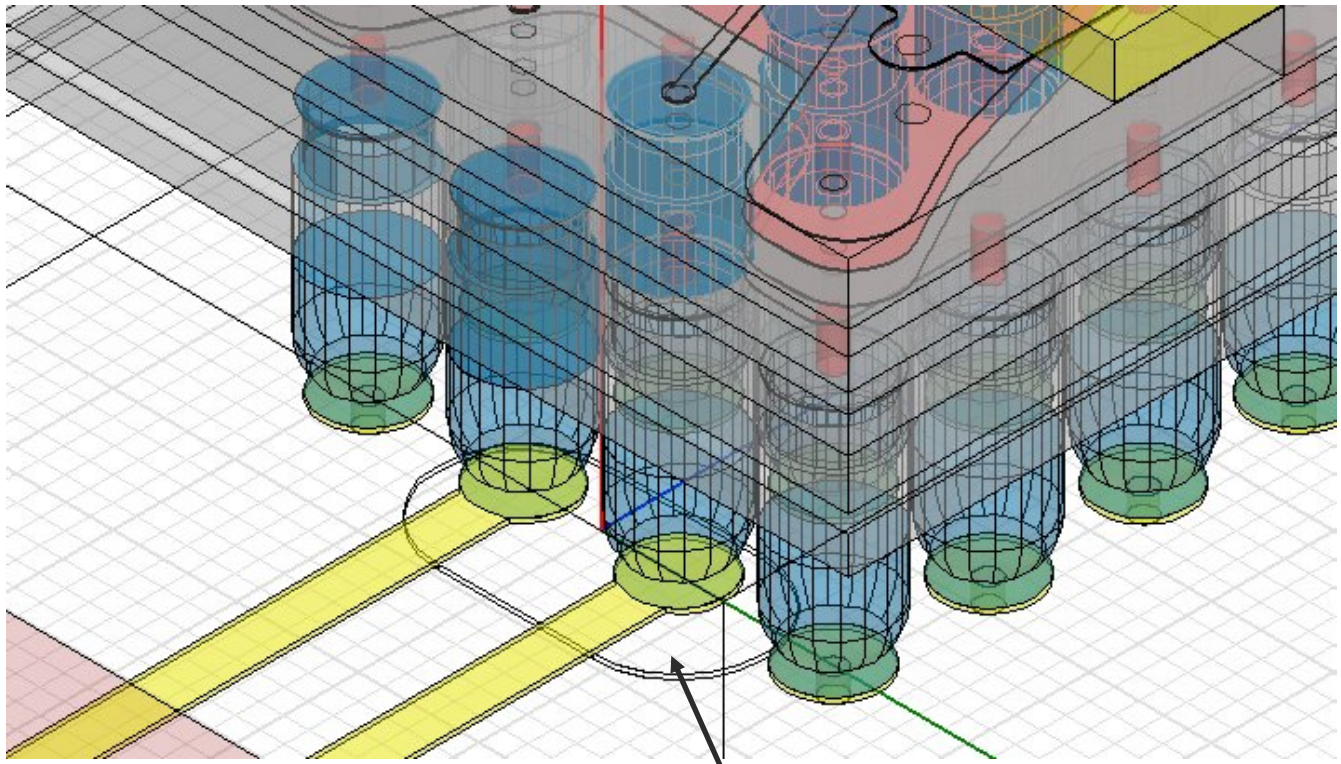
CI-CGA255 package
Package Electrical simulation for Analog Input using HFSS

- Simulation required huge resources : 630000 tetrahedrons, 16 Gbytes RAM + SWAP on hard disk.
- The most complex HFSS simulation ever made by e2v

Note: no solder mask)



100 Ohm Differential trace on board
1.27 mm pitch, 408 µm width x 40 µm thick
GND under 200 µm RO4003 Er = 3.38

Hole opening in GND plane from board to "remove" excess capacitance from lands 750 µm diameter.

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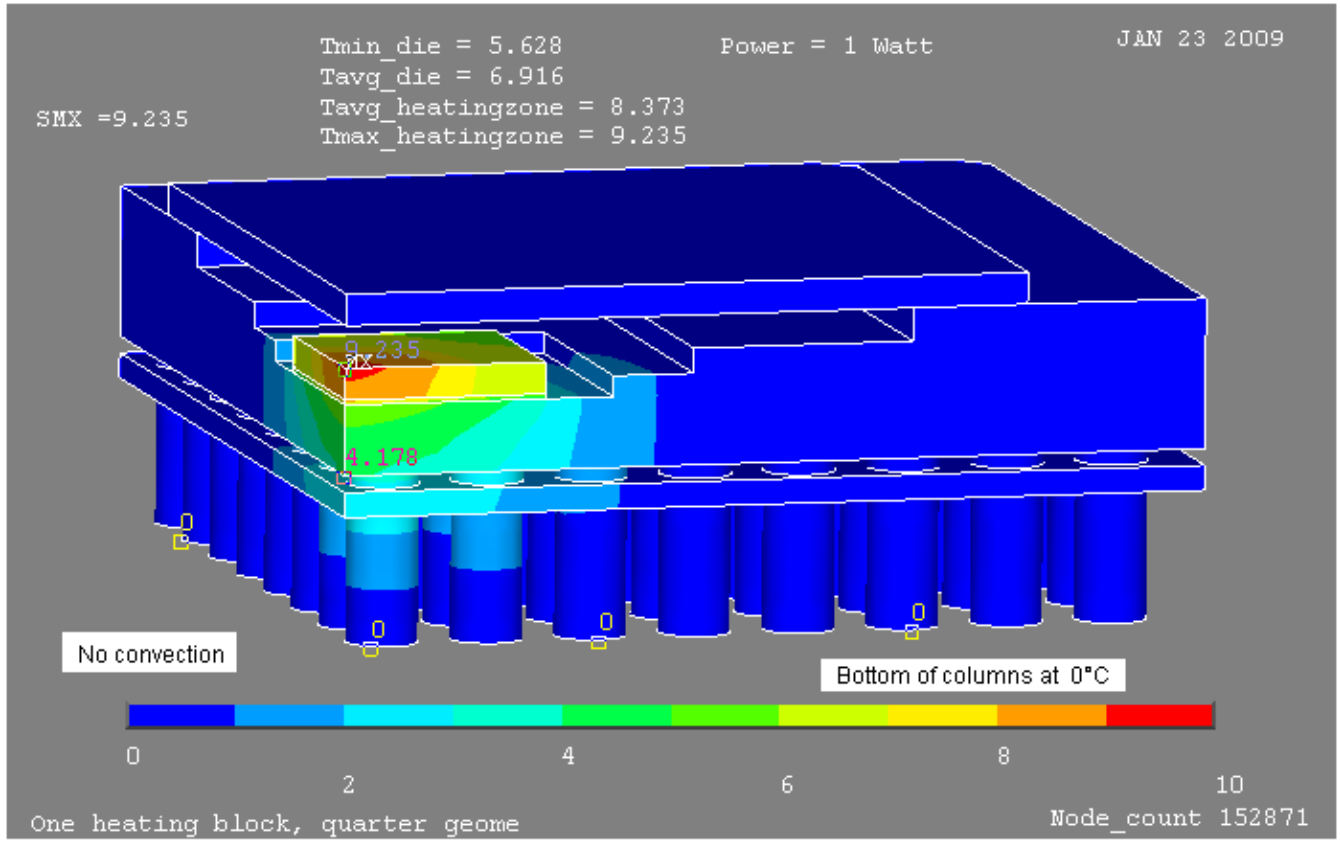
CI-CGA255 package
Package Thermal simulation

Thermal resistance junction to bottom_of_columns

= 9.2 °C/Watt

Solder Column Interposer from NTK



Die 4.88 x 4.88 mm2 380 µm
glue 60 µm 0.01 Watt/cm/K

heating zone = 2.44 x 2.44 mm2 (25% of die size)
1.0 Watt

RTH j-bottom-of-columns
Tref = 0°C

Body_thickness = 0.85 mm
Cavity_thickness = 0.25 mm
Deck1_thickness = 0.30 mm
Deck2_thickness = 0.40 mm

Body 21.0 mm SQ
Cavity 6.54 mm SQ
Deck1 8.50 mm SQ
Deck2 13.85 mm SQ

CI-CGA 255 16 x 16 matrix
1.27 mm pitch
SCI_column_height = 2.10 mm
Columns K = 0.40 W/cm/K

With 0.30 mm thin Ceramic of SCI
Lid 16.64 mm SQ, 0.38 mm thick

Al2O3 isotrope Kxx=Kyy=Kzz = 0.17 W/cm/K
No radiation, No convection
CPU time : 4 mn

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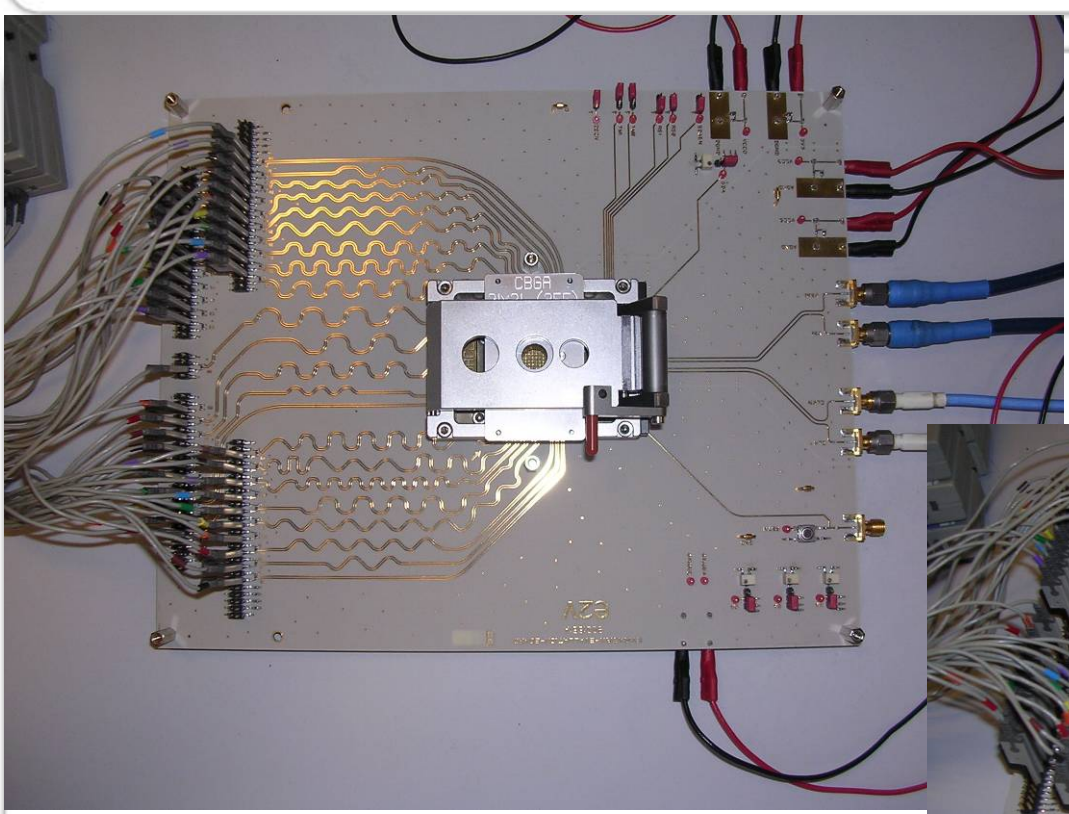
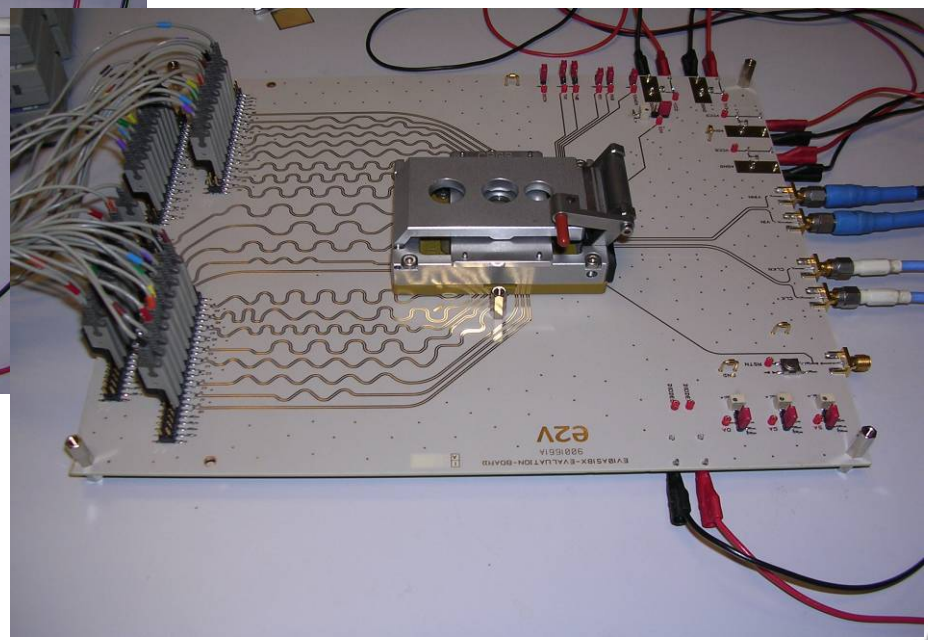
Evaluation Board
With dedicated socket





Project achievement summary

- Highlights of results obtained on first silicon (*detailed in next slides*)
  - First Silicon very close to final production Silicon
  - Performances very close to target
  - Package developed, validated and compliant with expectations
  - Preliminary Reliability tests performed prior to final design improvements satisfying
  - Total Dose 104Krad at 50rad/hour achieved
  - Heavy ion tests performed - no issue, in line with target specs

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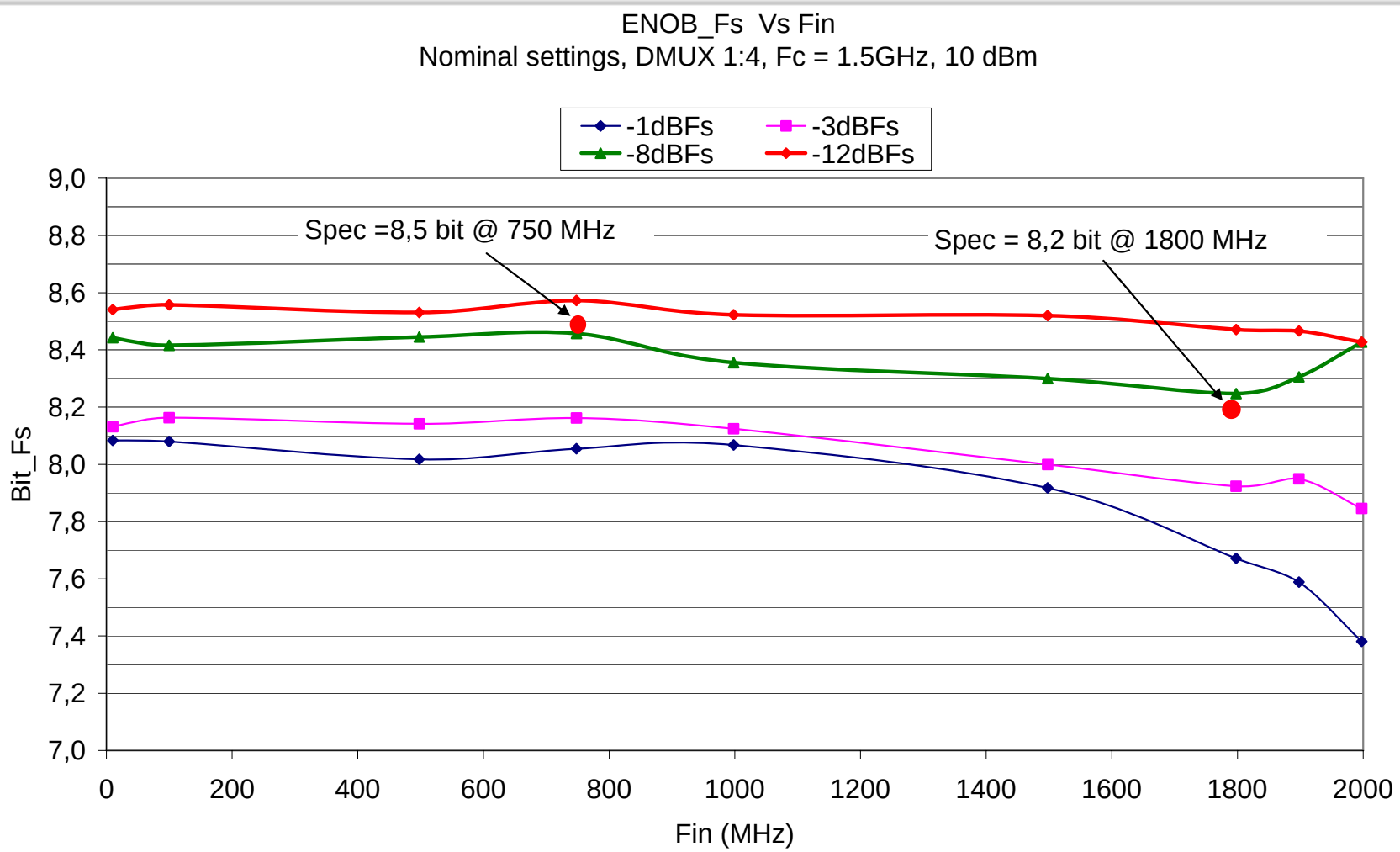
EV10AS180 *Performances obtained on first Silicon*
ENOB_FS
vs Fin, vs Ain (spec defined @ -12 dBFS)



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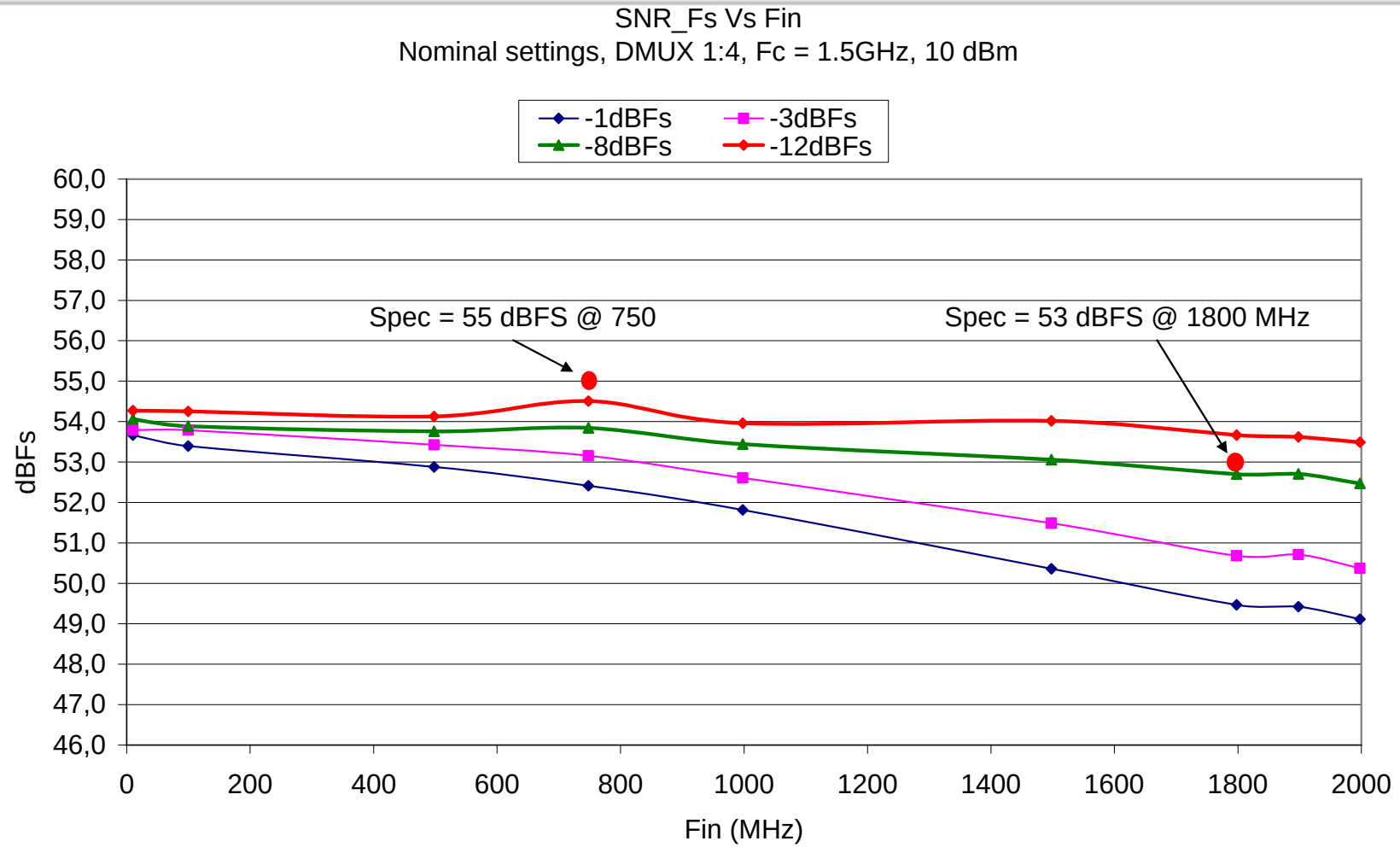
EV10AS180 *Performances obtained on first Silicon*
SNR_FS
vs Fin, vs Ain (spec defined @ -12 dBFS)



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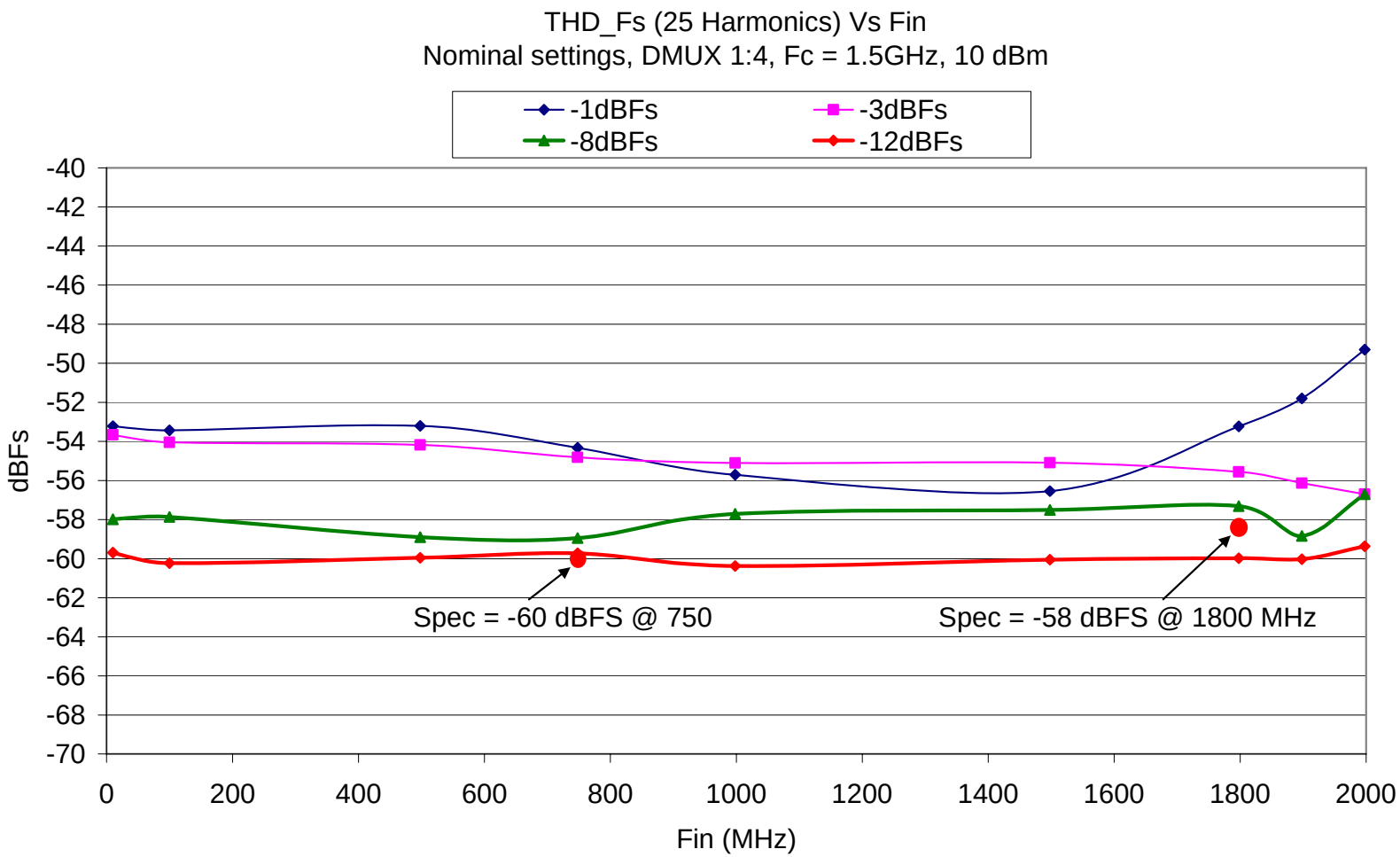
EV10AS180 *Performances obtained on first Silicon*
THD_FS (25 harmonics)
vs Fin, vs Ain (spec defined @ -12 dBFS)



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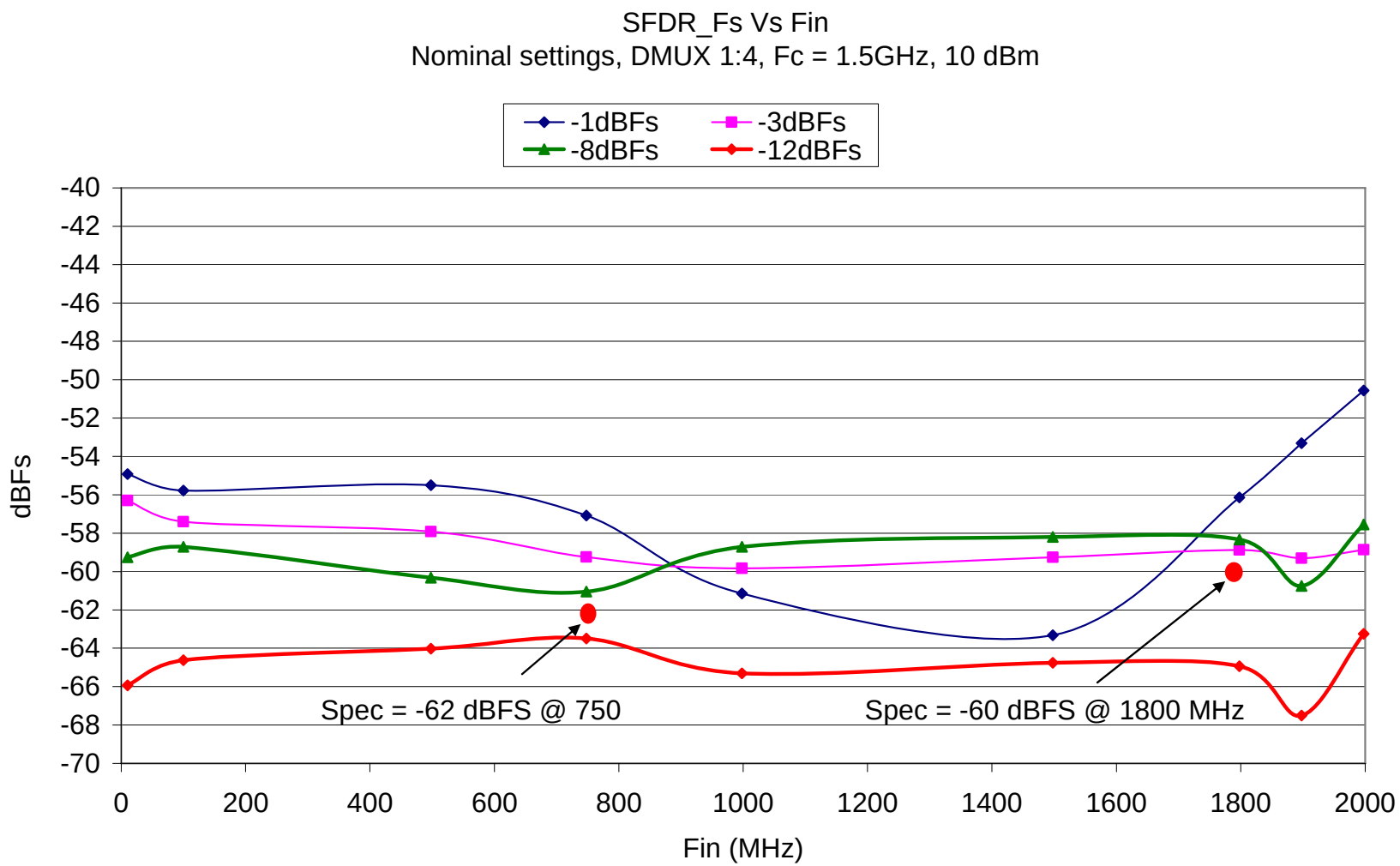
EV10AS180 *Performances obtained on first Silicon*
SFDR_FS
vs Fin, vs Ain (spec defined @ -12 dBFS)



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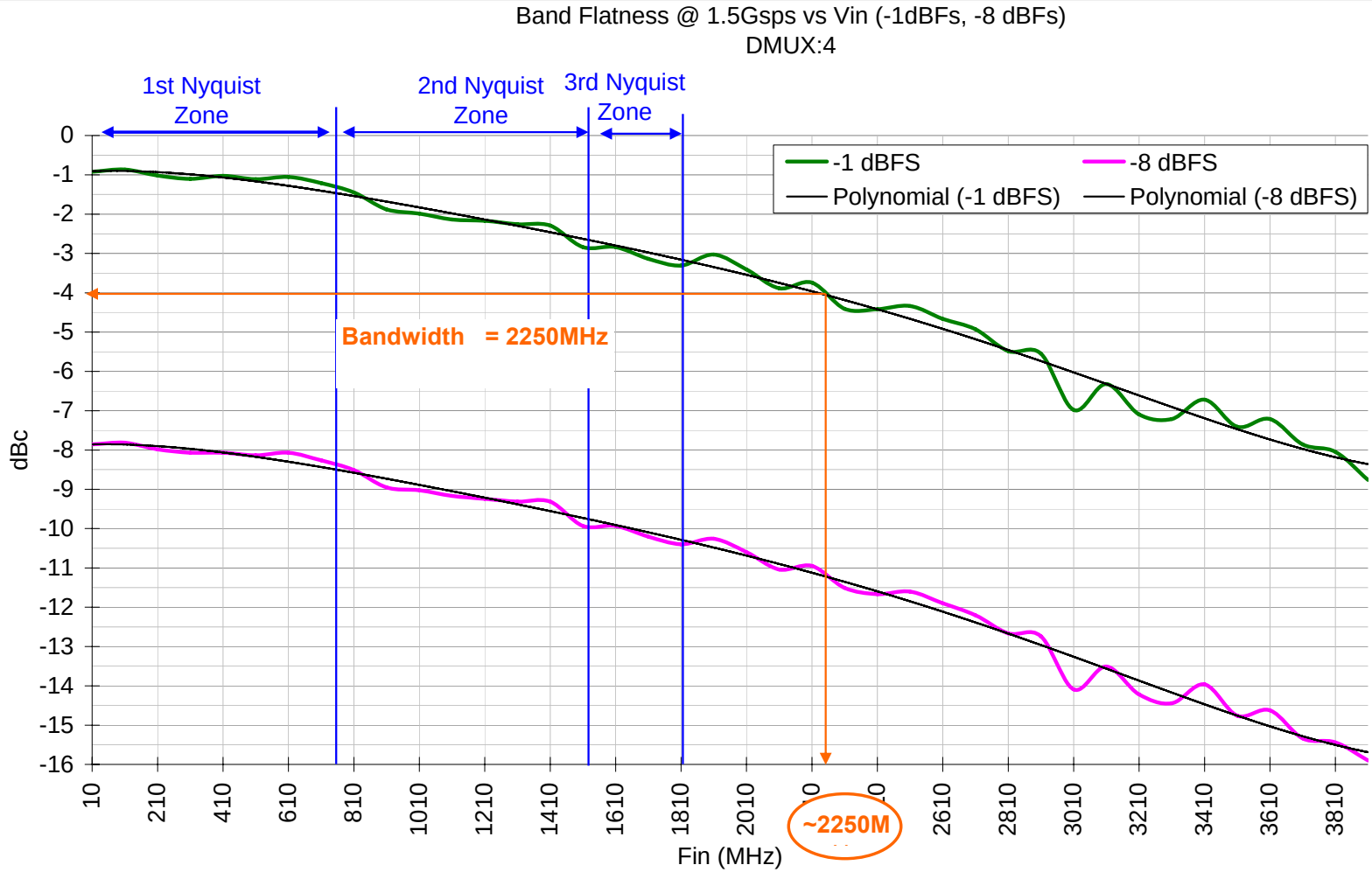
EV10AS180 *Performances obtained on first Silicon*
Bandwidth and band flatness



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EV10AS180 *Performances obtained on first Silicon*
NPR @ 1.5Gsps vs Nyquist zones

- Lab Test Conditions
  - Notch width = 500 KHz
  - Loading factor = -13 dBFS (optimum)
  - 1st Nyquist zone: notch centered on 50 MHz, 350 MHz, 657 MHz
  - 2nd Nyquist zone: notch centered on 800 MHz, 1100 MHz, 1407MHz
  - 3rd Nyquist zone: notch centered on 1550 MHz, 1850 MHz, 2157MHz

- Results:
  - In 1st Nyquist zone, measurements give an NPR figure of #44-45 dB (45 dB expected)
  - In 2nd Nyquist zone, correlation with SNR figure gives an NPR of #44 dB
  - In 3rd Nyquist zone, correlation with SNR figure gives an NPR of #43-44 dB (43 dB expected)

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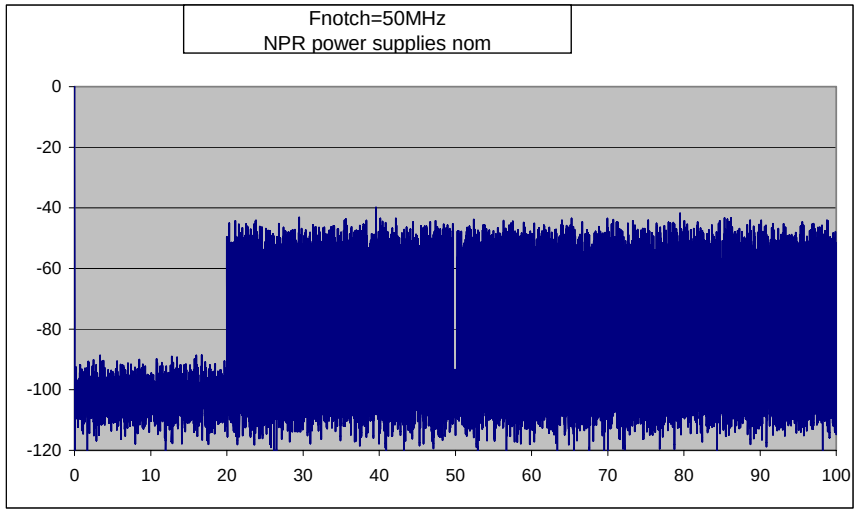
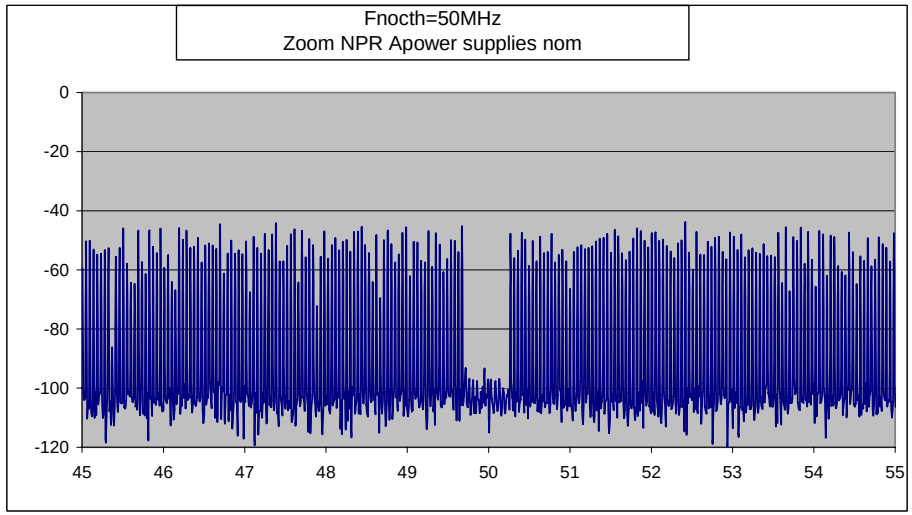
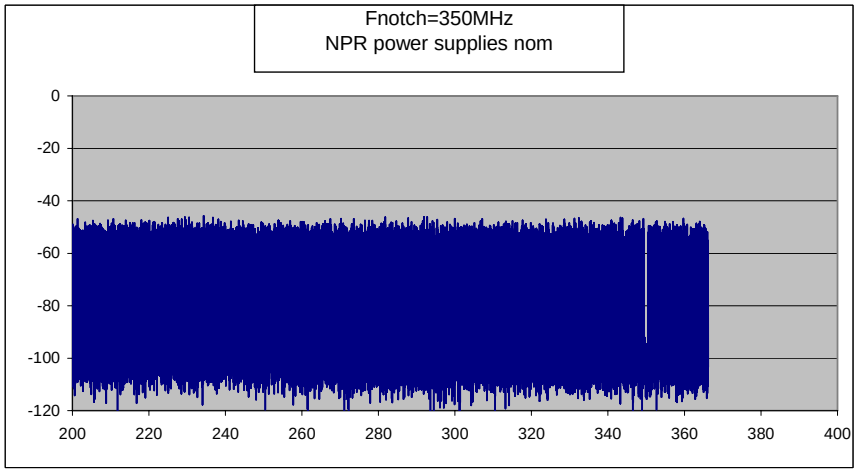
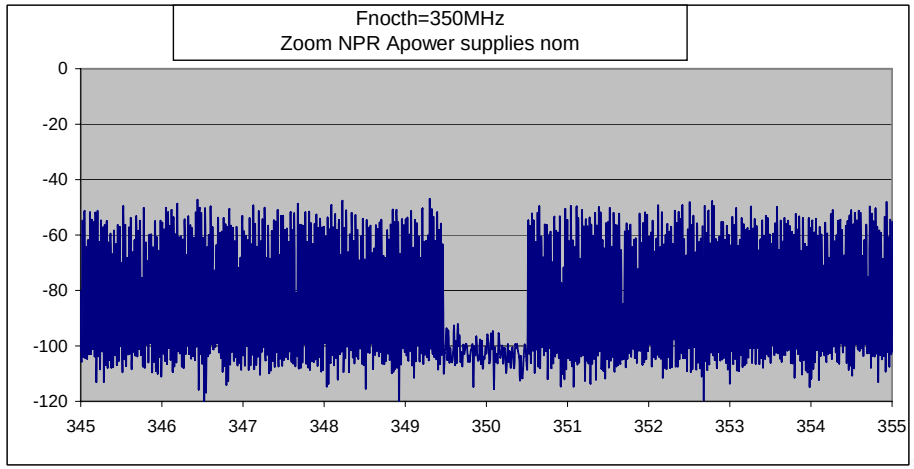
EV10AS180 *Performances obtained on first Silicon*
NPR in 1st Nyquist Zone









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ADC 10b/1.5GSps EV10AS180
Performances obtained on first Silicon
Summary

Parameter	Target Specification	Results (18 devices)
Dynamic performance @ -12 dBFS, Fs = 1.5G (nominal settings, 1:4 DMUX)		
THD Fin = 750 MHz Fin = 1800 MHz	 -60 dBFS -58 dBFS	 -58.2 dBFS -56.8 dBFS
SFDR Fin = 750 MHz Fin = 1800 MHz	 -62 dBFS -60 dBFS	 -62.3 dBFS -61.0 dBFS
SNR Fin = 750 MHz Fin = 1800 MHz	 55 dBFS 53 dBFS	 55.0 dBFS 54.1 dBFS
ENOB Fin = 750 MHz Fin = 1800 MHz	 8.5 bit_FS 8.2 bit_FS	 8.5 bit_FS 8.4 bit_FS
Power dissipation (*With performances in LBand)*	1.63 W (1:2 LVDS)	1.7 W (1:2 LVDS)

Some limitations on this first silicon have nevertheless been observed:

- Sensitivity vs temperature
- DMUX functionality limitation over clock range

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Preliminary Reliability Evaluation
Results Matrix

Test *Method*	**Test Conditions**	**Objective**	**Check**	**Sample**	***CA/CR = 0/1***
Construction analysis *ESCC 21400*	*B7HF200 ESA ADC*	-	B7HF200 specifications	6 Dice	**Pass**
Bond pull test *MIL-STD-883 TM.2011*	D	100% wires > 3 g	Measurements + IV	2 devices	**Pass: 0/1**
Stud pull test *MIL-STD-883 TM.2027*	-	> 0.2 Kg / mm²	Measurements + IV	2 devices	**Pass : 0/1**
Internal Water Vapor Content Test *MIL STD-883 TM-1018*	100°C	< 5000 ppm	Measurements	3 devices 2 devices	**Pass: 0/1**
Dimensional check	-	Outline specification	RVSI prog.	100%	**0/1**
Operating Life Test *MIL-STD-883 TM1005*	*ESA ADC B7HF200* 1000 Hrs / Tj 125°C (step 500Hrs)	1000Hrs	Characterisation program Room temp.	6 to 9 devices	**Pass 1000h (16 devices)**
LATCH UP *Jedec 78*	*ESA ADC B7HF200* Class 1 - room temp. Class 2 – Tj 125°C	6 parts ok Class 2	Characterisation program Room temp.	12 devices	**Pass: 0/1**
Temperature cycling ***JESD22-A104C***	*Cond. C A/A* *-65°C to 150°C*	500 cycles	Characterisation program Room temp.	5 devices	**Pass: 0/1**
ESD HBM *MIL-STD-883 TM3015* ---------- **ESD HBM** *JESD22-A114E*	ESA ADC B7HF200	3 parts stressed ok HBM level	Characterisation program Room temp.	3 devices	**Pass 1kV one access 750V**

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EV10AS180 *Preliminary Radiation Evaluation*
TID and Heavy Ions

- These tests were performed in order to have an initial evaluation of the architecture and process selected for the project, in anticipation to the ESCC evaluation.

- Total Dose (low dose rate 50rad/hour – performed at ESTEC)
  - Intermediate test at 30Krad
  - Final test at 100Krad
  - Test after annealing 24h
  - Test after annealing 168h

- Heavy ion Tests (16-hour tests, performed at Jyvaskyla)
  - Dynamic test (@ 600Msps)
  - Static test (@ 100Msps and 600Msps)

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EV10AS180 *Preliminary Radiation Evaluation* Results

Parameter	Symbol	Min	Typ	Max	Results	Unit
Radiation total dose	TID	100			**104**	Krad
Latch up free	SEL	80			**84 (at 115°C)**	MeV-cm²/mg
SEE performance (geosynchronous orbit)	SEE		1E-03 to 1E-02		**6.8 1E-03 to 1.7E-05**	SEU/device.day
SEFI (Single event Functional Interrupt) - Recoverable with Reset	SEFI	100 years			**No SEFI**	MTBF
Permanent conversion errors - Recoverable with Reset		100 years			**No permanent error Only self recovering error**	MTBF
Multi conversion errors (self recovering)		1 year			**1.2E-03/device.day (> 2.2 years)**	MTBF
Single conversion errors (self recovering)		1 day			**Max 6.8^{E}-03 (ie 147 days)**	MTBF

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10b/1.5GSps ADC EV10AS180 *Next Steps*
Scope, Objectives, Schedule

- Schedule of 10b/1.5GSps ADC EV10AS180
  - Samples version#1 available now
  - Final improvements of the ADC 10-bit 1.5Gsps Q2/2010
  - Beta Silicon in Q4 2010
    - Samples will be available for early application prototyping
  - Evaluation and qualification in Q1 2011
  - Production (Space level) in Q3 2011

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Conclusions

- EV10AS180 An unprecedented 10-bit 1.5GSps ADC has been developed by e2v with the support of ESA
  - Working in L-Band
  - Featuring Low power
  - And Integrated DMUX 1:2 1:4
  - With Early Radiation tolerance and reliability evaluated
- On time Project with regards to agreed TRP Schedule
- First prototypes show very good dynamic performances
- COMETS project (FP7) will allow to perform the necessary design improvements in order to make this 10-bit ADC the qualified product expected by the SPACE industry
- Then, last step will be to make this technical success be a commercial success…

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Thank you for your attention

Questions?

veronique.rozan@e2v.com
jean-philippe.amblard@e2v.com

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