High Resolution DAC for Space Applications

Microelectronics Presentation Days 2010
Integrated Systems Development
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Product highlights

- **Features**
  - Architecture: multi-bit $\Sigma\Delta$ modulator
  - Output stage: differential current steering
  - Digital input interface: Synchronous serial data format
  - Bandwidth: $0.1\text{mHz} – 1\text{kHz}$
  - Sampling frequency: selectable $6\text{kHz}$ or $12\text{kHz}$
  - Oversampling ratio: selectable x256 or x128
  - Configuration via $I^2C$ interface
  - 1.2V digital power supply
  - 3.3V analog power supply
  - Radiation hardened design

- **Applications**
  - High accuracy instrumentation and actuator drive for systems operating in space
## Target Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENOB</td>
<td>22 bit at 1kHz</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>130 dB (0.1mHz - 1kHz)</td>
</tr>
<tr>
<td>SNR</td>
<td>130 dB (0.1mHz - 1kHz)</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>&lt; 70mW</td>
</tr>
<tr>
<td>Temperature range (functional)</td>
<td>-55°C &lt; T &lt; 125°C</td>
</tr>
<tr>
<td>Temperature range (full-performance)</td>
<td>0°C &lt; T &lt; 50°C</td>
</tr>
<tr>
<td>TID tolerance</td>
<td>≥ 100 krad</td>
</tr>
<tr>
<td>LET for SEL immunity</td>
<td>≥ 70 MeV /mg/cm²</td>
</tr>
<tr>
<td>SEU immunity</td>
<td>Protection of critical memory cells</td>
</tr>
</tbody>
</table>
System Overview

Integrated Systems Development S.A.

Input interface

I²C interface

Clock Distribution network

DFT

Interpolation stage

3rd order ΣΔ modulator

DWA

Level Shifters (1.2 - 3.3V)

DAC 1 (Main)

Reference block

DAC 2 (Redundant)

SDIN
SCLK
SYNC
SDA
SCL
MCLK
Test signals

1.2V

DAC24BISDA

3.3V

OUTP1
OUTM1
Ref. Voltage
OUTP2
OUTM2
Architecture: Digital Part

Input interface

Clock Distribution network

Interpolator

IRP1 → IRP2 → IRP3 → SINC

I²C Registers bank

DFT block

3rd order ΣΔ Modulator

DWA

Digital to Analog interface block (Level Shifters)

1.2V

MCLK

SDIN
SCLK
SYNC

SDA
SCL

Test signals

Write
Read

DATA [31:0]

DATAp1 [31:0]
DATAm1 [31:0]
CLK1
PDN_ANA

DATAp2 [31:0]
DATAm2 [31:0]
CLK2
Multistage Interpolator

- **Purpose**
  - Increase the sampling rate → OSR selectable via I2C either x 128 or x 256
  - Filter unwanted spectral replicas → suppresses all signals over 3kHz to less than -136dB
- Multistage architecture leads to reduced computational complexity
- FIR filters exhibit linear phase and symmetric coefficients → minimal distortion of the input waveform
- Programmable SINC filter for OSR selection

<table>
<thead>
<tr>
<th>Filter type</th>
<th>Upsampling factor</th>
<th>Fs</th>
<th>Pass-band frequency</th>
<th>Stop-band frequency</th>
<th>Pass-band ripple</th>
<th>Stop-band attenuation</th>
<th>Filter order</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIR equiripple</td>
<td>2</td>
<td>12 kHz</td>
<td>1.01 kHz</td>
<td>3 kHz</td>
<td>0.0001 dB</td>
<td>-130 dB</td>
<td>44</td>
</tr>
<tr>
<td>Half Band Filter</td>
<td>2</td>
<td>24 kHz</td>
<td>3 kHz</td>
<td>9 kHz</td>
<td>0.00001 dB</td>
<td>-130 dB</td>
<td>30</td>
</tr>
<tr>
<td>Half Band Filter</td>
<td>2</td>
<td>48 kHz</td>
<td>3 kHz</td>
<td>21 kHz</td>
<td>0.00001 dB</td>
<td>-130 dB</td>
<td>18</td>
</tr>
</tbody>
</table>
**ΣΔ Modulator – design**

- 3\(^{rd}\) order feed-forward ΣΔ modulator
- 5-bit quantizer
- Sampling frequency 6kHz when OSR X256 and 12kHz when OSR X128
- Ideal SNR 179dB (OSR X256) or 158dB (OSR X128)
- Noise Transfer Function (NTF) : \( H(z) = (1 - z^{-1})^3 \)
- Idle Tone avoidance by introduction of dither (d)
- Dither signal generation using a 35-bit LFSR → pseudo-random signal generation every \(2^{35}-1\) instances.

![Block diagram of 3rd order feed-forward ΣΔ modulator](image)

**Diagram:**

- \(x\) input signal
- \(z^{-1}\) delay elements
- \(+\) summing nodes
- \(-\) subtraction nodes
- \(H-1\) noise filter
- \(d\) dither signal
- \(e\) error signal
- \(v\) intermediate output
- \(u\) quantizer input
- \(y\) output signal

**Frequency response of 3rd order modulator for sinusoidal input of 750Hz**

![Frequency response graph](image)
Dynamic Element Matching (DEM)

The output element mismatch error is minimized by the use of a DEM algorithm.

Data Weighted Averaging (DWA) as an efficient DEM algorithm.

Algorithm's objective → achieve an equal use of elements in long-term by rotating the output elements (current sources) in a cyclic fashion.

DWA uses only one index, which is updated with the addition of the input every clock cycle.
**Architecture: Analog Part**

- Bandgap cell provides an accurate reference voltage (1.2V) with a low temperature coefficient.
- First order RC filter reduces any noise from the bandgap block.
- Low noise Op-Amp along with M1 and current setting resistor ($R_{\text{ref}}$ or $R_{\text{ext}}$) implements the reference current source for generating the reference current $I_{\text{ref}}$.
- $I_{\text{ref}}$ can be set by selecting the internal resistor $R_{\text{Ref}}$ or connecting an external resistor $R_{\text{ext}}$.
- Differential elementary current sources build around the regulated cascode topology.
- Use of PMOS transistors for lower flicker noise ($1/f$) and high linearity.
Radiation Hardening

- Radiation hardening techniques
  - TMR at architecture level for the digital blocks (FSMs and counters)
  - Use of robust design cells during synthesis of the digital core
  - Techniques at layout level

irp1_fsm_state_next <=
(irp1_fsm_state_next1 and irp1_fsm_state_next2)
or (irp1_fsm_state_next1 and
irp1_fsm_state_next3) or (irp1_fsm_state_next3
and irp1_fsm_state_next2);
## Layout

- **Deep N-Well isolation (NISO)**
  - Minimizes the digital feed-through to the sensitive analog nodes
  - Improves the latch-up immunity
- **Layout and polarization scheme (ST's rules)**
Testability-1

- **Digital Part**
  - Full scan set of patterns

- **Analog part.**
  - When in ANALOG test mode, the digital blocks are fully bypassed and the current sources can be controlled directly through the input pads (e.g. from an FPGA)
  - **Exhaustive test mode (BYPASS)**
    - Serial transmission of a known test pattern via the input interface
    - Only the serial to // block remains active
    - Same clock frequency as in the input data latching
  - **Constant value test mode**
    - Predefined constant values applied using the dedicated test pins TEST [2:0]
    - No need for external support or additional I²C configuration
Testability-2

Normal operating mode

Test mode

Test settings

<table>
<thead>
<tr>
<th>TEST[2:0] Pins</th>
<th>Operation/OUT [1,2]</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Normal</td>
</tr>
<tr>
<td>001</td>
<td>Level -1</td>
</tr>
<tr>
<td>010</td>
<td>Level -1/2</td>
</tr>
<tr>
<td>011</td>
<td>Level 0 (Lower half)</td>
</tr>
<tr>
<td>100</td>
<td>Level 0 (Upper half)</td>
</tr>
<tr>
<td>101</td>
<td>Level 1/2</td>
</tr>
<tr>
<td>110</td>
<td>Level 1</td>
</tr>
<tr>
<td>111</td>
<td>Level 0 (even &amp; odd)</td>
</tr>
</tbody>
</table>

Level 1 $\rightarrow$ 5.83mA ($I_{\text{max}}$)
Level 0 $\rightarrow$ 2.73mA ($I_{\text{com}}$)
Level -1 $\rightarrow$ 0mA ($I_{\text{min}}$)
Floorplan and fabrication

- **Technology**: ST-Microelectronics™ 0.13um HCMOS9-GP
- **Line name**: DAC24BISDA
- **Dimensions**: ~1840 x 1840 um
- **Total area**: 3.42mm²
- **No of I/O pads**: 43
- **Minimum pad-to-pad spacing**: 90um
Validation plan

- Currently in progress
- Functional and performance validation - characterization

**Static performance tests**
- INL, DNL
- Offset and gain errors
- Power consumption, PSRR

**Dynamic performance tests**
- THD+N
- SNR, ENOB
- Dynamic range

**Radiation sensitivity tests**
- SEE → SEU, SEL → Cf-252
- TID under bias → Co60
Validation board

System block diagram

- Modular architecture --> Motherboard + DUT daughterboard
- FPGA based design
- Memories
- UART and USART interfaces
- Dedicated power supplies for the DUT
- On-board ADC for performing the SEU tests.
**Preliminary validation results**

**Analog output differential ramp signal**

- **Measurement conditions:** \( \text{V}_\text{DIG}=1.2\ V, \ \text{VANA}=3.3\ V, \ \text{R}_{\text{ref}}=219\ \Omega, \ \text{R}_L=100\ \Omega, \ \text{Ta}=25^\circ\text{C} \)

- **VBGOUT = 1.2V**

- **Analog supply current normal mode:** \( I_A = 19.5\ mA \Rightarrow P_A(\text{normal}) = 64.4\ mW \)

  → It is possible to reduce the analog power consumption by using a higher external current setting resistor \( R_{\text{ext}} \).

- **Analog supply current analog power down mode:** \( I_A = 270\ \mu A \Rightarrow P_A(\text{pdn}) = 890\ \mu W \)

- **Maximum differential output current per DAC cell:** \( I_o(\text{max}) \approx 5.75\ mA \)

- **LSB step current (current steered by a single CS):** \( I_{CS} \approx 180\ \mu A \)

- **SNR \approx 120\ dB**

- **The device will be part of ST Microelectronics aerospace offer**