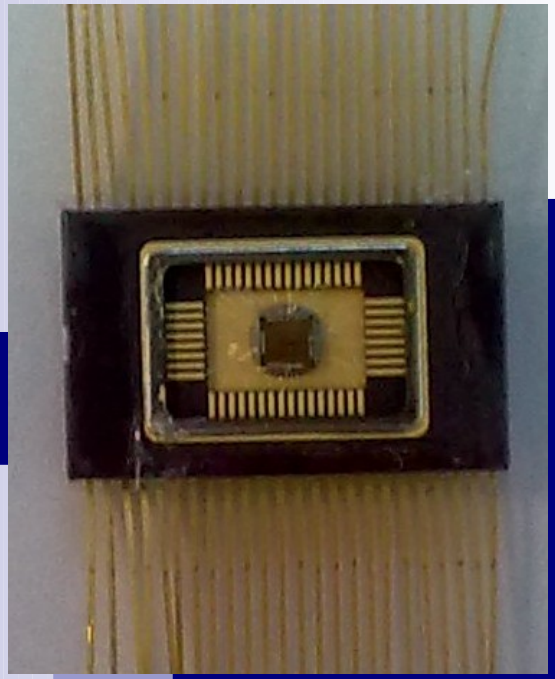


High Resolution DAC for Space Applications

Microelectronics Presentation Days 2010

Integrated Systems Development

30 March – 1 April 2010, ESA, ESTEC

ISD
Integrated Systems Development S.A.

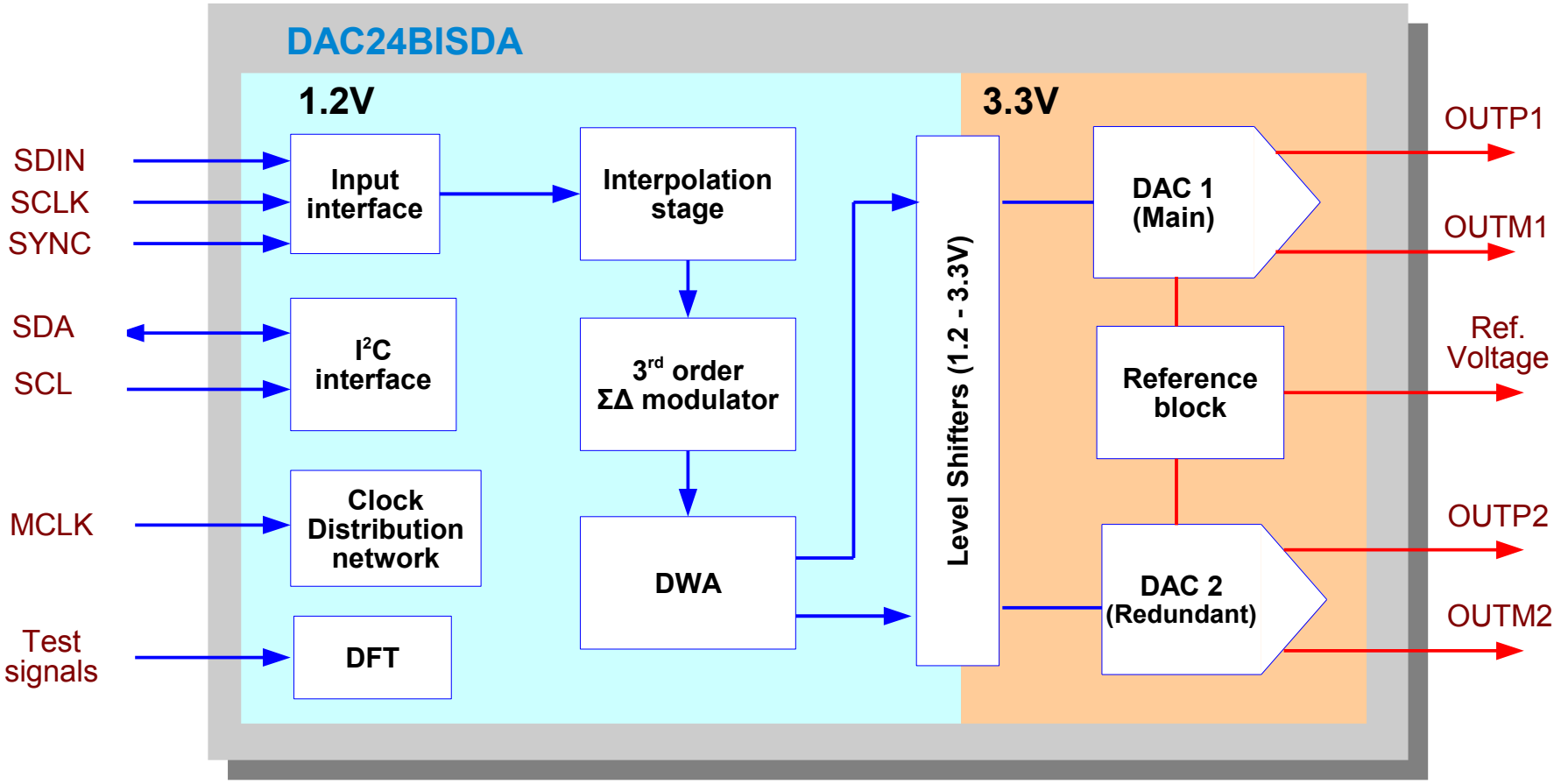
Product highlights

- **Features**
  - Architecture: multi-bit ΣΔ modulator
  - Output stage: differential current steering
  - Digital input interface: Synchronous serial data format
  - Bandwidth: 0.1mHz – 1kHz
  - Sampling frequency: selectable 6kHz or 12 kHz
  - Oversampling ratio: selectable x256 or x128
  - Configuration via I^2C interface
  - 1.2V digital power supply
  - 3.3V analog power supply
  - Radiation hardened design
- **Applications**
  - High accuracy instrumentation and actuator drive for systems operating in space

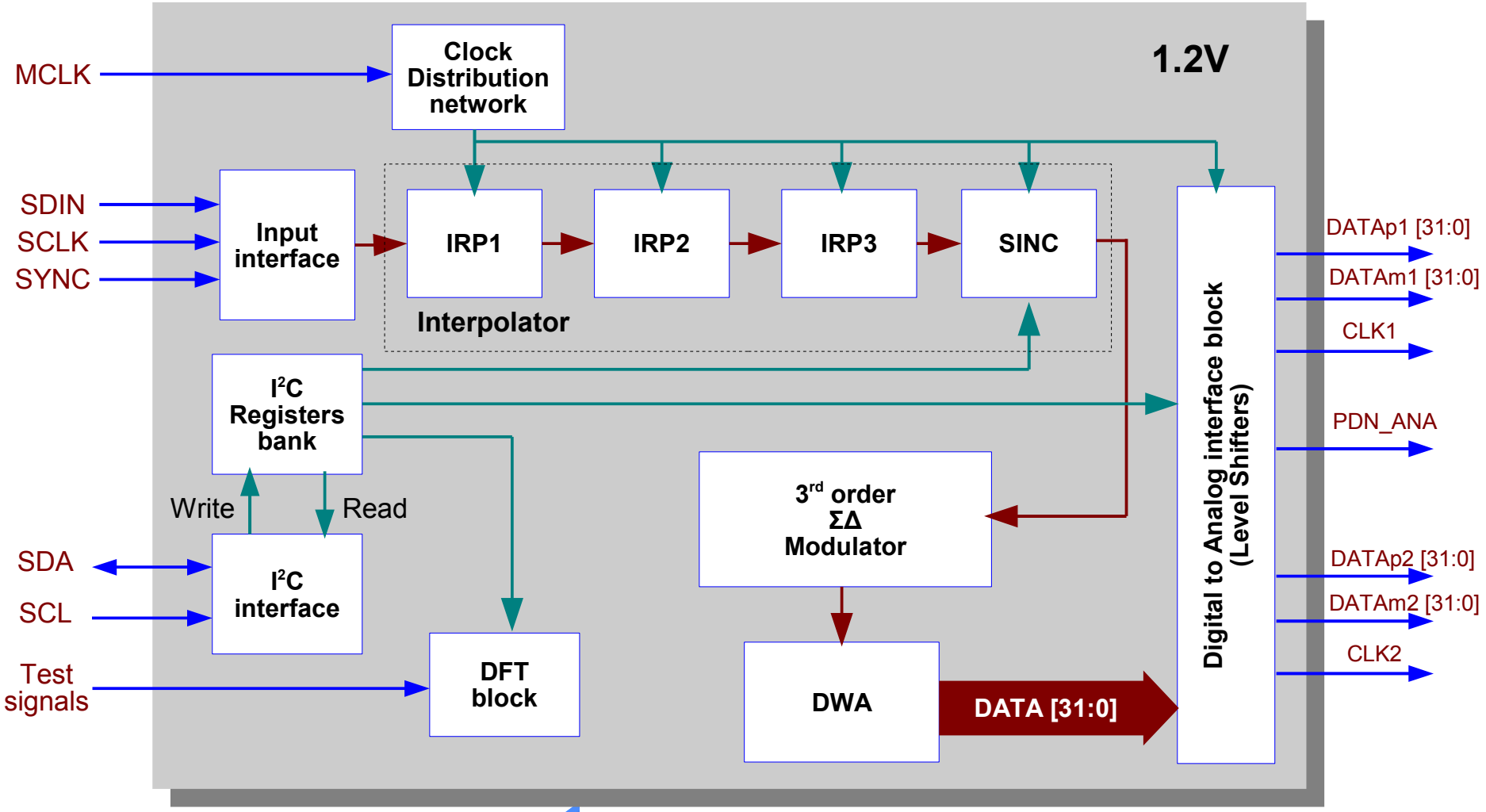
Target Performance

Parameter	Value
ENOB	22 bit at 1kHz
Dynamic range	130 dB (0.1mHz - 1kHz)
SNR	130 dB (0.1mHz - 1kHz)
Power dissipation	< 70mW
Temperature range (functional)	-55ºC < T < 125ºC
Temperature range (full-performance)	0ºC < T < 50ºC
TID tolerance	≥ 100 krad
LET for SEL immunity	≥ 70 MeV /mg/cm^2
SEU immunity	Protection of critical memory cells

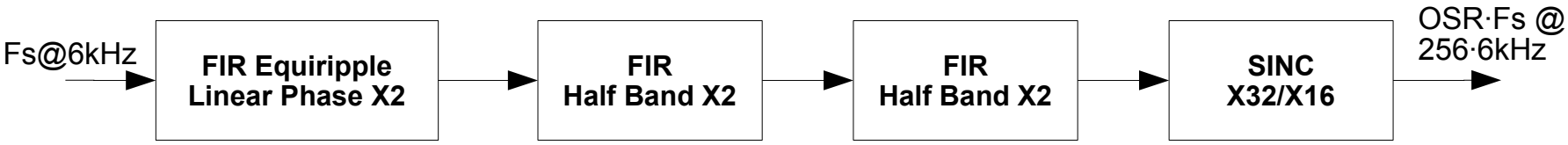
System Overview



Architecture: Digital Part



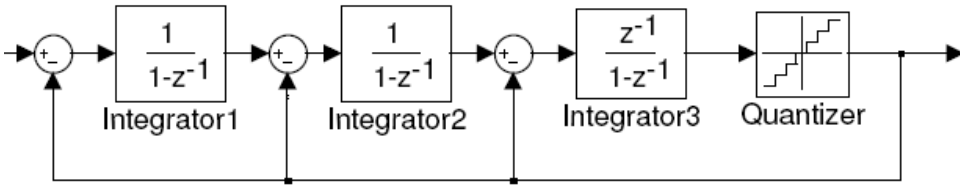
Multistage Interpolator

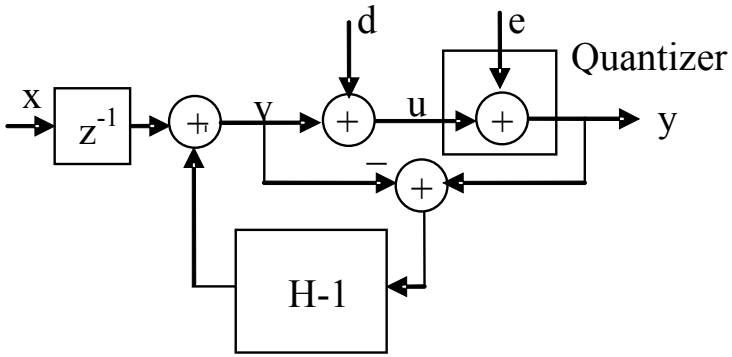


- **Purpose**
  - increase the sampling rate → OSR selectable via I2C either x 128 or x 256
  - Filter unwanted spectral replicas → suppresses all signals over 3kHz to less than -136dB
- Multistage architecture leads to reduced computational complexity
- FIR filters exhibit linear phase and symmetric coefficients → minimal distortion of the input waveform
- Programmable SINC filter for OSR selection

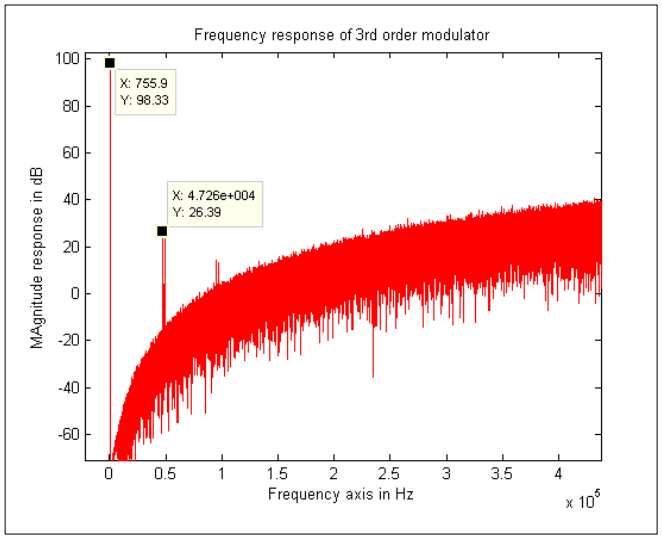
Filter type	Upsampling factor	Fs	Pass-band frequency	Stop-band frequency	Pass-band ripple	Stop-band attenuation	Filter order
FIR equiripple	2	12 kHz	1.01 kHz	3 kHz	0.0001 dB	-130 dB	44
Half Band Filter	2	24 kHz	3 kHz	9 kHz	0.00001 dB	-130 dB	30
Half Band Filter	2	48 kHz	3 kHz	21 kHz	0.00001 dB	-130 dB	18

ΣΔ Modulator – design





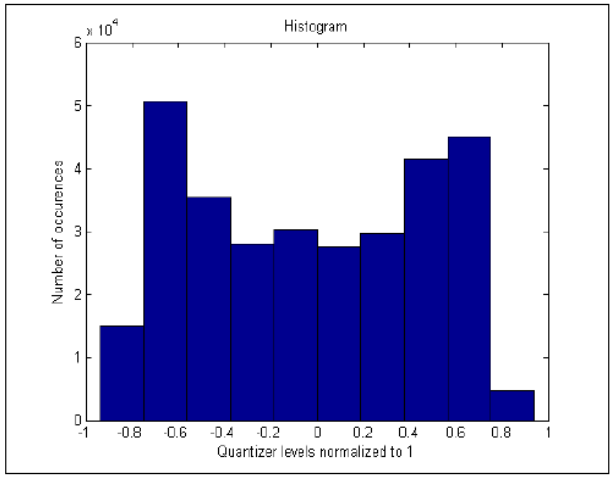
- 3rd order feed-forward ΣΔ modulator
- 5-bit quantizer
- Sampling frequency 6kHz when OSR X256 and 12kHz when OSR X128
- Ideal SNR 179dB (OSR X256) or 158dB (OSR X128)
- Noise Transfer Function (NTF) : $H(z) = (1- z^{-1})^3$
- Idle Tone avoidance by introduction of dither (d)
- Dither signal generation using a 35-bit LFSR → pseudo-random signal generation every 2^{35}-1 instances.



Frequency response of the modulator for sinusoidal input of 750Hz

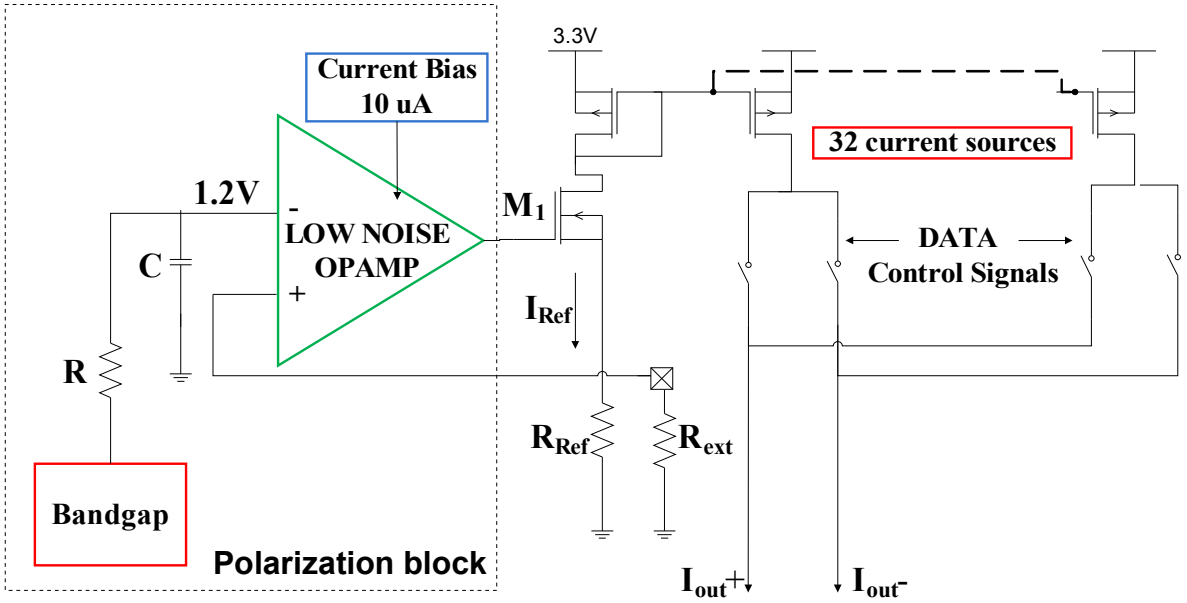
Dynamic Element Matching (DEM)

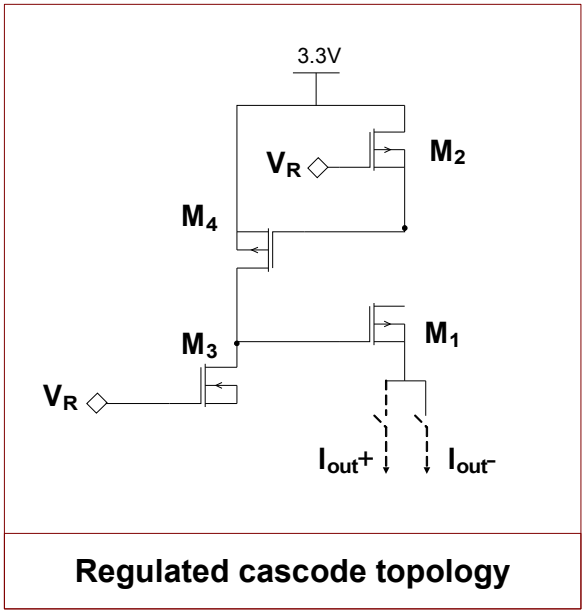
Time	Input	Index	1	2	3	4	5	6	7
1	3	1	■	■	■				
2	2	4				■	■		
3	5	6	■	■	■			■	■
4	6	4	■	■		■	■	■	■
5	2	3			■	■			
6	7	5	■	■	■	■	■	■	■



- The output element mismatch error is minimized by the use of a DEM algorithm.
- Data Weighted Averaging (DWA) as an efficient DEM algorithm.
- Algorithm's objective → achieve an equal use of elements in long-term by rotating the output elements (current sources) in a cyclic fashion.
- DWA uses only one index, which is updated with the addition of the input every clock cycle.

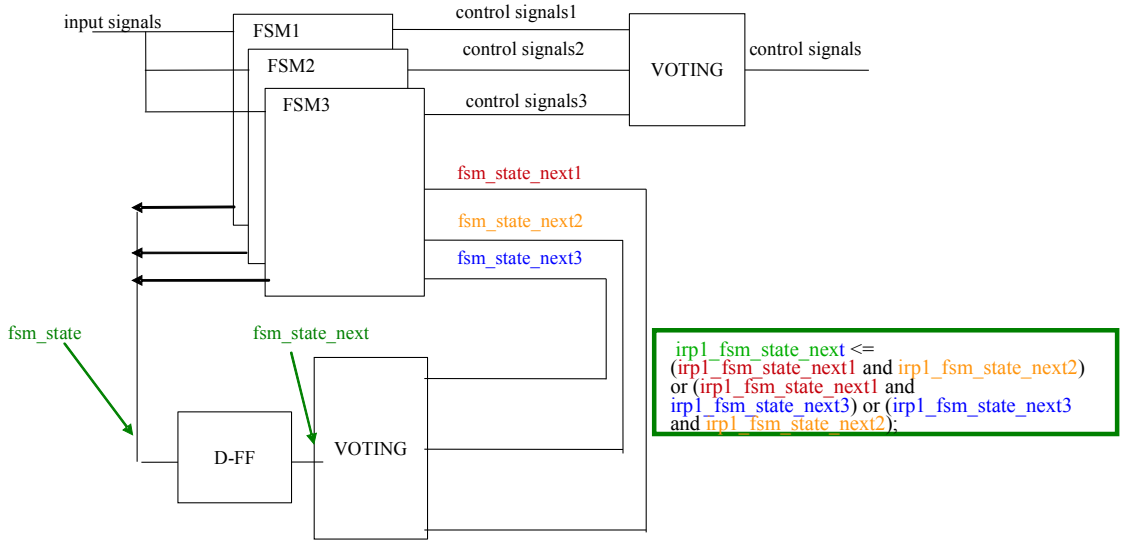
Architecture: Analog Part





- Bandgap cell provides an accurate reference voltage (1.2V) with a low temperature coefficient.
- First order RC filter reduces any noise from the bandgap block.
- Low noise Op-Amp along with M1 and current setting resistor (R_{ref} or R_{ext}) implements the reference current source for generating the reference current $I_{ref.}$
- I_{Ref} can be set by selecting the internal resistor R_{Ref} or connecting an external resistor $R_{ext.}$
- Differential elementary current sources build around the regulated cascode topology.
- Use of PMOS transistors for lower flicker noise(1/f) and high linearity.

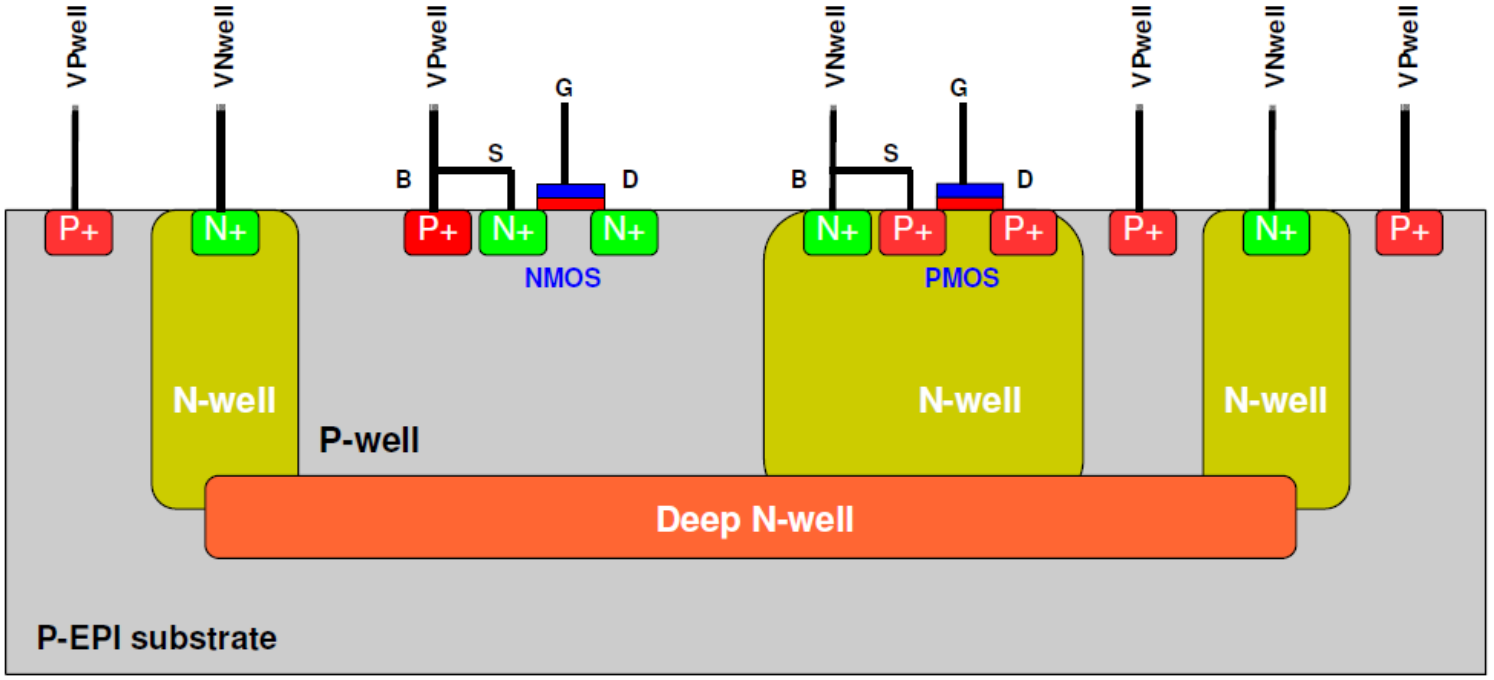
Radiation Hardening



- **Radiation hardening techniques**
  - TMR at architecture level for the digital blocks (FSMs and counters)
  - Use of robust design cells during synthesis of the digital core
  - Techniques at layout level

Layout

- **Deep N-Well isolation (NISO)**
  - Minimizes the digital feed-through to the sensitive analog nodes
  - Improves the latch-up immunity
- **Layout and polarization scheme (ST's rules)**

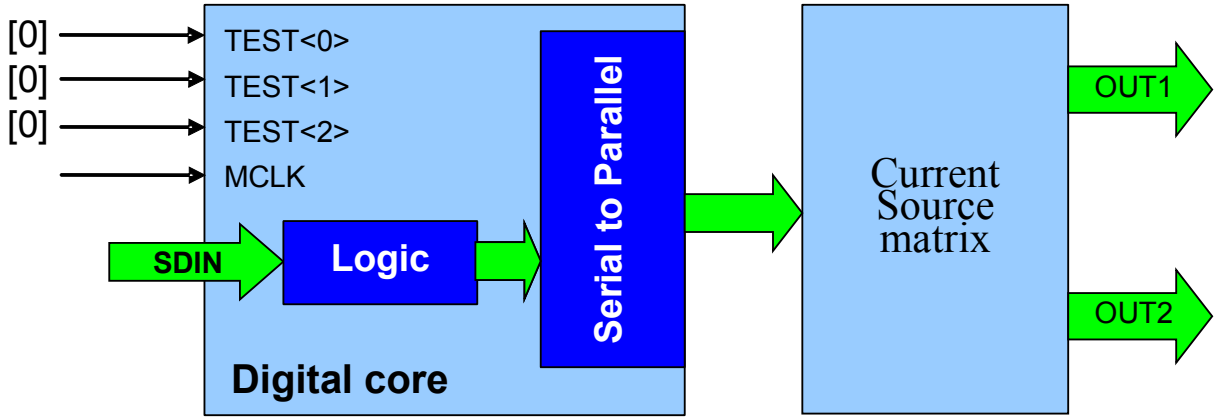


Testability-1

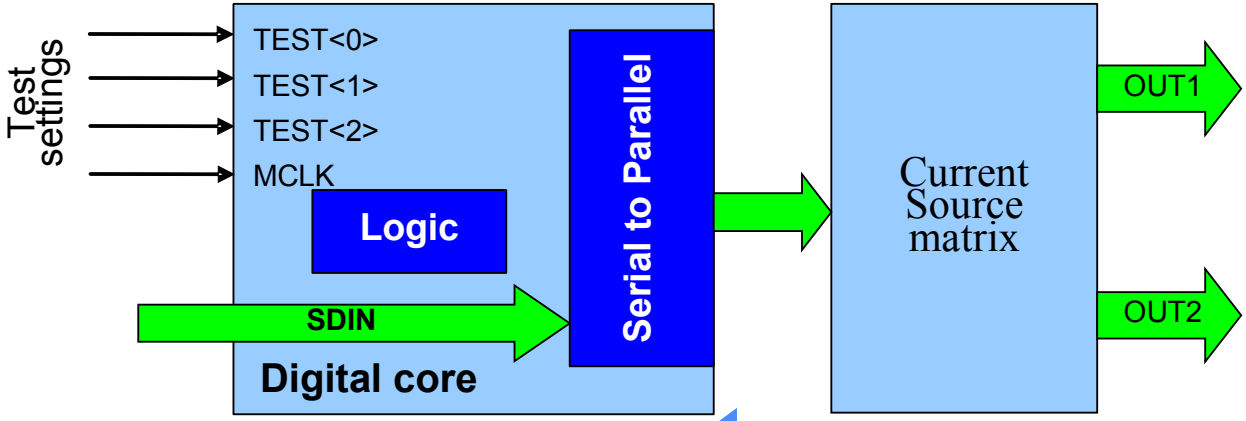
- **Digital Part**
  - Full scan set of patterns
- **Analog part**.
  - When in ANALOG test mode, the digital blocks are fully bypassed and the current sources can be controlled directly through the input pads (e.g. from an FPGA)
  - **Exhaustive test mode (BYPASS)**
    - Serial transmission of a known test pattern via the input interface
    - Only the serial to // block remains active
    - Same clock frequency as in the input data latching
  - **Constant value test mode**
    - Predefined constant values applied using the dedicated test pins TEST [2:0]
    - No need for external support or additional I^2C configuration

Testability-2

Normal operating mode



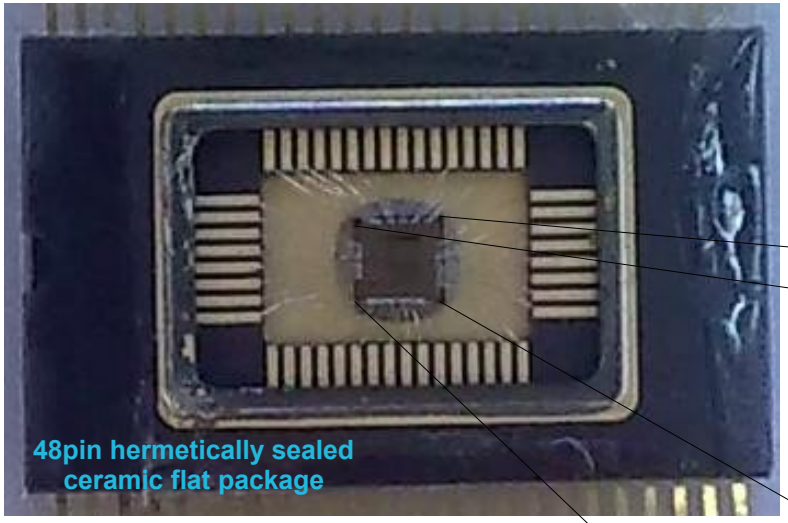
Test mode

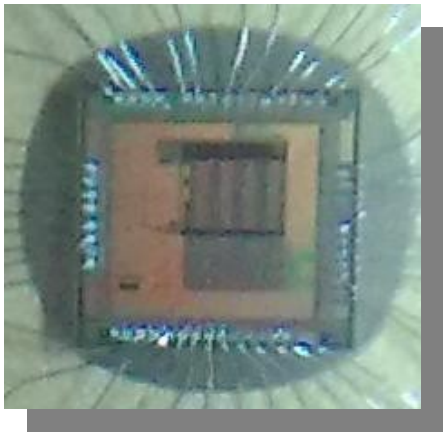


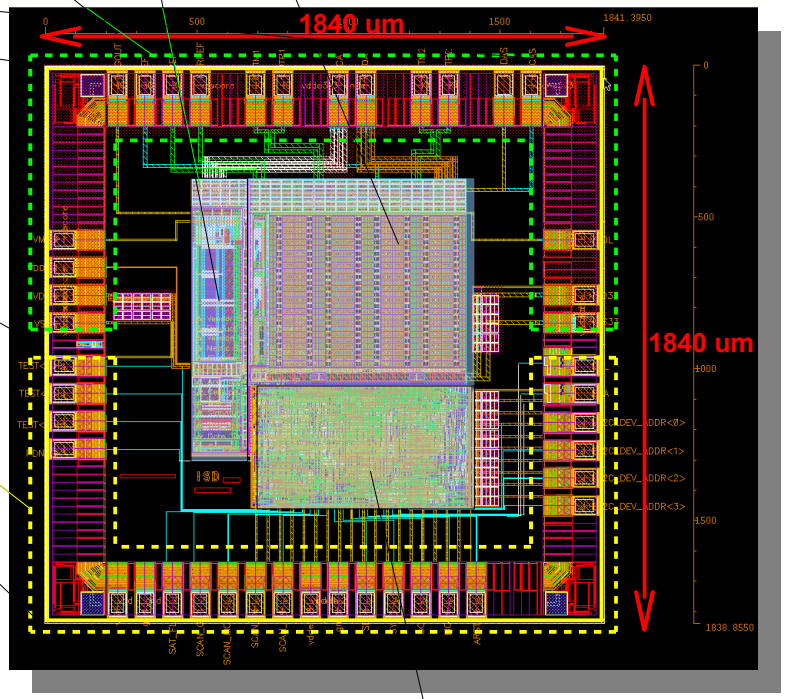
TEST[2:0] Pins	Operation/ OUT [1,2]
000	Normal
001	Level -1
010	Level -1/2
011	Level 0 (Lower half)
100	Level 0 (Upper half)
101	Level 1/2
110	Level 1
111	Level 0 (even & odd)

Level 1 → 5.83mA (Imax)
Level 0 → 2.73mA (Icom)
Level -1 → 0mA (Imin)

Floorplan and fabrication



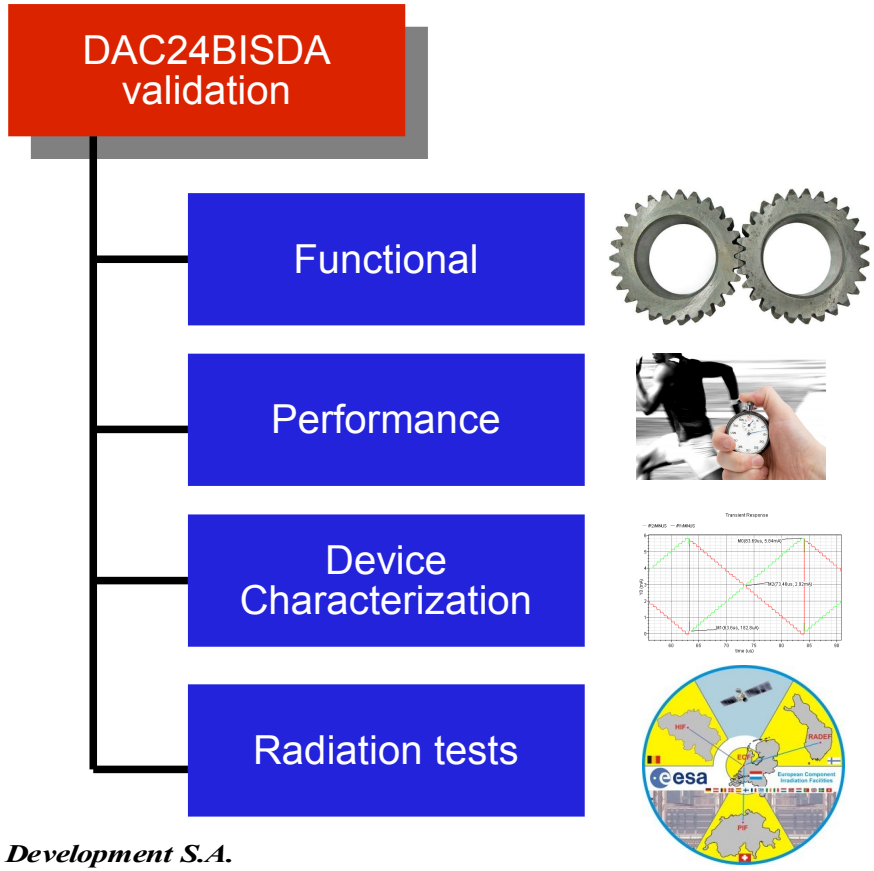




- **Technology**: ST-Microelectronics™ 0.13um HCMOS9-GP
- **Line name**: DAC24BISDA
- **Dimensions**: ~ 1840 x 1840 um
- **Total area**: 3.42mm^2
- **No of I/O pads**: 43
- **Minimum pad-to-pad spacing**: 90um

Validation plan

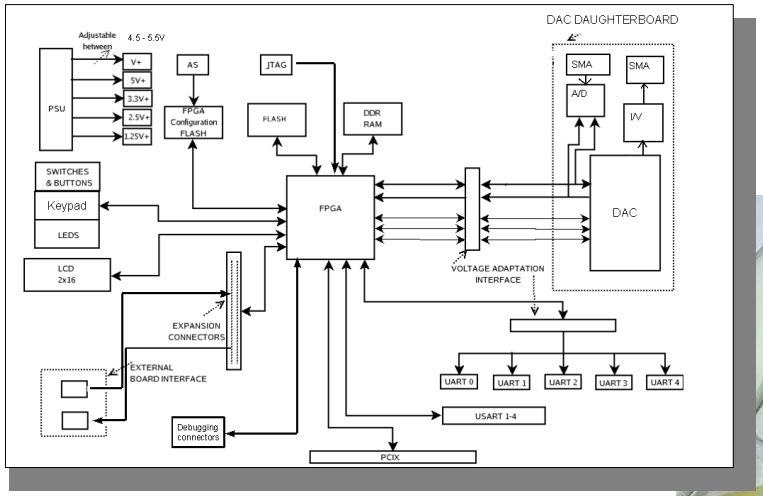
- → Currently in progress
- Functional and performance validation - charachterization
- **Static performance tests**
  - INL, DNL
  - Offset and gain errors
  - Power consumption, PSRR
- **Dynamic performance tests**
  - THD+N
  - SNR, ENOB
  - Dynamic range
- **Radiation sensitivity tests**
  - SEE → SEU, SEL → Cf-252
  - TID under bias → Co60

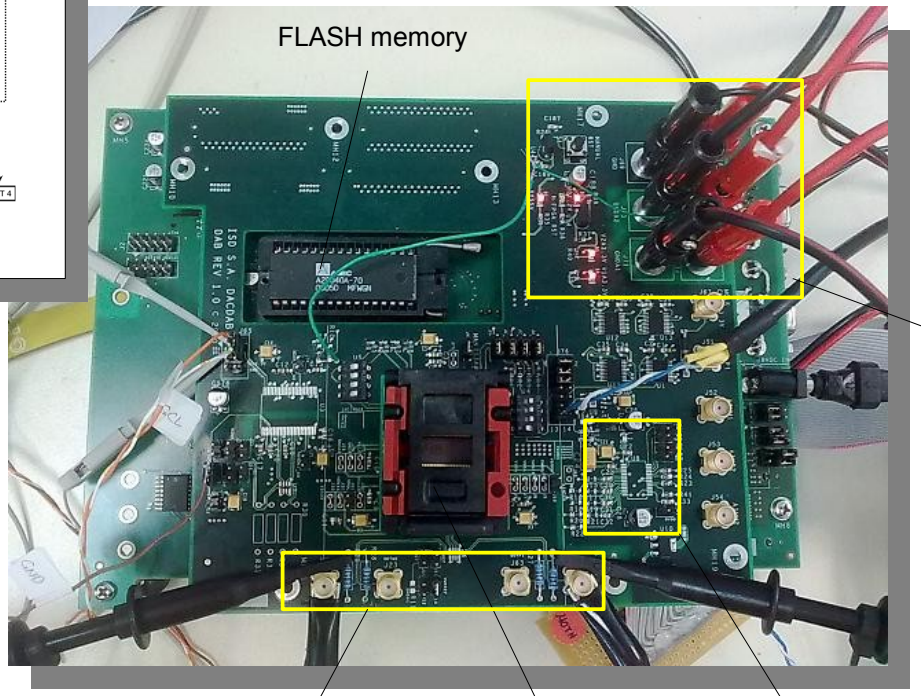


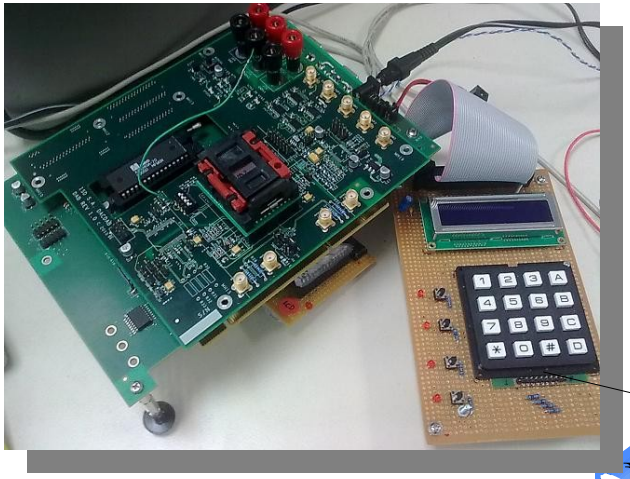
Validation board

- Modular architecture --> Motherboard + DUT daughterboard
- FPGA based design
- Memories
- UART and USART interfaces
- Dedicated power supplies for the DUT
- On-board ADC for performing the SEU tests.

System block diagram







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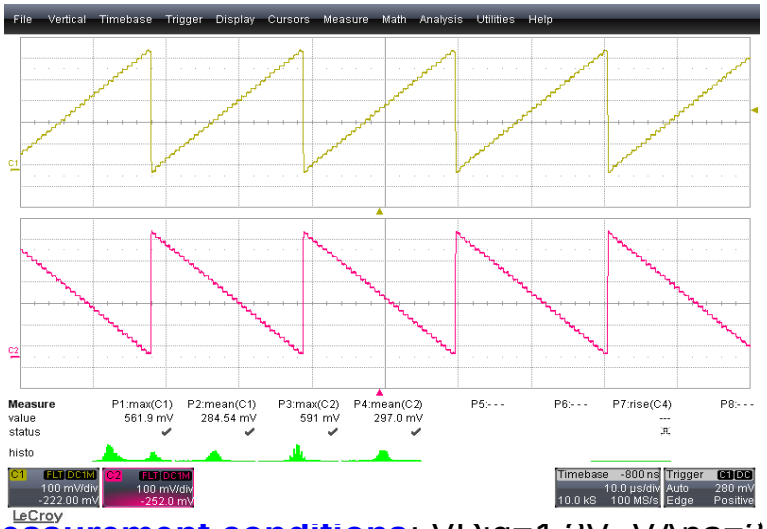
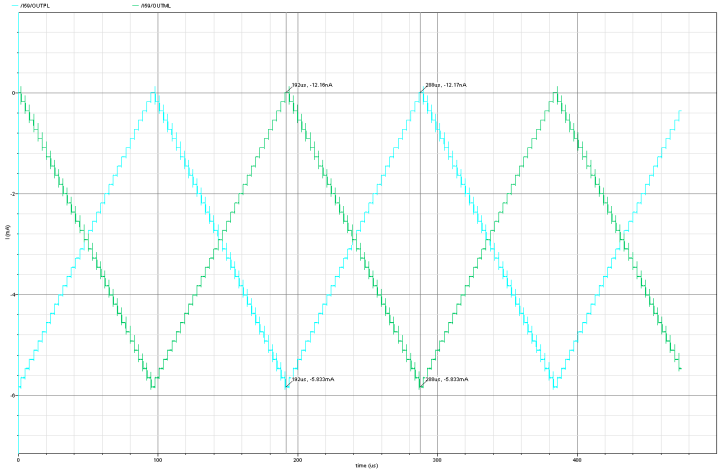
Preliminary validation results

Analog output differential ramp signal





- **Measurement conditions**: VDig=1.2V, VAna=3.3V, R_{ref}=219Ω, R_L = 100Ω, Ta=25ºC
- VBGOUT = 1.2V
- Analog supply current normal mode: I_A = 19.5mA => P_A(normal) = 64.4mW

→ It is possible to reduce the analog power consumption by using a higher external current setting resistor R_{ext}.

- Analog supply current analog power down mode: I_A = 270µA => P_A(pdn) = 890µW
- Maximum differential output current per DAC cell: I_o(max) ≈ 5.75mA
- LSB step current (current steered by a single CS): I_{CS} ≈ 180µA
- SNR ≈ 120 dB
- The device will be part of ST Microelectronics aerospace offer