High-Speed High-Resolution ADC with BISC

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Key Project Objectives

- New **high-speed high-resolution ADC technology** for communications, imaging, physics experiments and space applications

  - 1. High Linearity: Resolution of 13-bits
  - 2. High Speed: Sampling rate up to 80MS/s
  - 3. Low-Power: below 120mW
  - 4. Low-Cost: Standard 90nm CMOS manufacturing process from a pure-play foundry
  - 5. High Reliability: Robustness against space radiation effects

Project Partners

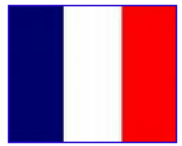
S3 Portugal
Prime Contractor
ADC, BISC Design,
Prototype Implementation
Silicon Testing

Testing Support,
Lab Equipment

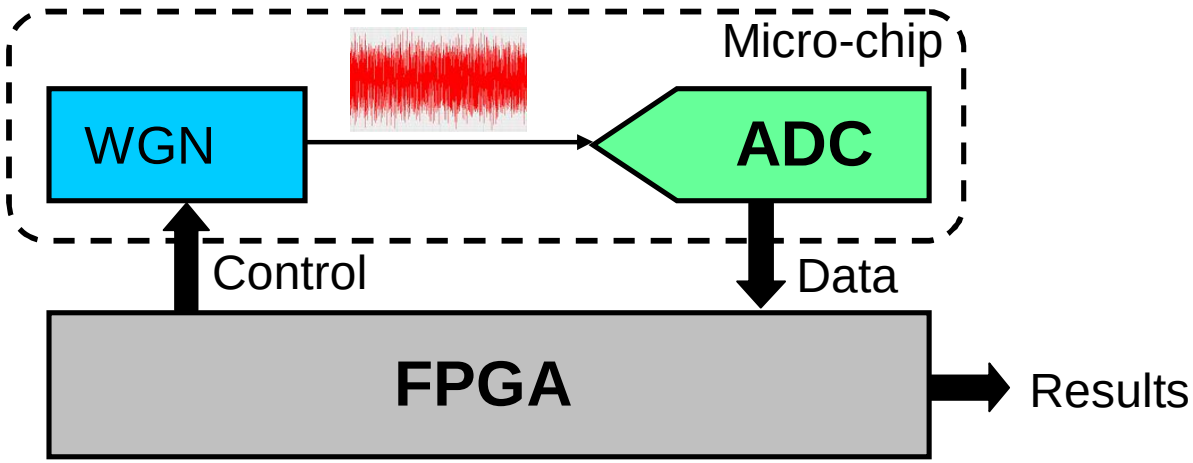
Digital BISC, FPGA

Chip Fabrication via TSMC

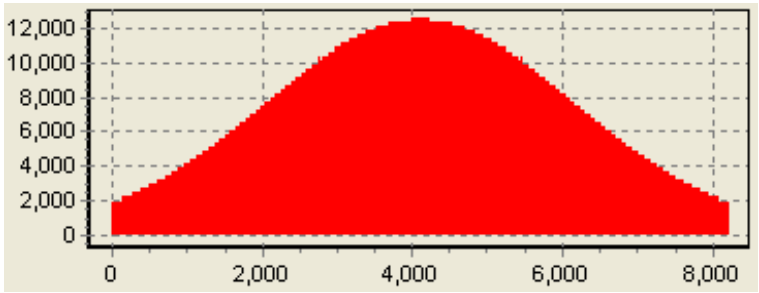
Radiation Tests



Histogram-based BISC Algorithm

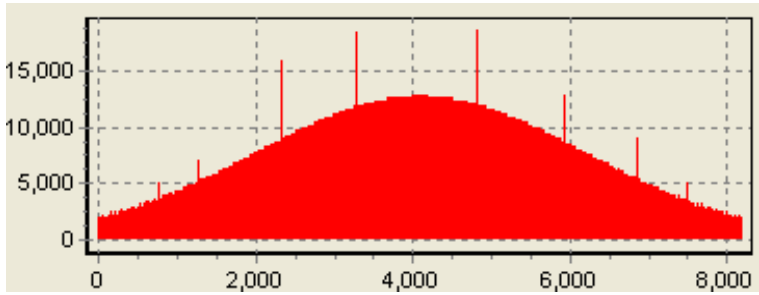


Ideal Histogram



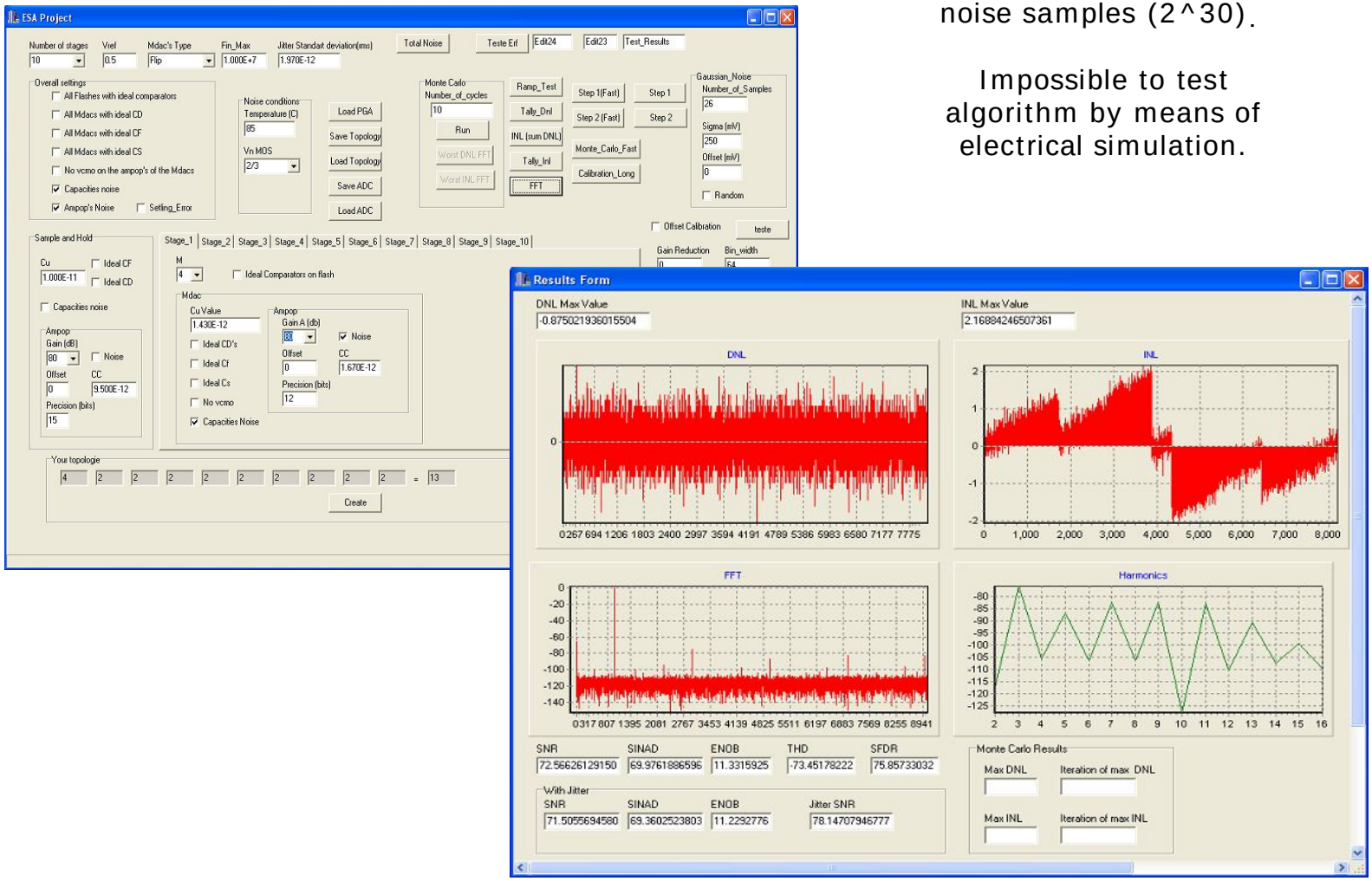
Real Histogram

(Including ADC non-linearities)



- Measuring the histogram spikes we are able to calculate its deviations from the ideal histogram and calculate the Calibration Codes.

ADC and BISC Modulation Software

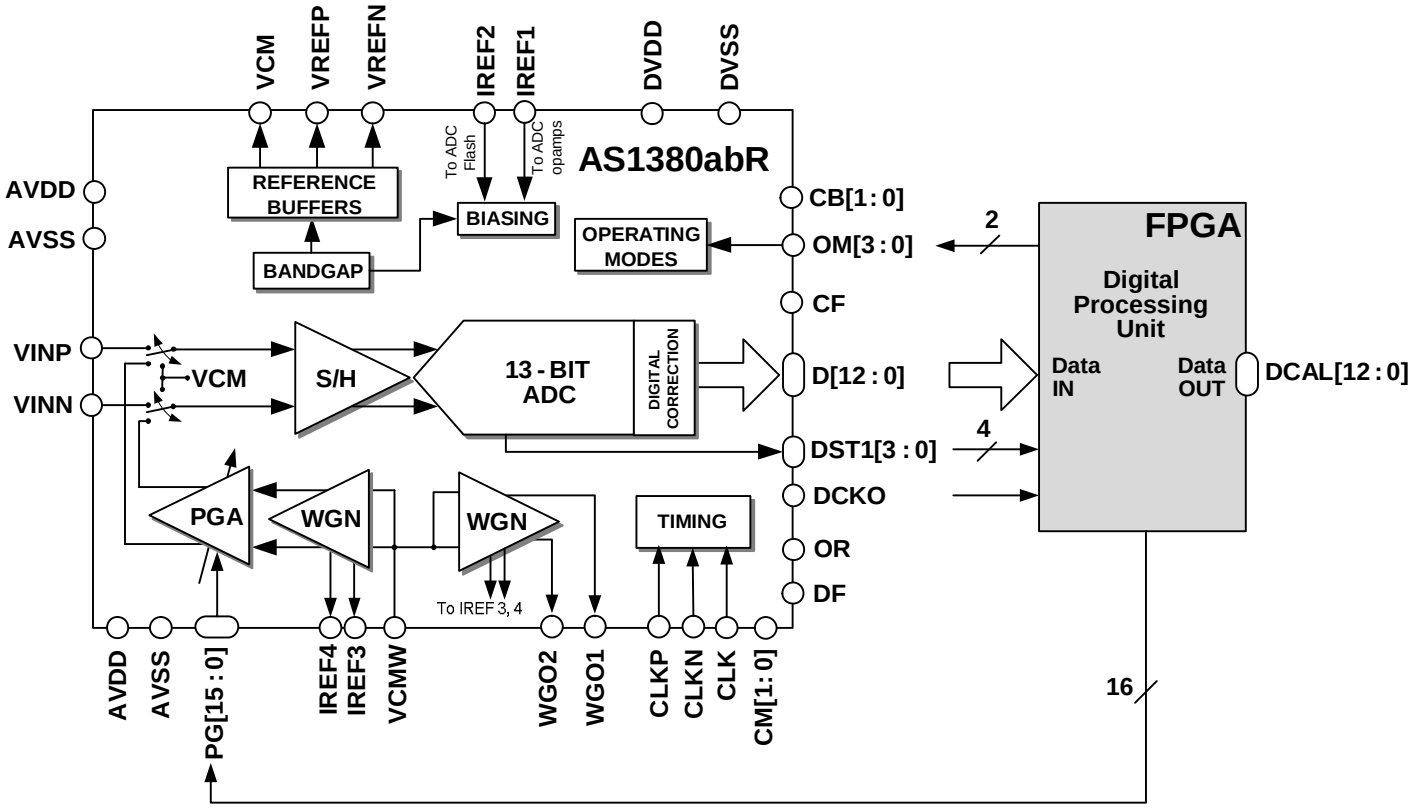


Very large number of noise samples (2^30).

Impossible to test algorithm by means of electrical simulation.

Complete A/D system architecture

- A 13-bit pipeline ADC is associated to a noise generator (WGN) and to a 16-bit PGA.
- For flexibility in testing, an FPGA implements the calibration algorithm.

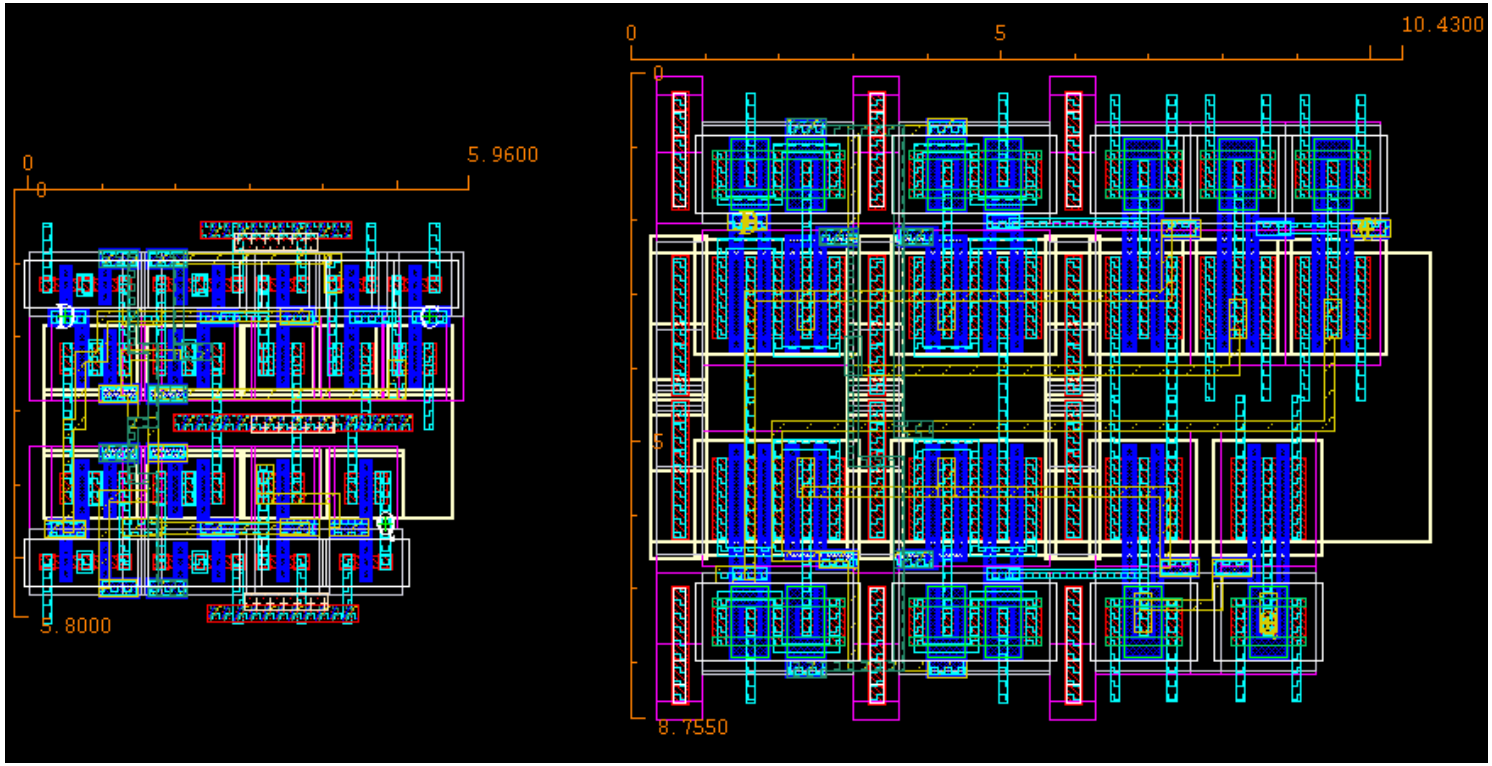


Radiation Robustness by Design

	Specification	Effect in the circuit	Hardening by Design Techniques Employed
TID	100krad Max. (Phase 1) 1000krad Max. (Phase 2)	V_T change	• Effect diminished has process geometries are reduced. Should not be very critical in 90nm technology. • Use high-Vt NMOS and standard-Vt PMOS devices. • Design transistors with a lower V_{Dsat} voltage to improve robustness to Vt variations. • Calibrate the ADC offset.
TID	100krad Max. (Phase 1) 1000krad Max. (Phase 2)	Parasitic leakage current	• Use P+ guard rings to separate different circuit in the layout. • Use enclosed layout transistors specially designed for this project by S3 Portugal.
SEL	70MeV.mg-^{1}.cm^{2}	Circuit latch-up	• Use large P+ guard rings to separate NMOS and PMOS transistors. • Use large N+ guard rings inside NWELLS.

ADC Design – Example of D Flip-Flop

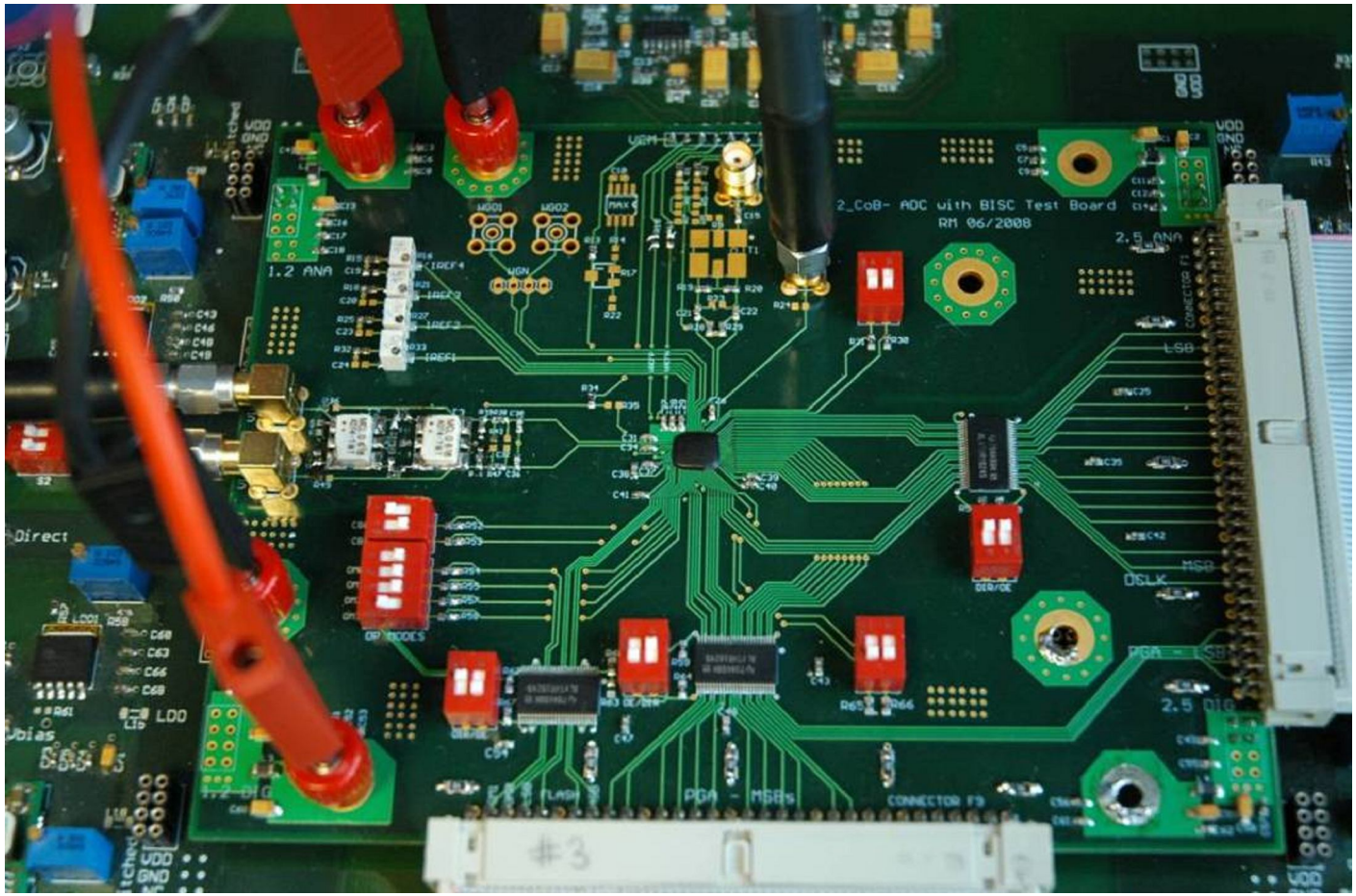
D-Type Flip-Flop Circuit Layout



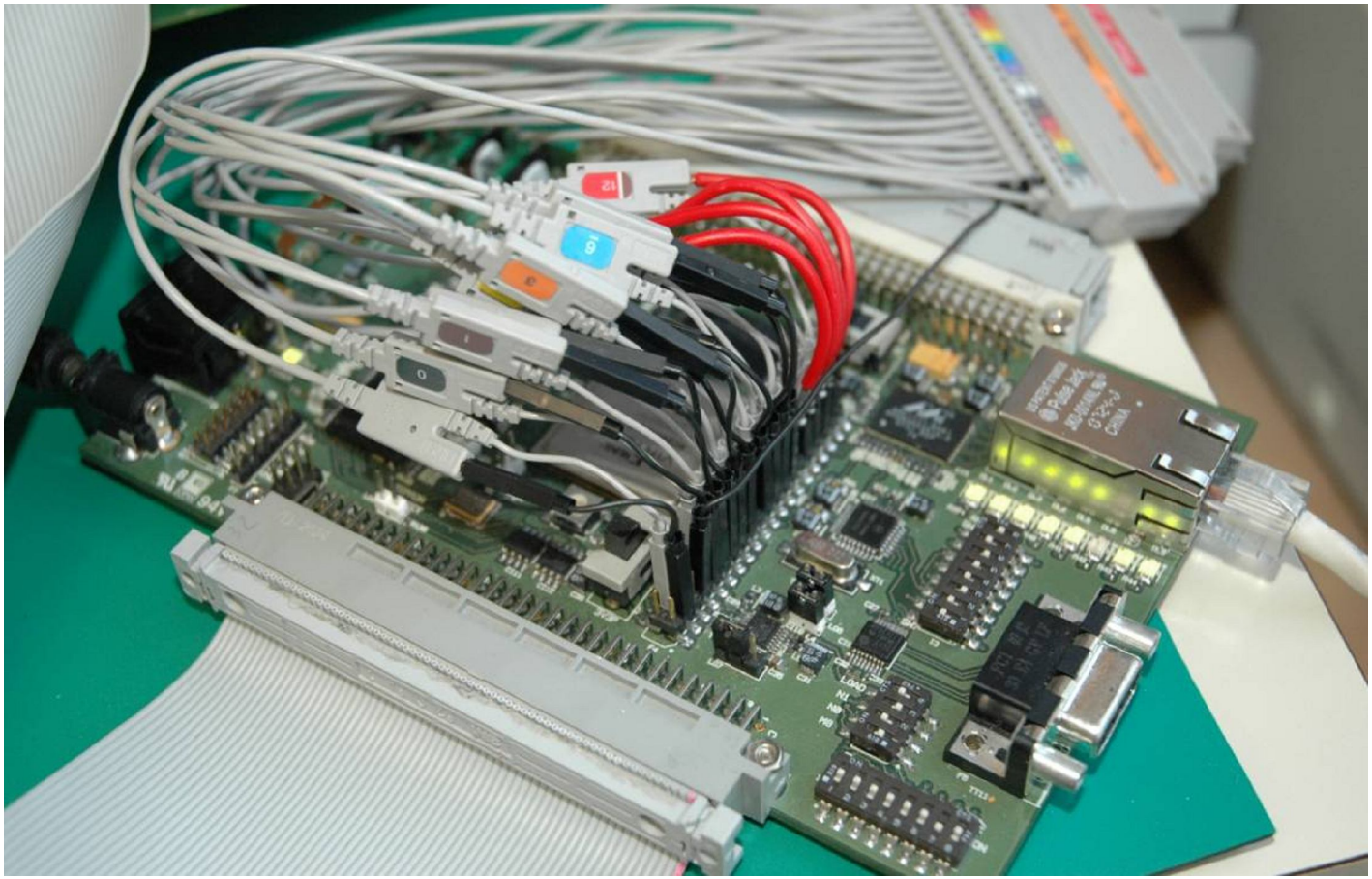
No encloded transistors

With encloded transistors.
Area = 2.6X larger

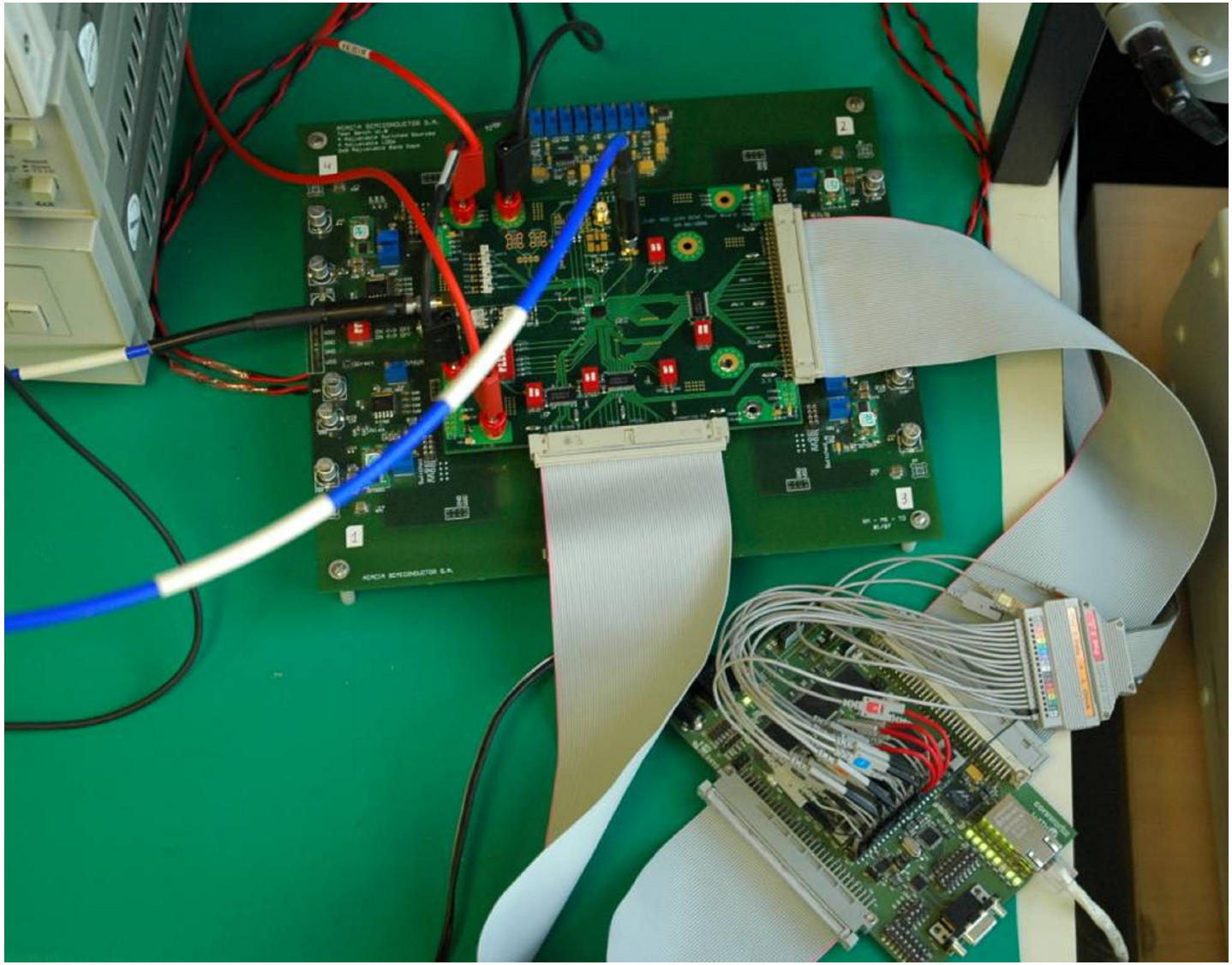
CoB assembly & PCB board for full performance evaluation at S3 Portugal labs



FPGA Board



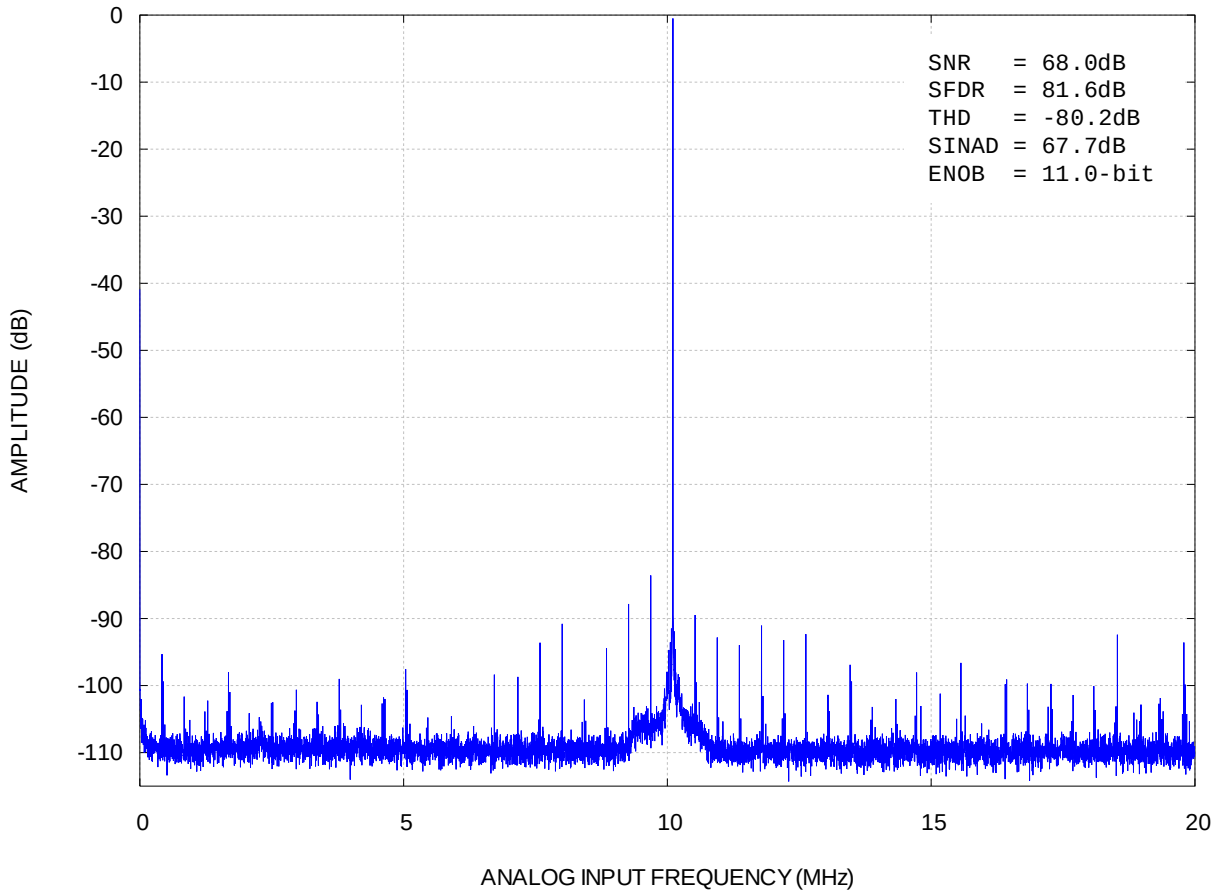
CoB Assembly Test PCB + FPGA Board



Test Results (ADC Stand-Alone)

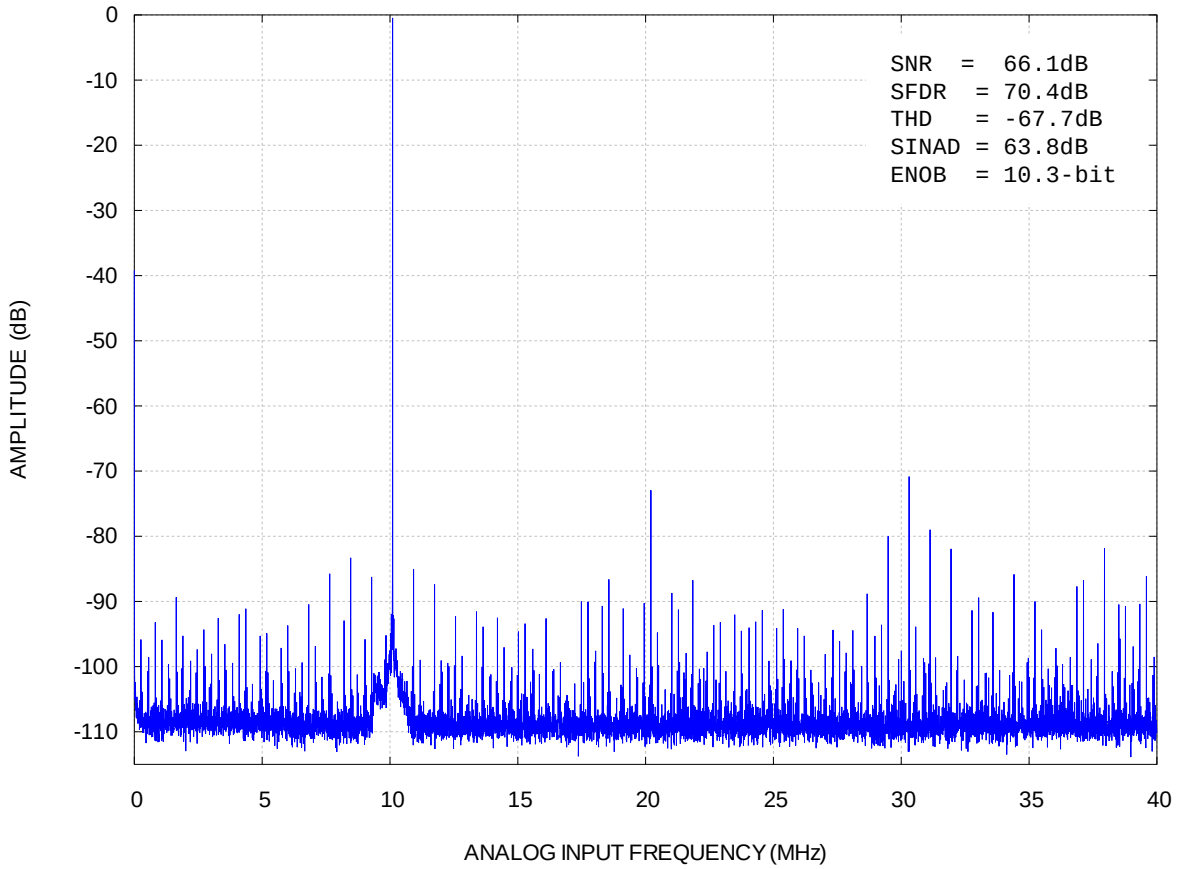
ADC Stand-Alone Silicon Tests

FFT for 40MS/s and 1.2V at +27ºC, 50mW @1.2V



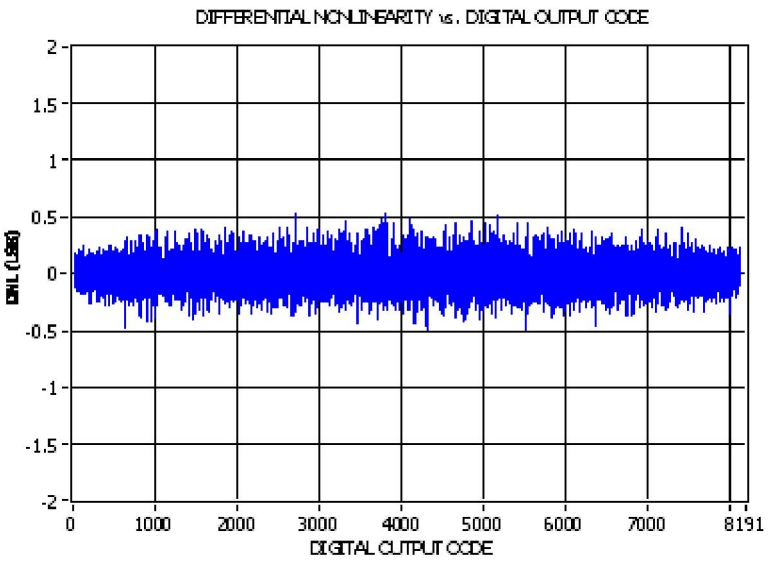
ADC Stand-Alone Silicon Tests

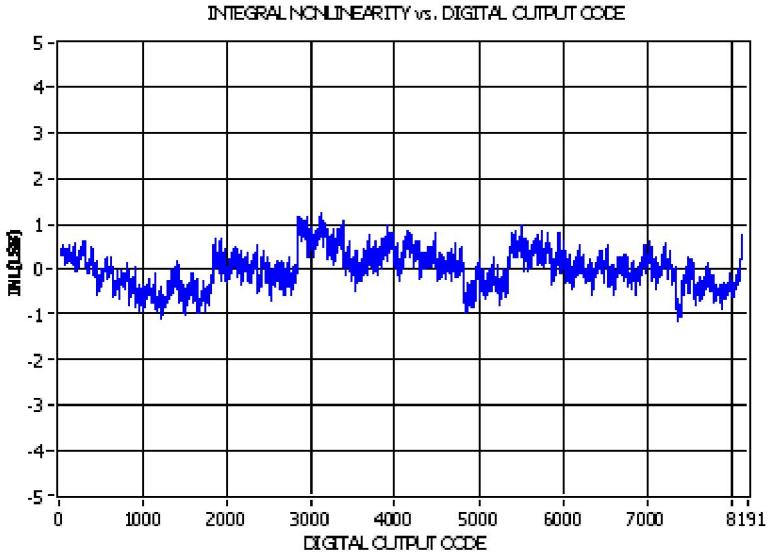
FFT for 80MS/s and 1.2V at +27ºC, 93mW @ 1.2V



ADC Stand-Alone Silicon Tests

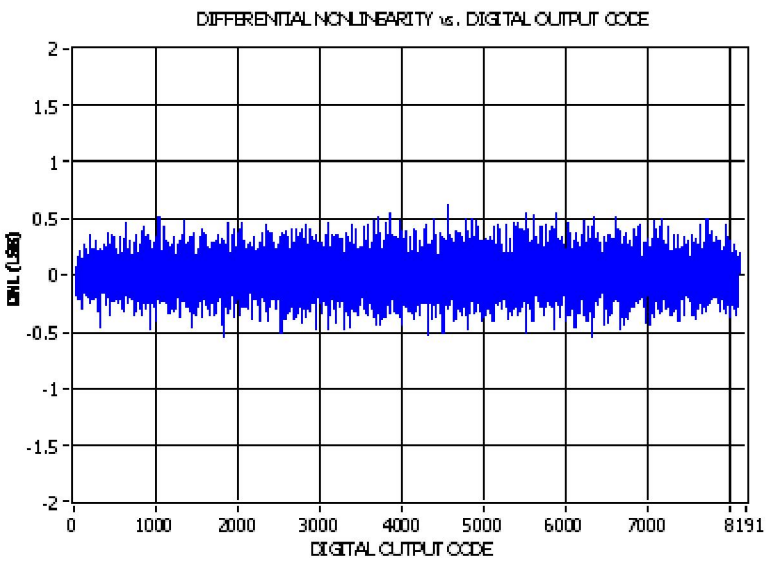
DNL, INL for 40MS/s and 1.2V at +27ºC

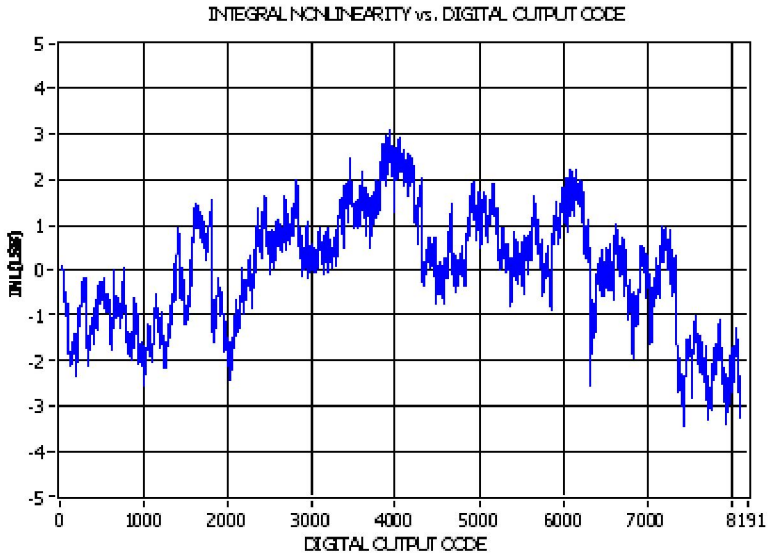




ADC Stand-Alone Silicon Tests

DNL, INL for 80MS/s and 1.2V at +27ºC

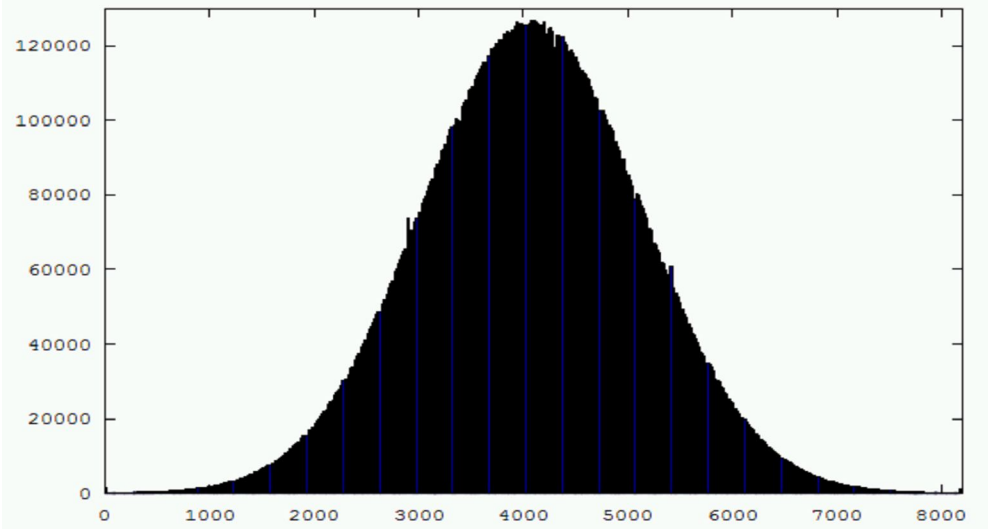




Test Results (ADC + BISC)

Measured results: WGN block

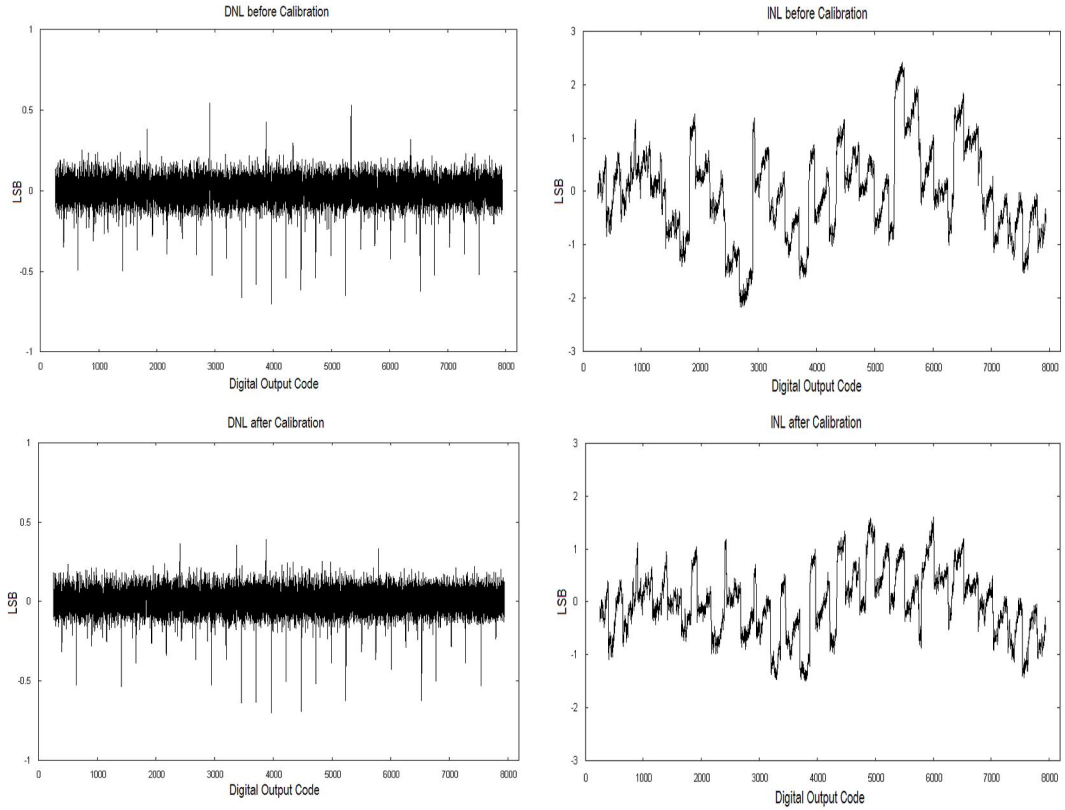
- The 13-bit ADC was used to digitalize the WGN (GNG) noise at 80 MS/s, 20.8 million samples were collected at the outputs of the ADC and an histogram was computed. After statistical analysis, we found that both, the asymmetry and kurtosis coefficients are very close to the expected ideal values (zero).



20M samples digitized by ADC @80MS/s

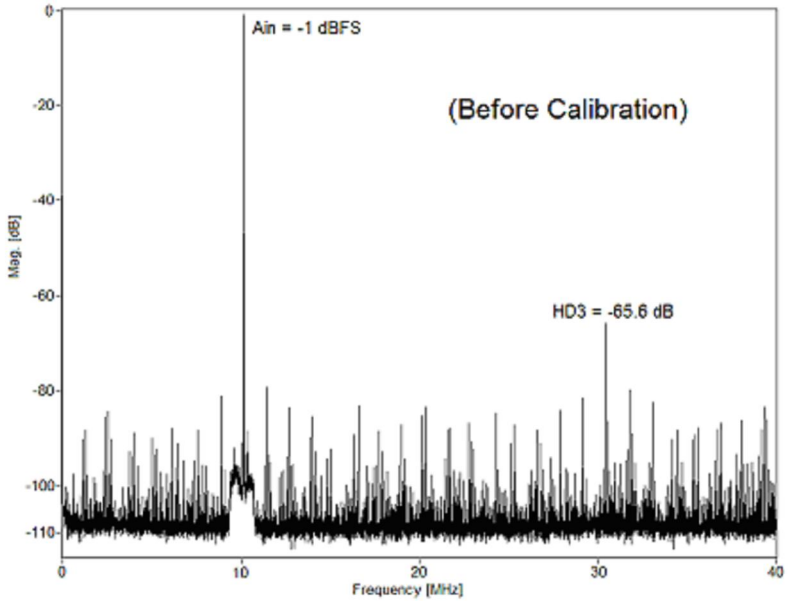
Parameter	Measured Results	
	Fs = 80 MS/s	Unit
Mean	4148.0	LSB
Offset	52.0	LSB
Standard-deviation, σ	1052.0	LSB
Asymmetry coefficient	0.0000516	-
Kurtosis coefficient	-0.0018050	-

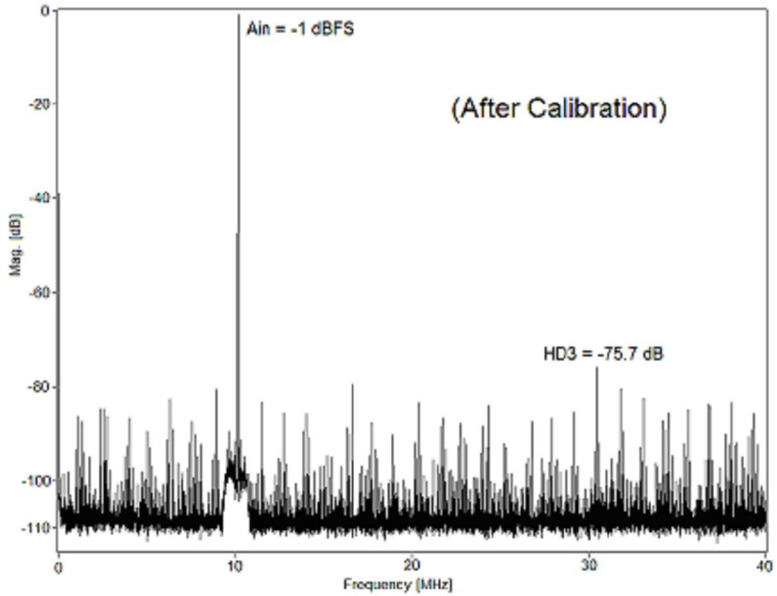
Measured results: DNL/INL @ 80 MS/s



- Calibration improves both characteristics and, after calibration, INL is bounded to ±1.5 LSB.
- This limit is mainly imposed by the second stage in the pipelined chain (that corresponds to the first stage of the 10-bit back-end ADC) which has an 1.5-bit resolution and it is not calibrated.

Measured results: FFTs @ 80 MS/s





- SFDR is improved by 10dB to 74.6dB
- THD is improved by 8.4dB to -72.7dB

Radiation Test Results

Key Goals for TRAD for Phase 2

- Obtain similar ADC dynamic performance as obtained in S3 lab (above 10-bit ENOB)
  - S3 designed the new PCB platform (mother and daugther board) targeting improved performance
  - S3 provided SRS signal generator for sampling clock purposes
  - S3 provided input signal Band-Pass filter of 10.7MHz
- Test up to 1000 krad (1076krad)
- 5 irradiated samples + 1 reference sample

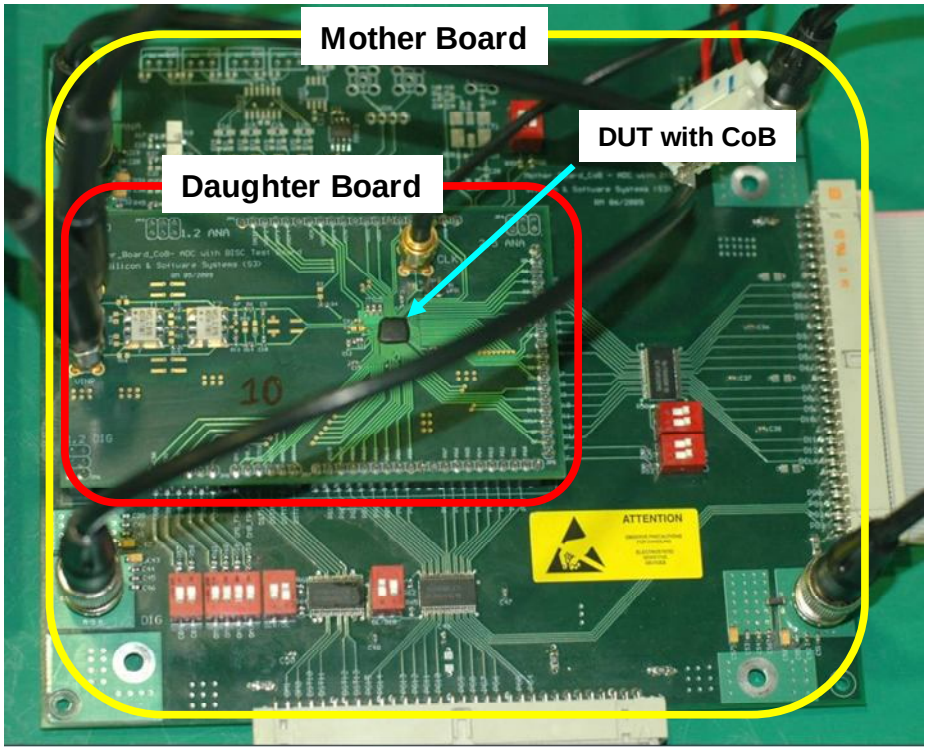
TRAD Phase 2

Chip On-Board Assembly

+ PCB designed by S3

= improved test results by TRAD

= over 2x better performance (over 9-bit ENOB)



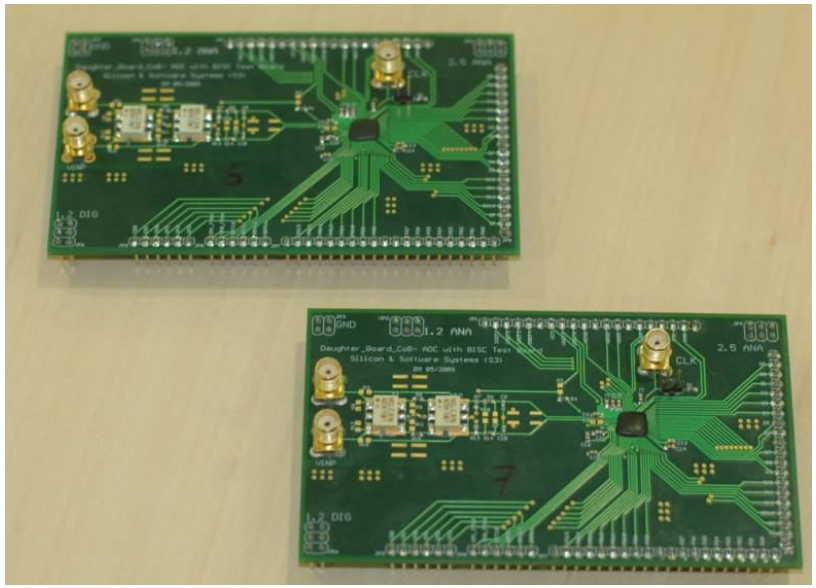
Chip On-Board Assembly

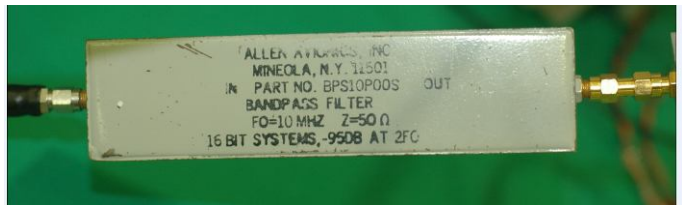
+ PCB designed by S3

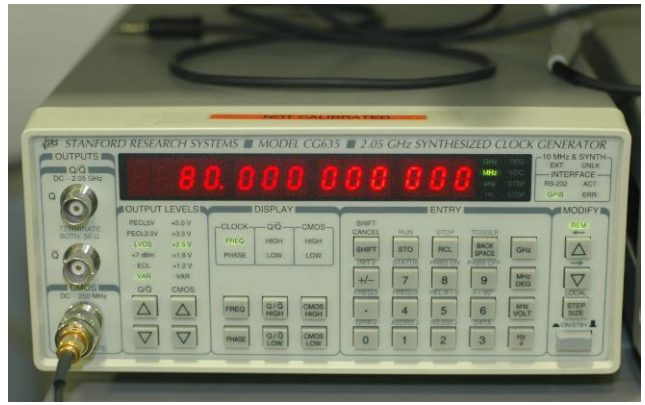
+ test equipment (filter, clock gen) provided by S3

= high performance test results by TRAD

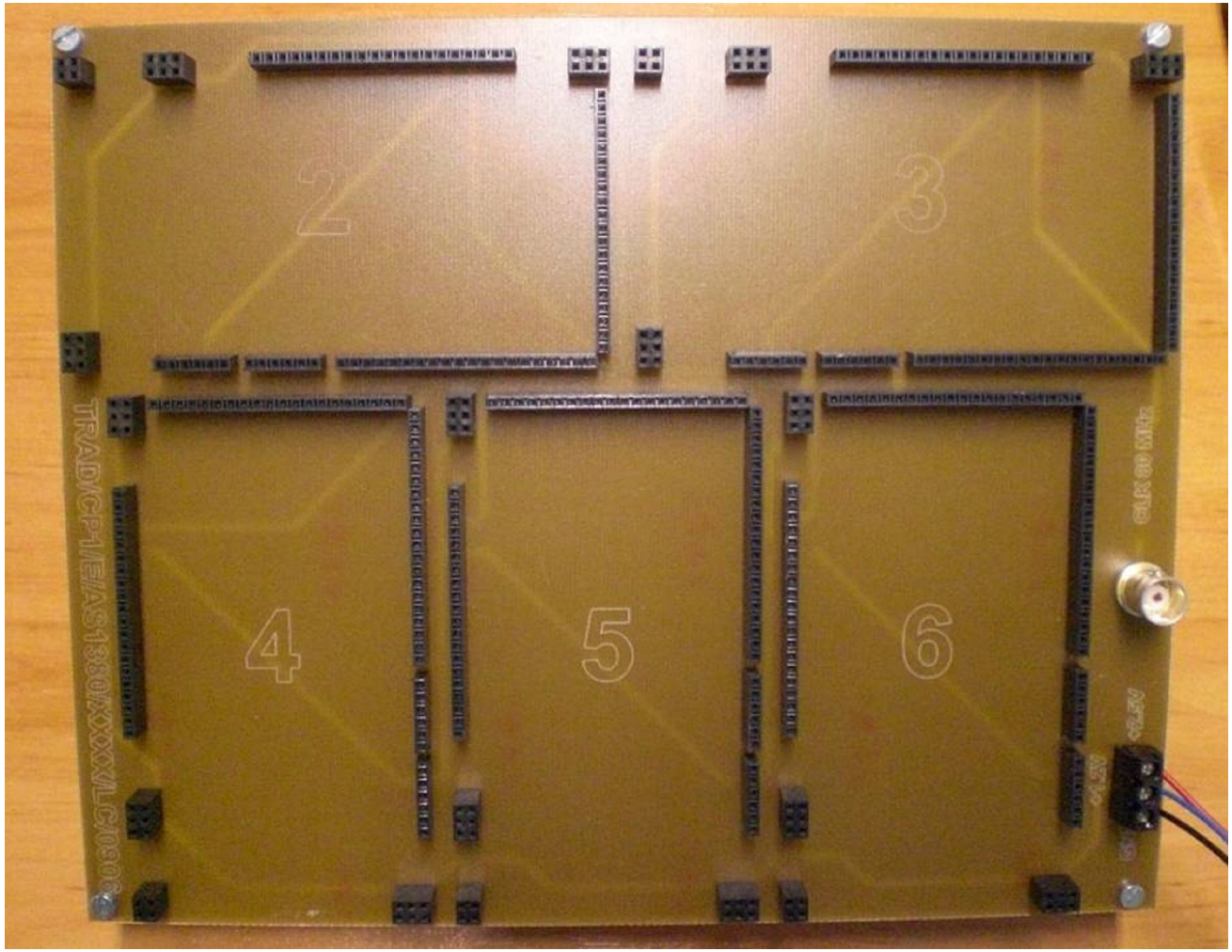
= over 4x better performance (over 10-bit ENOB)



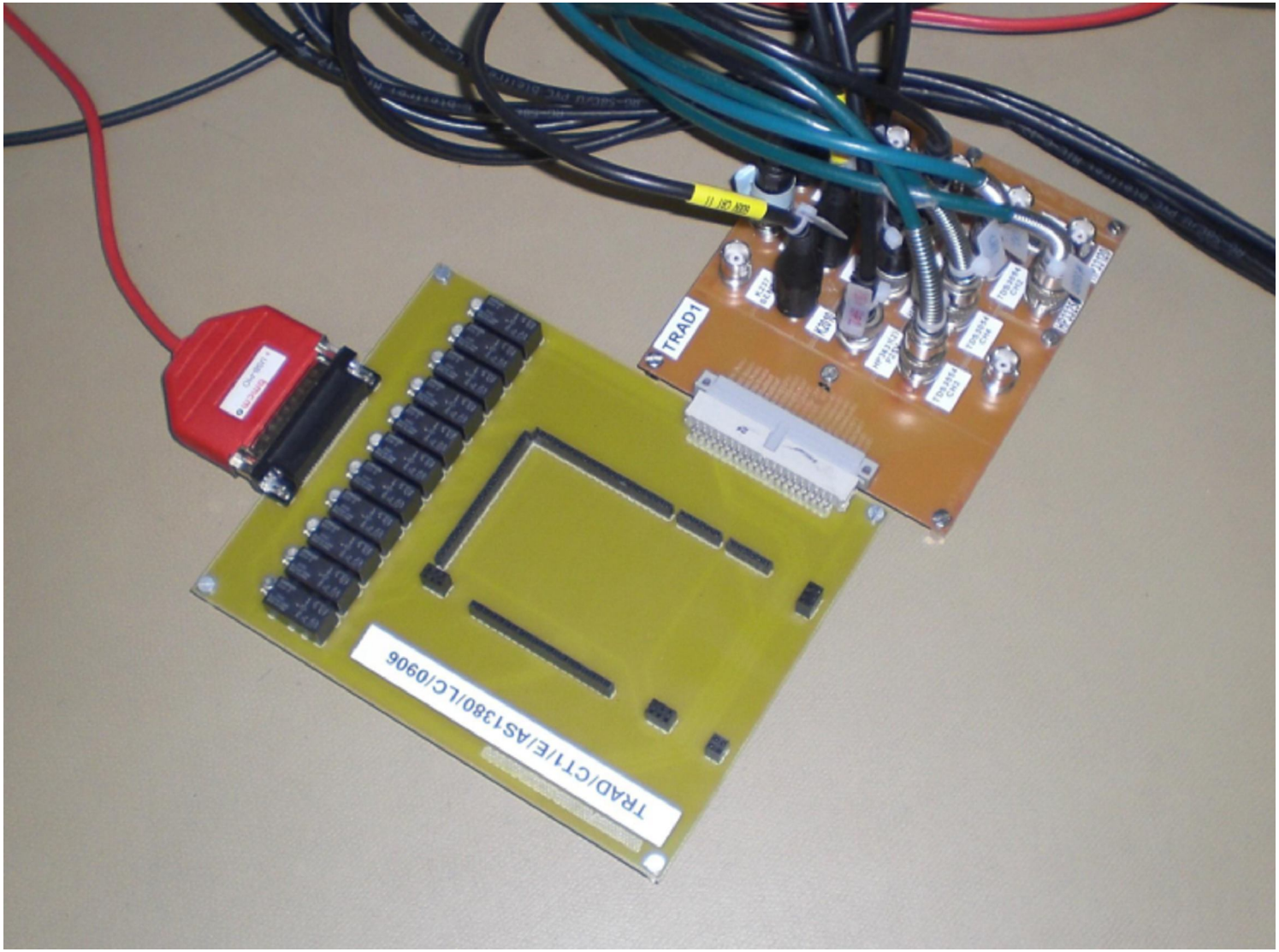




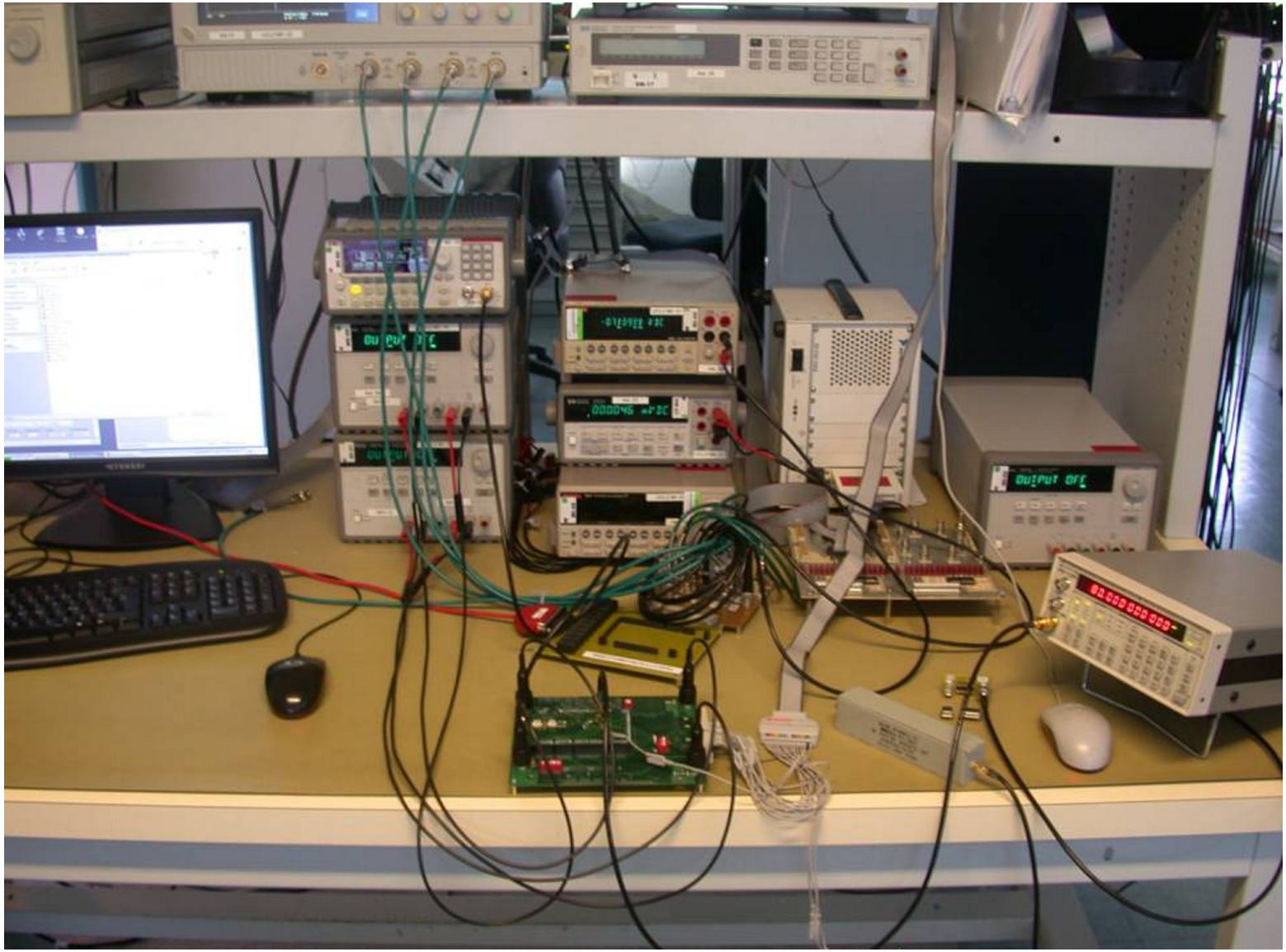
Phase 2 – TRAD Test Platform



Phase 2 – TRAD Test Platform

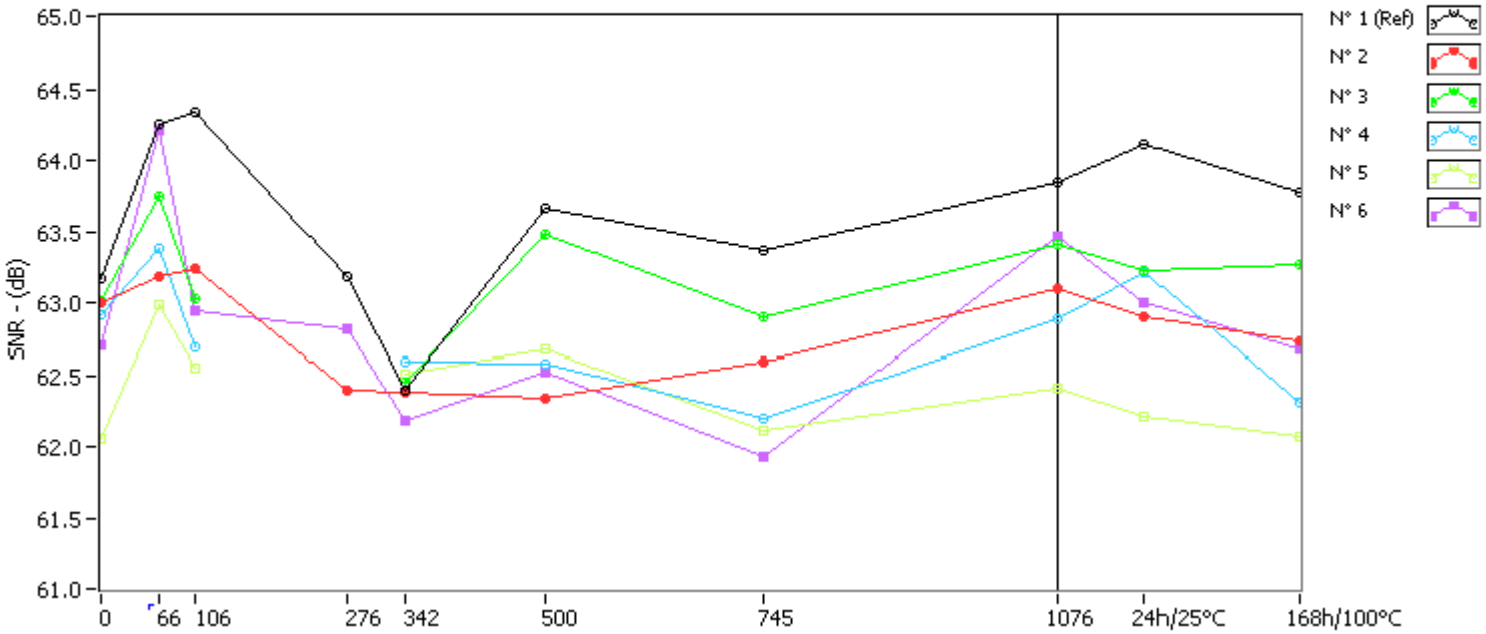


Phase 2 – TRAD Test Lab



35. SNR

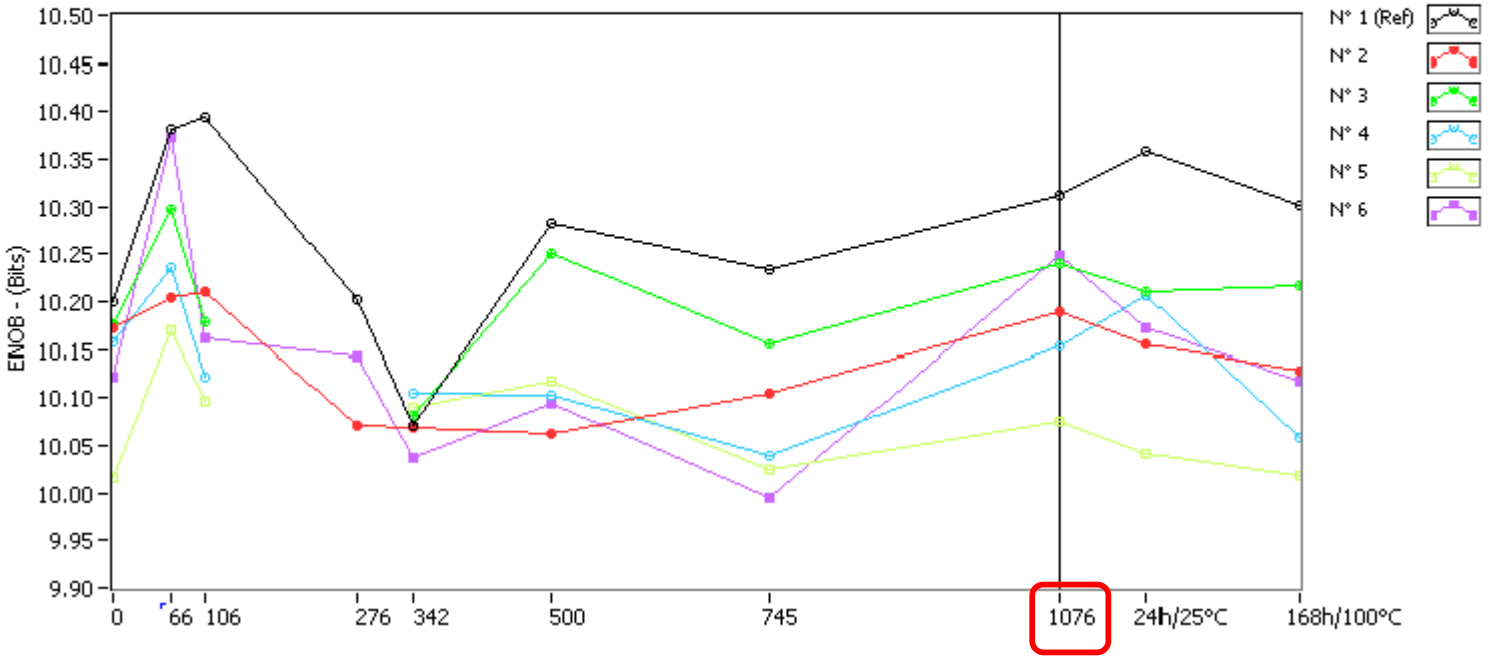
T=25°C; AVDD=DVDD=+1.2V; 80MS/s Sampling Rate; 50% Duty Cycle Clock; Differential Sine-Wave Input Analog Signal with -1.4dBFS Amplitude and 10.7 MHz Frequency ; Full Scale of 1.0Vppdiff



TID Radiation Tests Phase 2

ENOB Measurements by TRAD, at 80MS/s, 1 ref + 5 samples, up to 1076krad

T=25°C; AVDD=DVDD=+1.2V; 80MS/s Sampling Rate; 50% Duty Cycle Clock; Differential Sine-Wave Input Analog Signal with -1.4dBFS Amplitude and 10.7 MHz Frequency ; Full Scale of 1.0Vppdiff



ENOB . (Bits)

	0krad(Si)	66krad(Si)	106krad(Si)	276krad(Si)	342krad(Si)	500krad(Si)	745krad(Si)	1076krad(Si)	24h/25°C	168h/100°C
N° 1 (Ref)	10.200	10.381	10.394	10.203	10.072	10.282	10.233	10.312	10.358	10.302
N° 2	10.173	10.204	10.212	10.071	10.070	10.063	10.105	10.190	10.156	10.129
N° 3	10.176	10.298	10.178	7.240	10.082	10.251	10.155	10.241	10.210	10.217
N° 4	10.158	10.235	10.121	5.620	10.105	10.103	10.040	10.153	10.207	10.058
N° 5	10.017	10.171	10.097	1.001	10.091	10.119	10.024	10.075	10.041	10.018
N° 6	10.123	10.373	10.163	10.143	10.038	10.093	9.995	10.249	10.173	10.118

Summary of Measured Results

Parameter	Measured Specification	Comments
General Specifications		
Resolution	13-bit	
Sampling Rate	80MS/s	
Supply Voltage	1.2V ±10%	
Junction Operating Temperature	-40°C to +125°C	
Die Area ADC Core	0.88mm²	Over-achieved. Actual die area 41% below target.
Die Area Analog BISC	0.28mm²	
Radiation Specifications		
Total Ionizing Dose (TID)	1076krad	Better than 10x versus spec.
Single-Event Latch-up (SEL)	70 MeV.mg^{-1}.cm²	
Static Performance		
Differential Non-Linearity Error	<±1LSB	Achieved < ±1 LSB even without calibration at 40MS/s and 80MS/s.
Integral Non-Linearity Error Before Calibration	<±4LSB	
Integral Non-Linearity Error After Calibration	±2LSB	Achieved after calibration.
Dynamic Performance		
Signal to Noise Ratio (SNR) At 40MS/s	68dB	
Signal to Noise Ratio (SNR) At 80MS/s	66dB	
Total Harmonic Distortion (THD) – Before to Calibration	-68dB	
Total Harmonic Distortion (THD) – After Calibration	-75dB	
Effective Number of Bits (ENOB) Before Calibration at 40MS/s	10.9	
Effective Number of Bits (ENOB) Before Calibration at 80MS/s	10.3	
Effective Number of Bits (ENOB) After Calibration at 80MS/s	10.8	
Power Dissipation at 40MS/s	50mW	Typical.
Power Dissipation at 80MS/s	93mW	Typical, -20% below spec.
Calibration Time at 40MS/s	54s	
Calibration Time at 80MS/s	27s	