Pressure Sensor Interface (pSIF) ASIC

DUTH/SRL - SPACE ASICS

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Rationale & Goals

What is currently available?

- Pressure sensor biasing relies on discrete components.
- Signal conditioning relies on discrete components.
- Analog signals are transferred to a remote ADC where quantization and calibration takes place.
- Alternatively, use a commercial μController with all the drawbacks of such a solution.

What will pSIF offer

- RadHard, low power, all in one device (Sensor biasing, signal conditioning, ADC and data transmission).
- In addition, various strain gauge types of sensors can be handled.

Functionality and Block Diagram

Functionalities

- Bias the sensor with either a constant voltage or a constant current
- Amplify with a programmable gain the differential voltage
- Quantize the differential sensor voltage and the sensor voltage Vs and Vr
- Transmit the quantized sensor data to the S/C through the I2C bus
- Handle up to 4 sensors simultaneously

Key Features

- Programmable gain amplifier (20 to 80dB) with offset correction
- 14 bit ADC (12 true)
- Power consumption $<$15mW (including one sensor current)
- -55 to + 125°C operating range
- TID Hardness $>$ 1Mrad
- No SEEs up to $80 MeV/mg/cm^2$ (maximum LET value tested)
- On chip voltage reference
- Single 3.6 to 2.0 V power supply.

pSIF Block Diagram

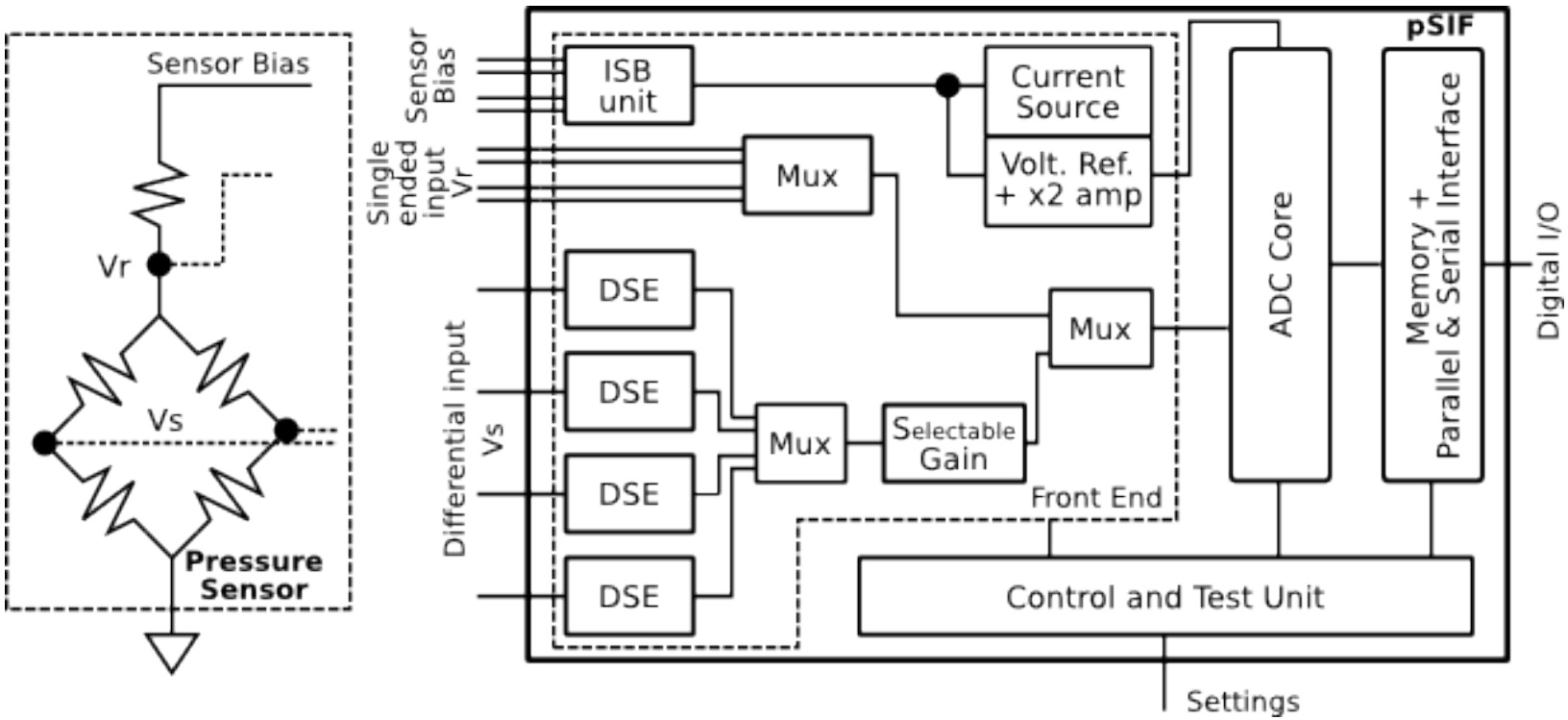


Figure: Block diagram of the EM pSIF device.

pSIF Blocks

Analog

- ISB circuit that handles the biasing of the sensors attached to the device.
- 4 Differential to Single Ended (DSE) conversion units (one per sensor). The DSE stages apart from converting the differential voltage to a single ended, they also provide a gain of 20-40dB.
- A programmable amplification unit (pgain). The gain of this unit is programmed through an I2C/parallel command.
- 3 Multiplexers that direct the input voltages to the ADC core.
- A Current Source that is used for providing a bias current to the sensor.
- A Voltage Reference unit which includes a bandgap reference and an x2 amplifier.
- A 14 bit ADC core.

Digital

- A Memory together with a parallel and serial interface unit.
- A Control and Test unit.

Key Features

Key Design Characteristics

- Over 100000 transistors (x5 physical)
- 80% is analog
- 20% is digital
- Full custom layout
- Fully transferable design
- Die size 5x5mm in UMC 0.25μm process
- AZ ADC (algorithmic topology based on AZ rad hard 11 and 5 bit SA cores)
- Substrate isolation between analog and digital

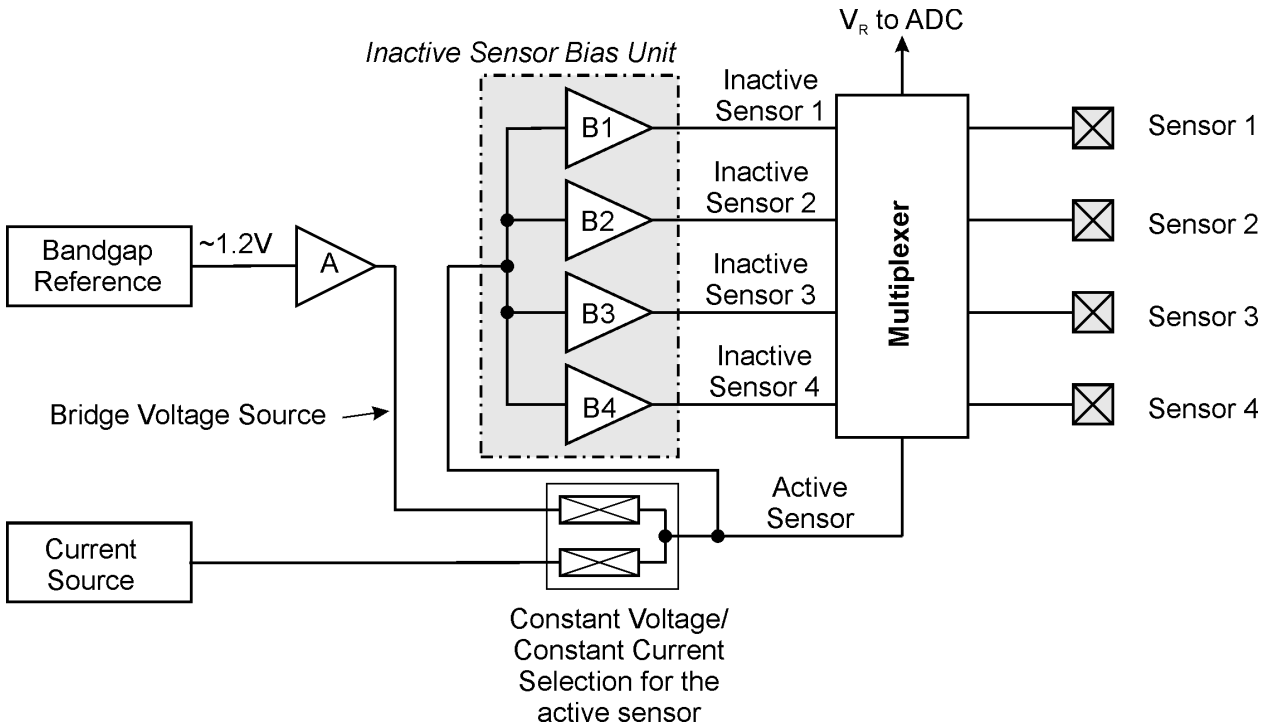
Sensor Biasing

Active Sensor Bias

- Through a constant voltage (up to 2.5V)
- Through a constant current (up to 3mA)

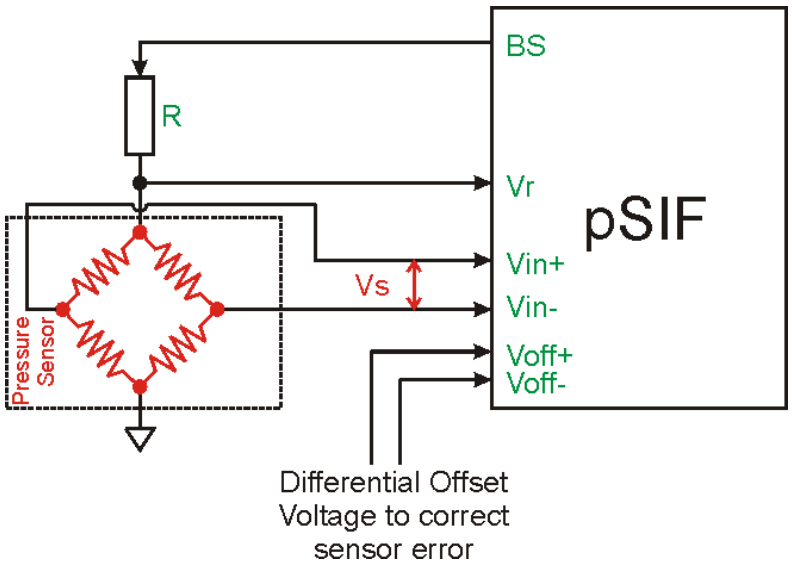
Inactive Sensor Bias

- When selected, a copy of the bias voltage on the active sensor is provided to the inactive sensors
- 4 3mA capable output buffers are used



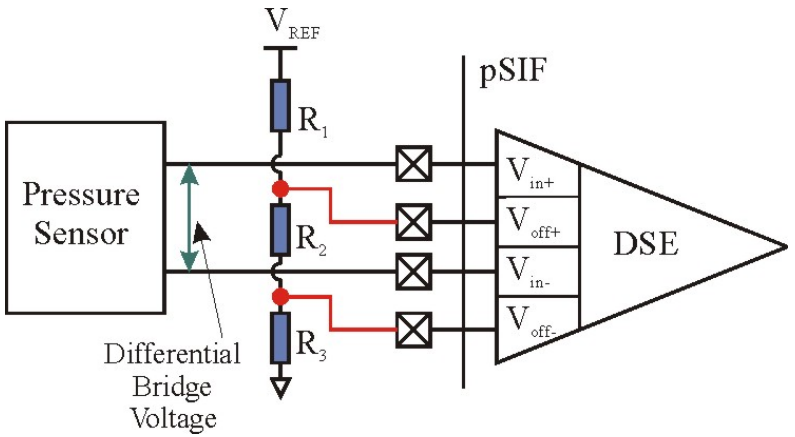
Sensor Interface Setup

Sensor Interface Setup



Sensor Offset Cancellation

Use of a differential difference amplifier (DDA)



Validation Status

Tests Performed

- Functional
- Thermal
- Power supply
- IDDQ, SAF
- TID
- SEE
- Burn in and life tests

Test Status

- EM design has been successful
- More than 70 devices tested. Yield close to 70%.

ADC Performance

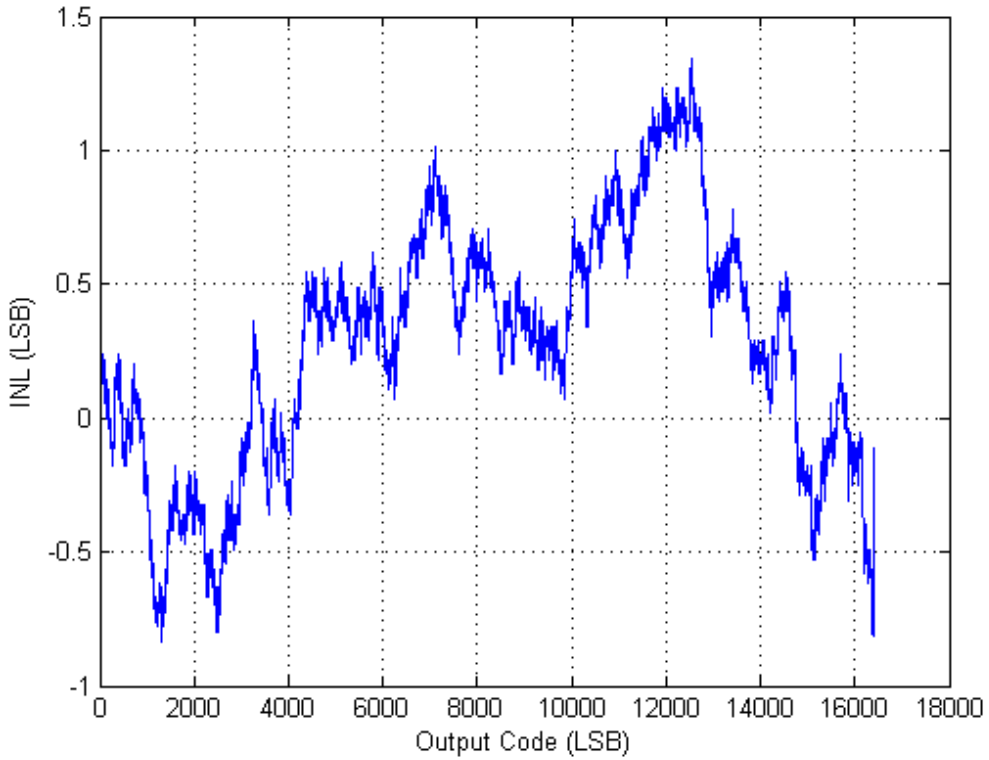


Figure: Typical ADC INL.

ADC Characteristics

- INL less than $\pm$1LSB
- Monotonicity
- No missing codes
- Max INL deviation from pre-rad @1MRad: $<$2LSB

ADC TID Performance

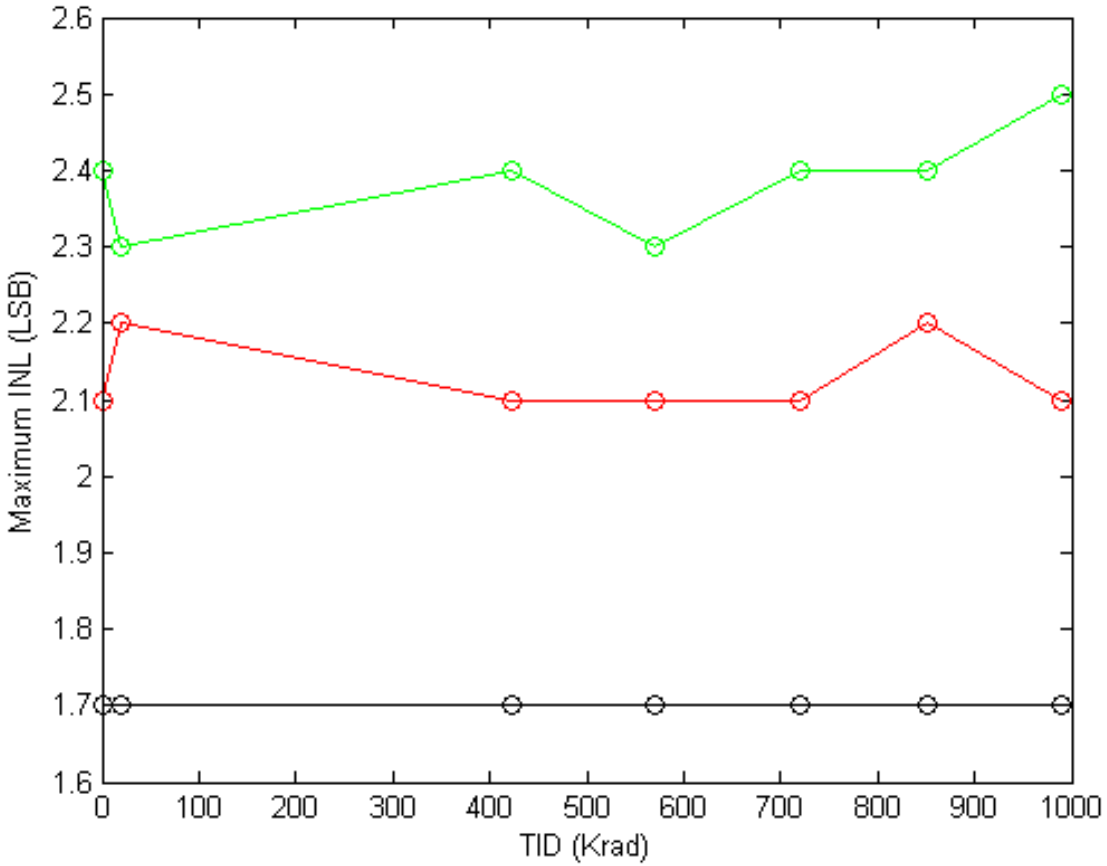


Figure: Maximum INL vs TID for three devices tested. INL remains constant with TID.

Voltage Reference Performance

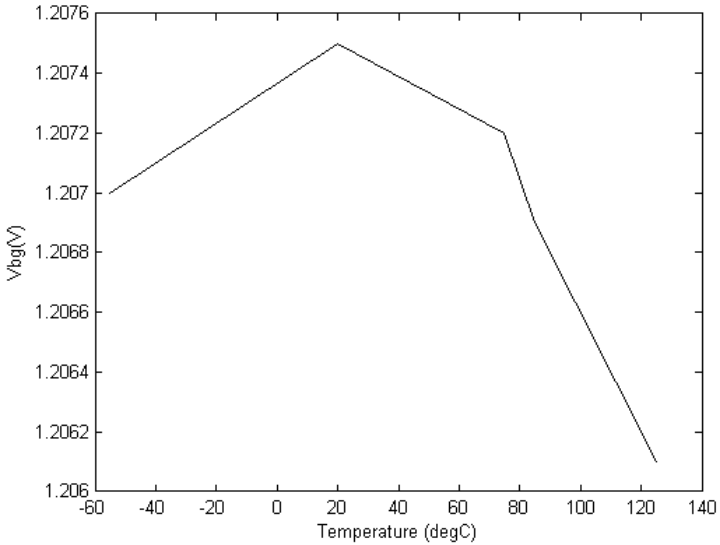


Figure: Typical V_{REF} versus temperature.

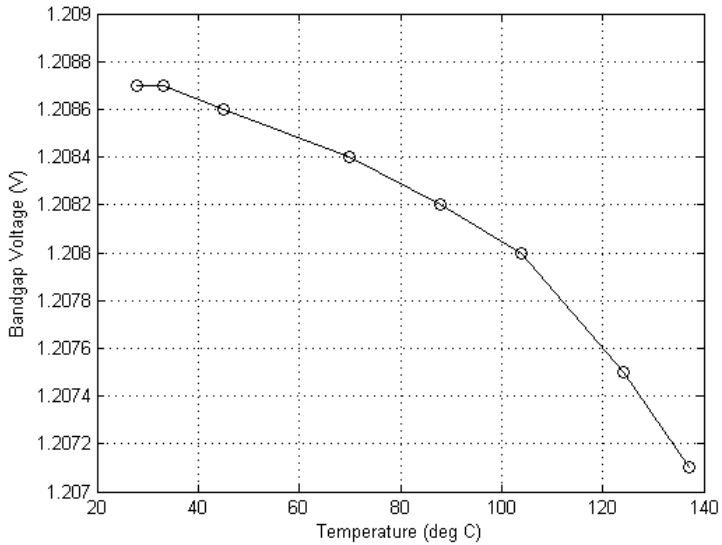


Figure: Typical V_{REF} versus temperature.

DSE Gain Results

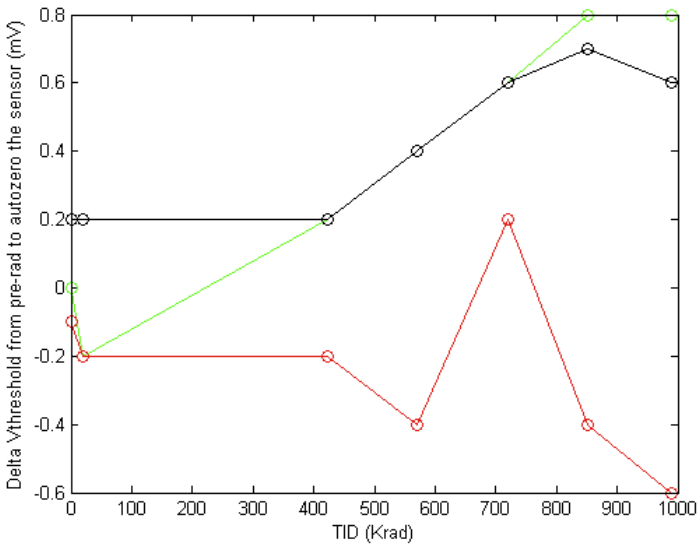


Figure: Offset of the DSE versus TID.

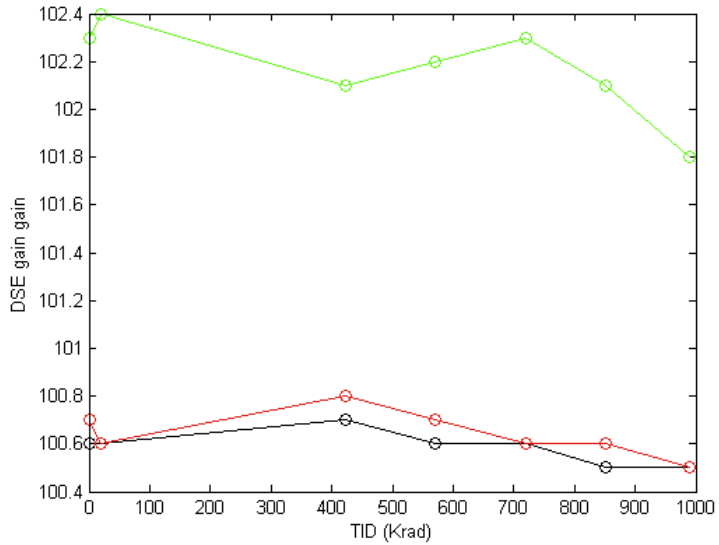


Figure: Gain Stability of the amplification stage vs TID.

Overall Performance

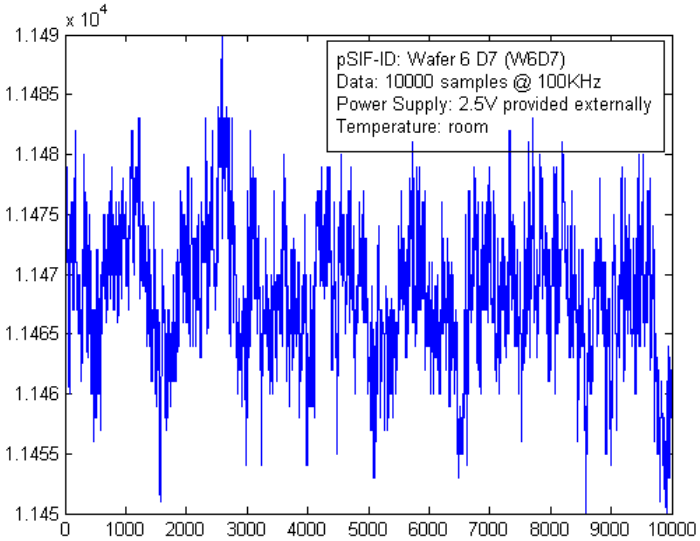


Figure: Typical ADC readout data for the full differential chain. All systems are on.

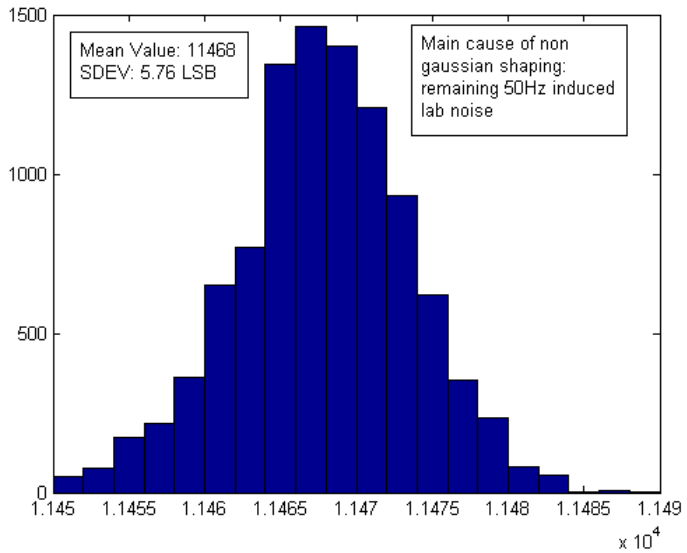


Figure: Histogram of the data.

Overall Performance

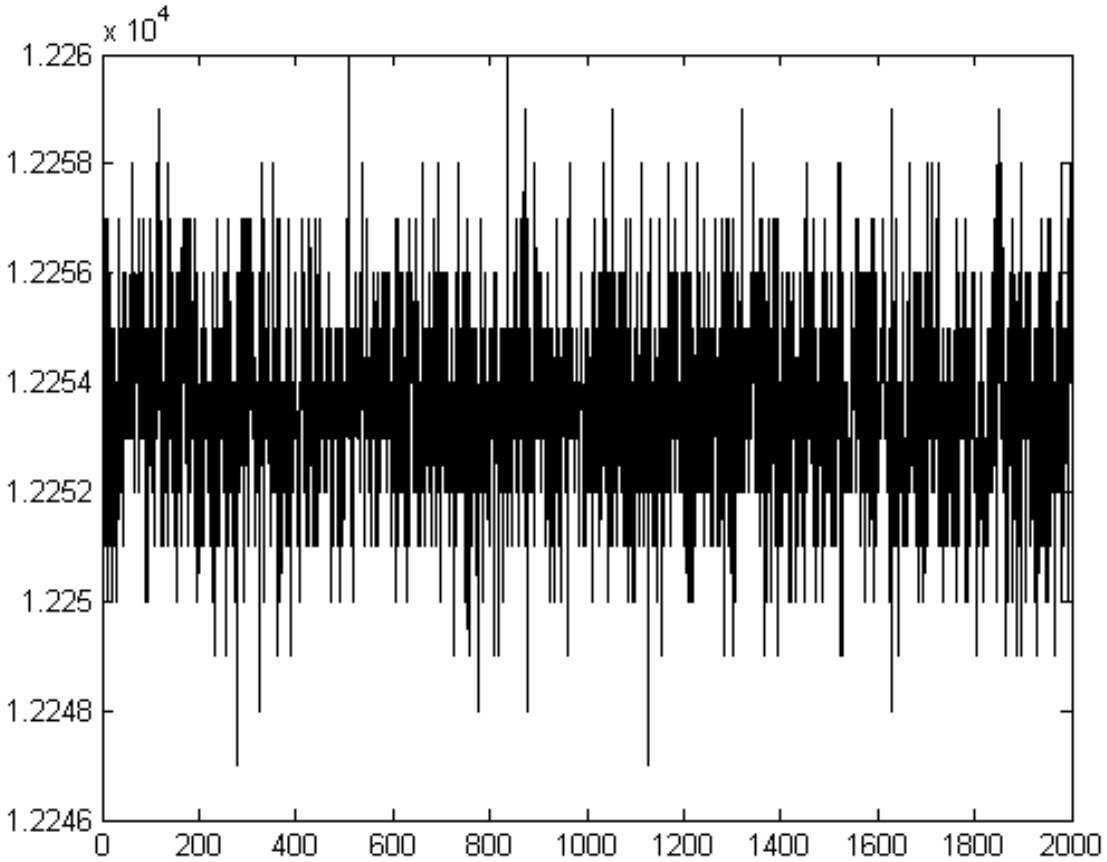


Figure: Typical ADC readout data when pSIF is powered with a battery. Noise sources are isolated.

Accomplishments

Low Power

- <15mW with the first run.

RadHard

- Very good Voltage Reference after 1Mrad.
- INL variation less than 1LSB after 1Mrad. No missing codes. AZ takes care of any TID induced errors.

Overall Performance

- Functioning device from the first run. In the analog world this is something that can't be taken for granted.

Future Work

FM Production

- Next generation of pSIF is expected in Q4 2010/Q1 2011.
- More generic capabilities will be added.
- A version of pSIF with a higher resolution ADC is being considered.