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Space

Industrial Applications

A 12 Bit High Speed Broad Band Low Power Digital to Analog Converter for Satellite Telecommunications

Microelectronics Presentation Days 2010

at ESTEC, Noordwijk

30 March – 1 April 2010

Kayser-Threde GmbH, Munich / Heinz-Volker Heyer
IHP Microelectronics GmbH, Frankfurt Oder / Karl Schrödinger

Contents

- Project team
- Major features
- Block diagram / overview
- Current switch and ladder structure
- Calibration mechanism
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- Simulations results
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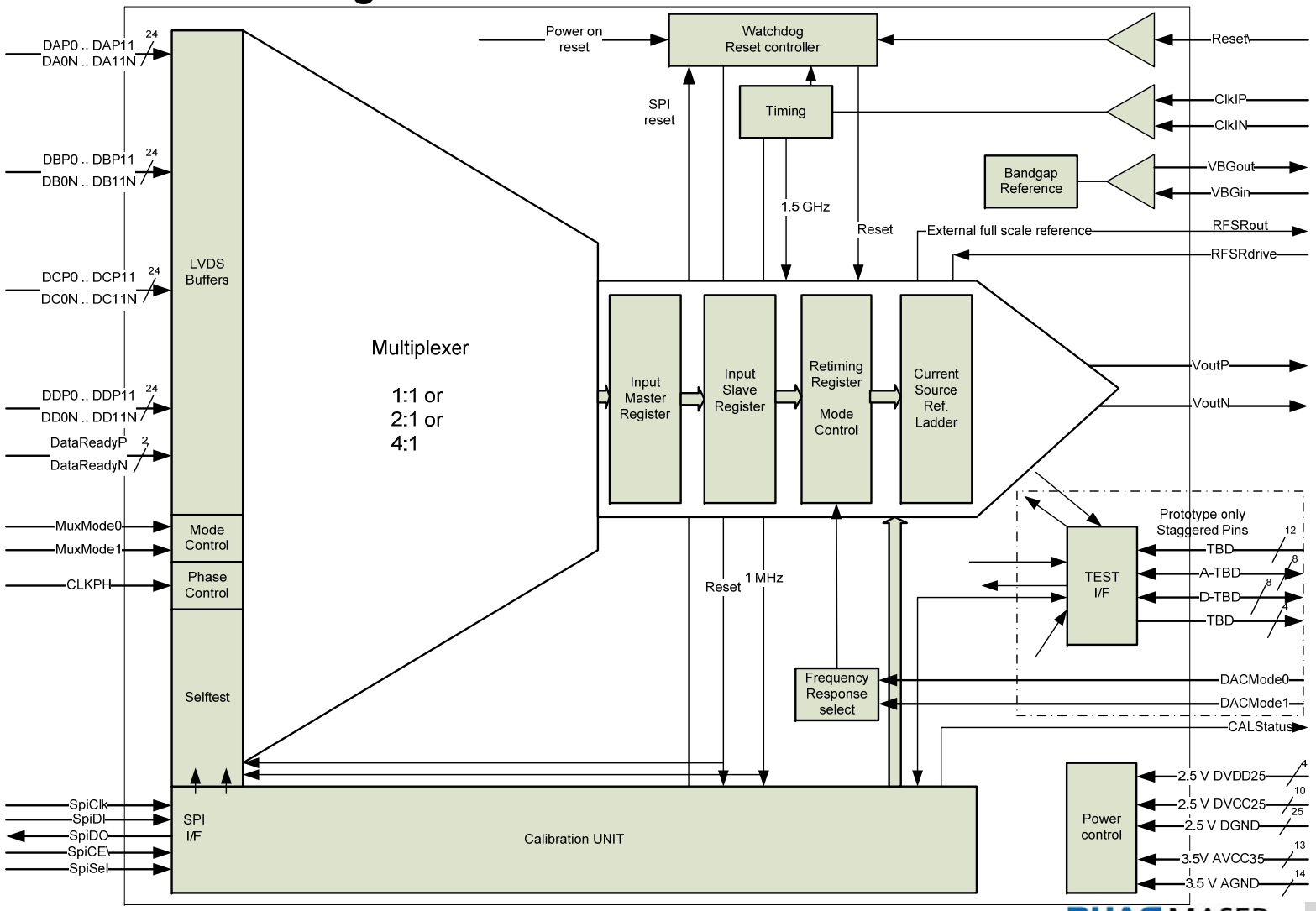
Project Partners:

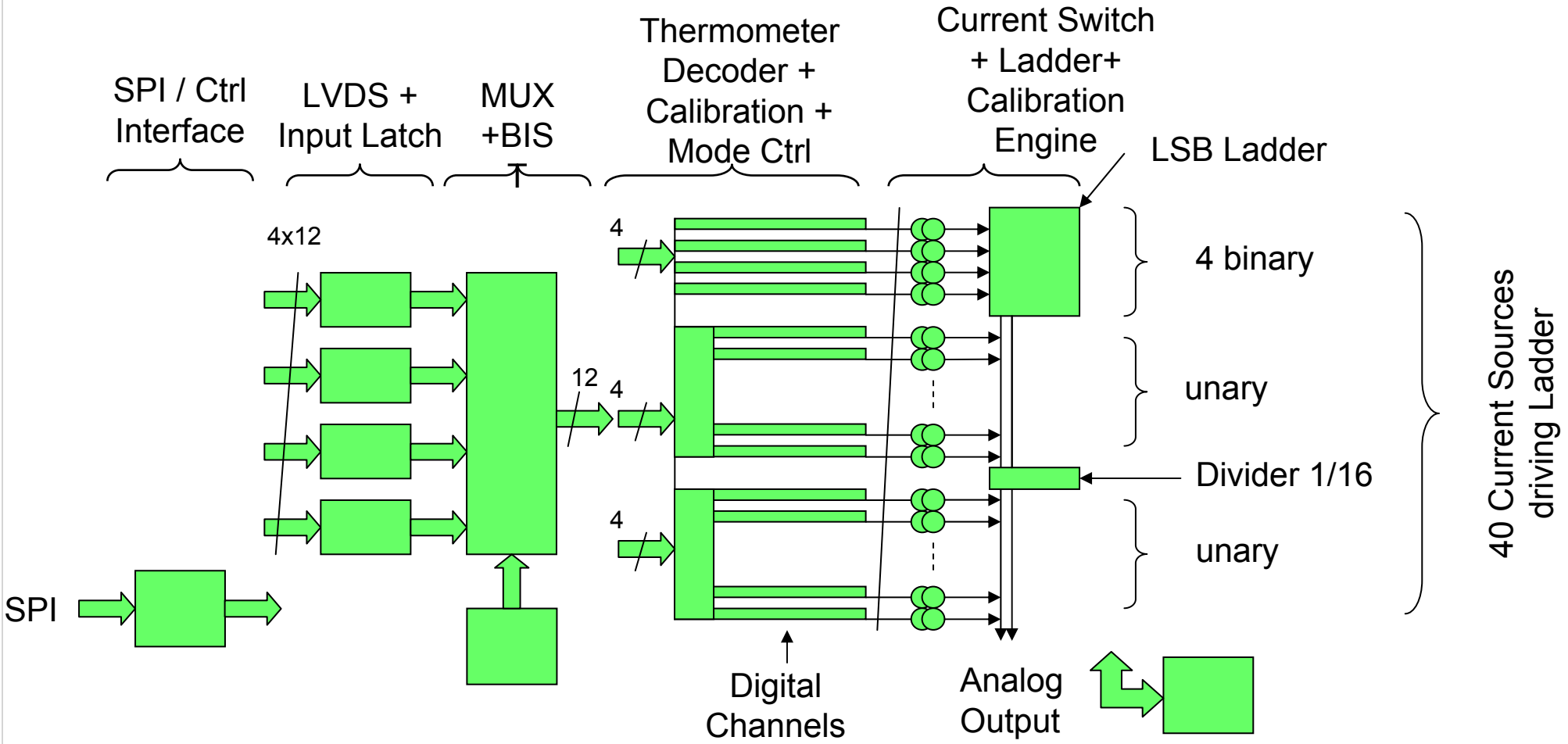
- **Kayser-Threde – Germany: Project management and radiation tests**
- **IHP – Germany: Analog high speed circuit design and technology support**
- **Advico – Germany: Low speed and digital circuit design**
- **Maser – Netherlands: Reliability**
- **Ruag – Sweden: Radiation support**
- **Astrium – GB / Thales – France: Application support, potential customers**

Major Features

- 12 Bit segmented DAC with 1.5 GHz sampling rate
- Low power LVDS input receivers and input latch
- Flexible CLK system: Flexible input CLK and system CLK
- 1:1, 1:2 and 4:1 multiplexer operation
- Multiple Built-In Self Test structures (BIST)
- Power on and (hidden) background calibration
- Multiple DAC modes: NRZ, RZ, RF → signal in 1st, 2nd and 3rd Nyquist zone
- Programmable high output level up to 1.6Vpk-pk at differential 100Ω load
- Radiation safe design

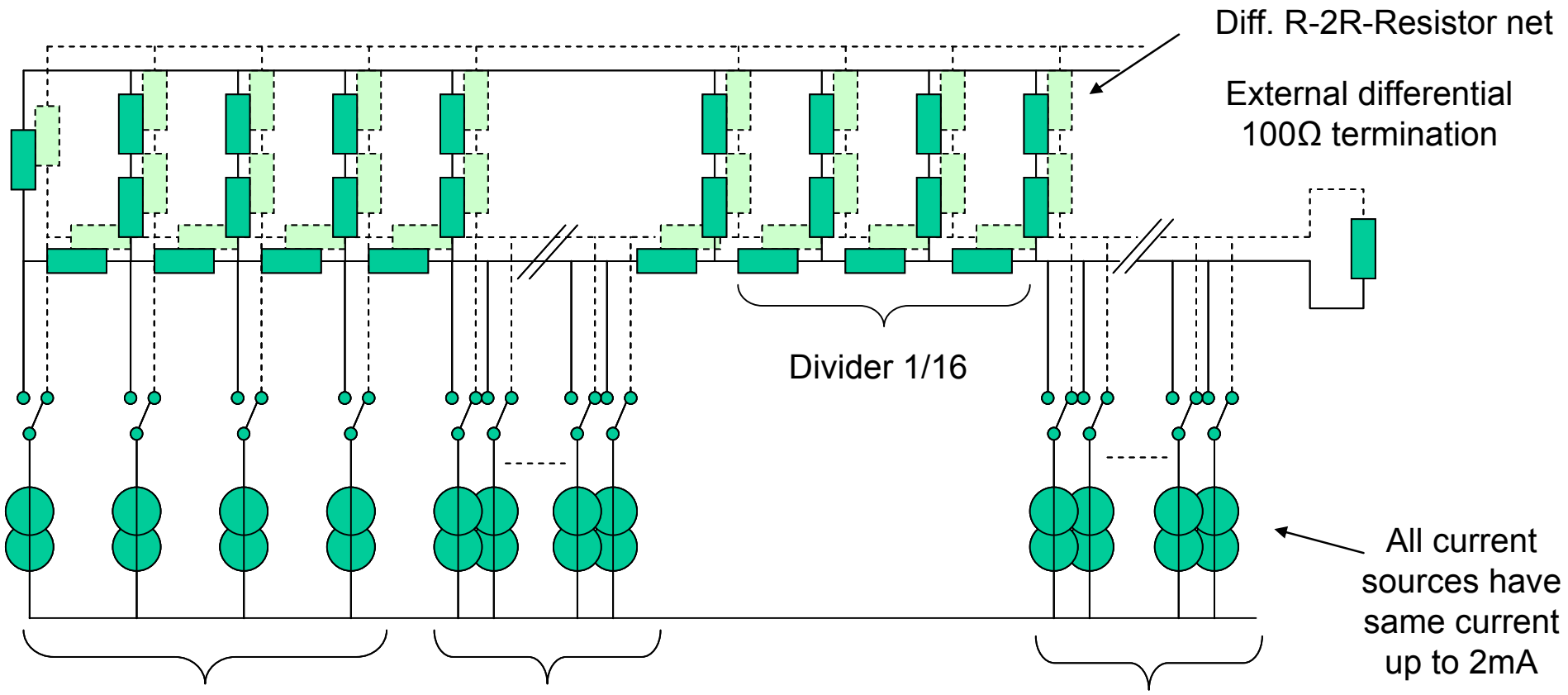
Overall block diagram



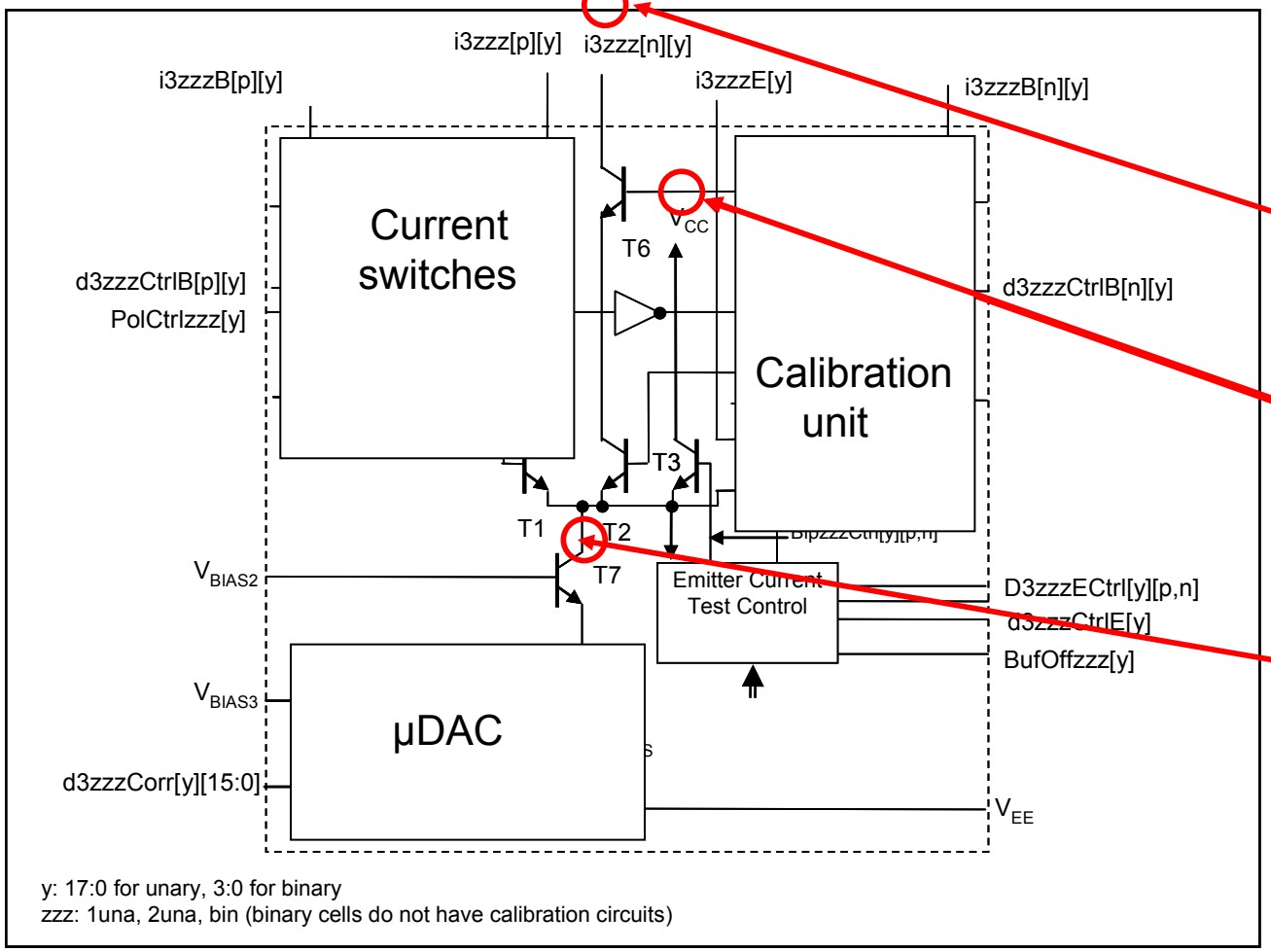

SPI / Ctrl Interface
LVDS + Input Latch
MUX +BIS
Thermometer Decoder + Calibration + Mode Ctrl
Current Switch + Ladder+ Calibration Engine
LSB Ladder
4x12
4
12
4
4
4 binary
unary
Divider 1/16
unary
40 Current Sources driving Ladder
SPI
Digital Channels
Analog Output

Current Switch Output and Ladder Structure:

→ Segmented DAC: 1 Binary Section, 2 Unary Sections



Current Switch Schematic Structure and Tolerances*



*) due to Temperature, Aging and Radiation

Resistor Tolerances of Ladder: matching below 0,5% needed

Base Current of Cascode and Switch Transistors: needed precision 0,5µA

Collector Current of Current Source Transistors : needed precision 0,5µA

Needs sophisticated calibration mechanism

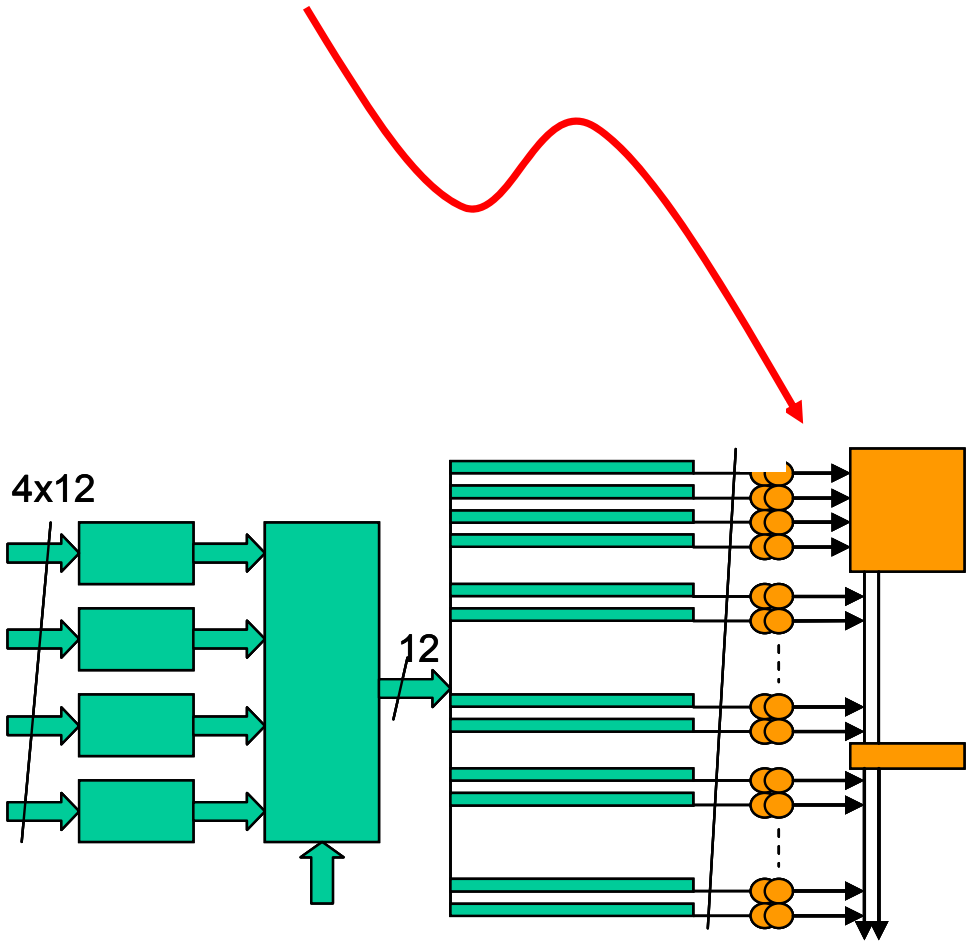
Calibration Mechanism Overview

- Power on calibration:
  - Resistor tolerances are compensated with modified currents of current sources
  - Deviation from nominal current is stored in memory
  - Golden reference current is modified with resistor DAC and memory information
  - All currents are calibrated for minimum output distortion

- Background calibration:
  - A background calibration is necessary to compensate for temperature, aging and radiation degradation during operation (satellite is never switched off!)
  - Background calibration needs synchronous switching between current sources (channels) at full speed (1.5GHz CLK) with minor (analog) signal distortion at output (no or minor glitches)
  - Synchronous switching needs additional digital and analog circuits as well as some additional power

Calibration Mechanism inside the Analog Part

- Base current calibration
- Collector current calibration
- Ladder resistor calibration

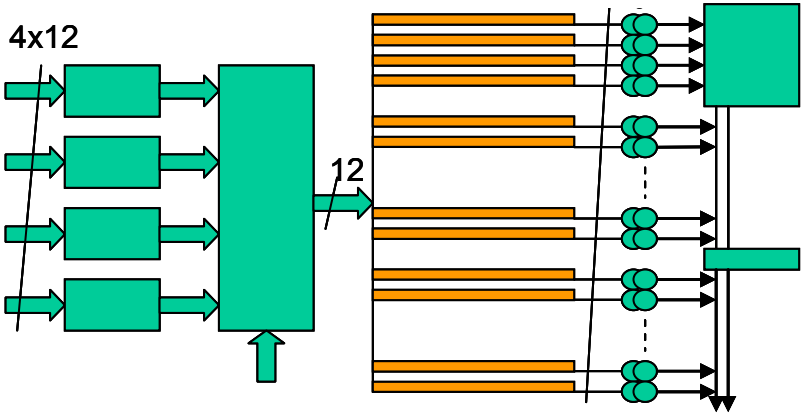


Calibration Mechanism:

- Ladder: Measuring output voltage and adjust each current source accordingly → compensate for resistor matching tolerances
- Measure base Current and add to current source collector current → compensate for base current variations
- Keep collector current constant during operation – adjust µDAC accordingly → compensate for current source variation

Calibration Mechanism: Digital Part

- Binary part will not be calibrated in background mode – only in power up mode
- Two Unary blocks, with each 15 active channels, are calibrated in power up and background mode
  - Spare channels are used for background calibration of base and collector current
  - Channel switch over is done synchronously within digital and analog part of the DAC



Provisions for Radiation Hardness

- All provisions are preliminary until tested and qualified with radiations tests

- Single Event Effects (SEE)
  - Analog and digital circuits are safeguarded by guard rings to reduce radiation induced ionization impacts on circuits and components
  - Bipolar digital circuits (FF) are updated after one CLK cycle (1.5GHz) and thus are not taken as critical
  - CMOS (static) registers use **T**ripple **M**ode **R**edundancy (TMR) → to be checked if good enough
  - CMOS logic is tested and proven on big ASICs (e. g. IHP's LEON processor)

- Total Dose Impacts (TID)
  - Mainly affecting analog degradation: All component and circuit degradations can be calibrated with calibration mechanism – except total failures

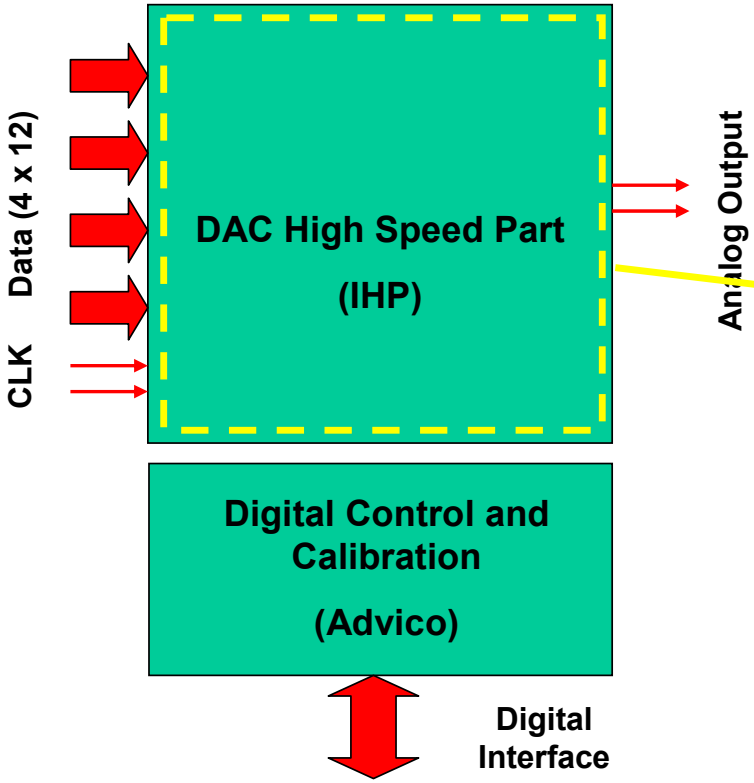
Radiation Related Specification Items

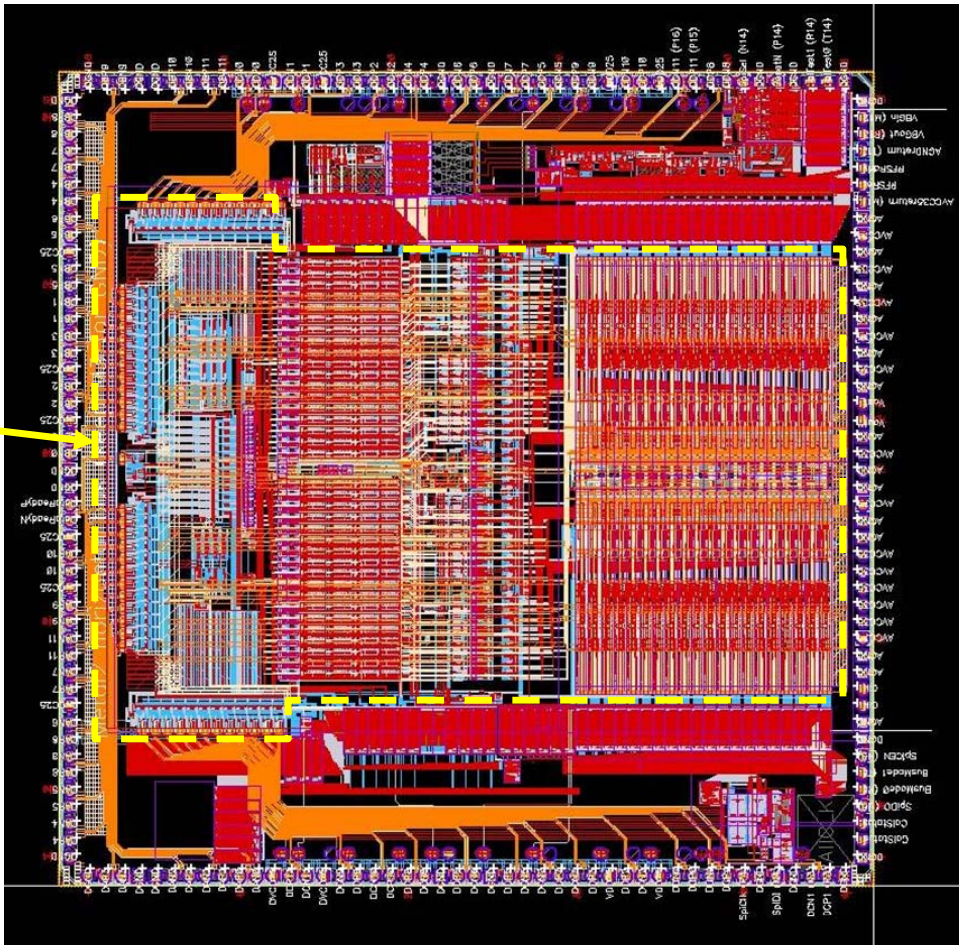
Req. #	Item	Symbol	Conditions	min	max	Unit
DAC-0285	**SE Functional Interrupt induced MTBF**	**SEFI**	**[Recoverable with reset]**	**100 years**		**MTBF**
DAC-0290	**Multiple Conversion Errors MTBF**	**MCE**	**[Self recovering]**	**1 year**		**MTBa**
DAC-0295	**Single Conversion Error MTBF**	**SCE**	**[Self recovering]**	**1 day**		**MTBF**
DAC-0300	**Permanent conversion errors**	**PCE**	**[Recoverable with reset]**	**100 years**		**MTBF**
DAC-0305	**Radiation total dose**			**100**		**krad**
DAC-0310	**Latch up free**			**80**		**MeV-cm2/mg**
DAC-0315	**SEE performance**		**(geosynchronous orbit)**		**10^{-8}**	**bit/day**
DAC-0320	**Useful life**	**t_B**		**20**		**years**
DAC-0325	**Early failure rate**				**2/1000**	**dpm/h**

→ All specifications items are proven only theoretically at the moment

DAC Layout

Chip Design

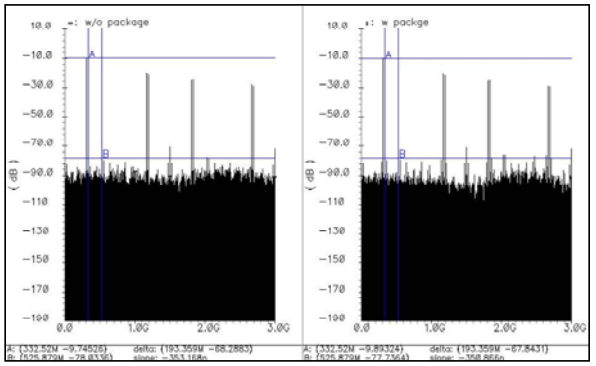




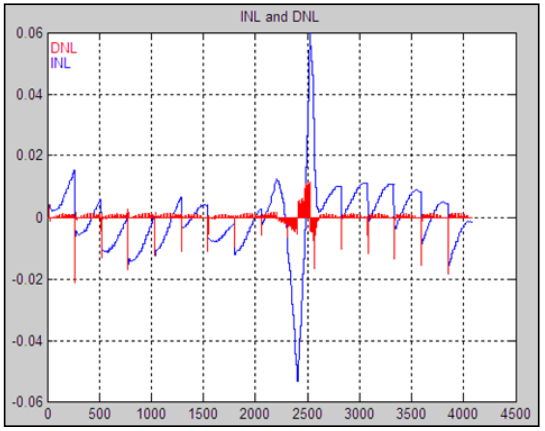
SIMULATIONS

Simulation Results

Multi tone simulation:
2 tones around 300MHz:
- better than -67dBc/-79dBfs
- CLK spur at 71dBfs



- Tape out release from ESA of Prototype 1 achieved in September 2009
- Simulations show specified performance
  - Speed (sampling rate) achieved, 1.5Gsps
  - DAC resolution reached: better than 12 bit
  - SFDR better than -60dB
  - INL and DNL specification reached
  - Calibration mechanism works

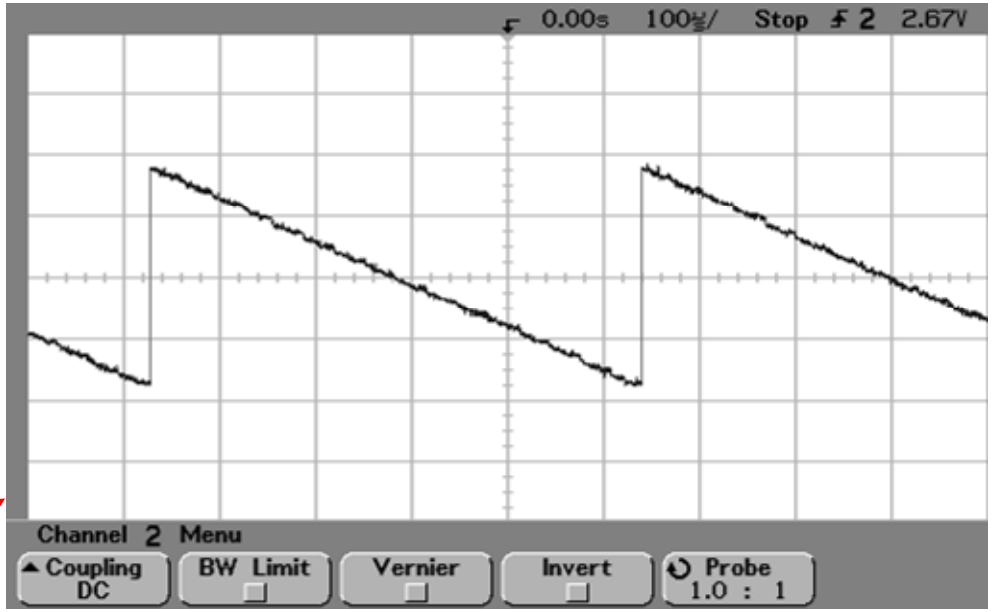


INL/DNL Simulation:
better 0.1 LSB

Test Results

Actual Test Results

- Some test boards built up
- Test equipment installed and operating
- Problems with CMOS logic and programming → under evaluation at Advico and Kayser-Threde
- BIST mode signal derived from internal 12 bit counter successfully tested (uncalibrated)
- Additional test boards are in production



DAC Output in BIST Mode
4096 steps

CONCLUSION

- The DAC contains a calibration circuitry to achieve the required performance.
- The DAC is internally a complex mixed D/A circuit; however for the user it looks like a high performance DAC with excellent robustness against environmental changes, aging and radiation effects.
- The features are high accuracy by consuming less power than non calibrating DACs.
- The calibration allows the analog part to be small.
- The DAC has been manufactured in a Multi Project Waver (MPW) at IHP Frankfurt (Oder) Sept. to December 2009.
  Devices are under test since January 2010.

Thank you for your attention!

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