Galileo RF Receiver

ESTEC Contract 19068/05/NL/JD

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Introduction

- **The project targets are:**
  - Design and manufacture a dual channel RF Front-end for the reception of Galileo/GPS signals
  - Characterize and validate at system level
  - Produce an ASIC including all the necessary Customer Support Services
  - 180nm TSMC CMOS Non Space technology

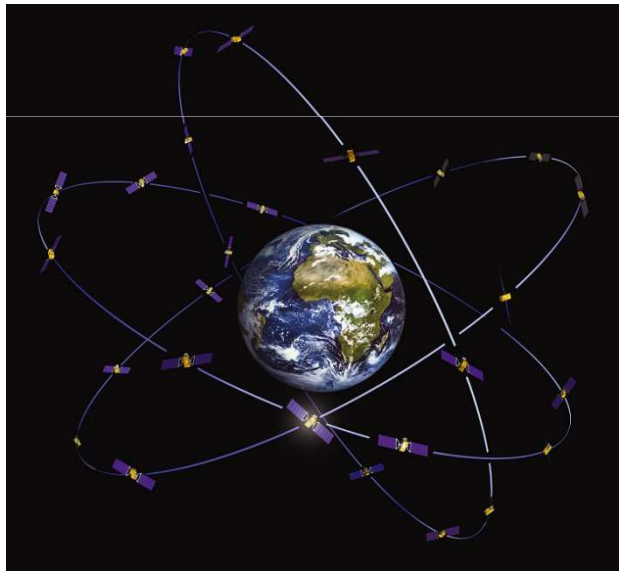
- **Project participants:**
  - Synopsys (IP design house)
  - Septentrio (GNSS receiver manufacturer)

- **Design started in 2005**

- **Three silicon cycles:**
  - Version 1v0 for validating the most critical functions, in RF and baseband
  - Design centering in version 2v0 that was already used for System Validation at sub-contractor facilities
  - Final version 3.0 with full features for product application

Galileo Satellites

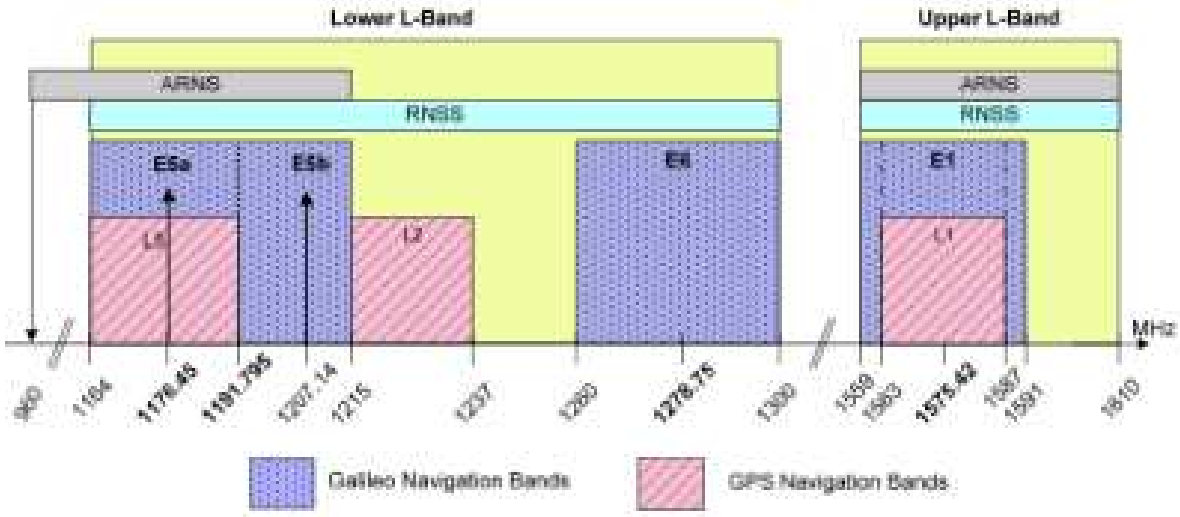
- Giove A was the first launched test satellite on 28th Dec 2005
- Giove B was launched in on 27th April 2008
- Signal analysis of GIOVE-A/B data has confirmed successful operation of all the Galileo signals with the tracking performance as expected
- Contract for building the first 14 operational satellites has been announced on 7th January 2010



→ We need to get ready for the next generation market

Supported GNSS Frequency Bands

- The Galileo navigation Signals are transmitted in four different frequency bands E5a, E5b, E6 and E1
- The corresponding target RF bandwidths vary between 20 and 51 MHz
- Therefore, the RF receiver requires simultaneous tuning to programmable bands and programmable bandwidth
- GPS and Glonass also supported

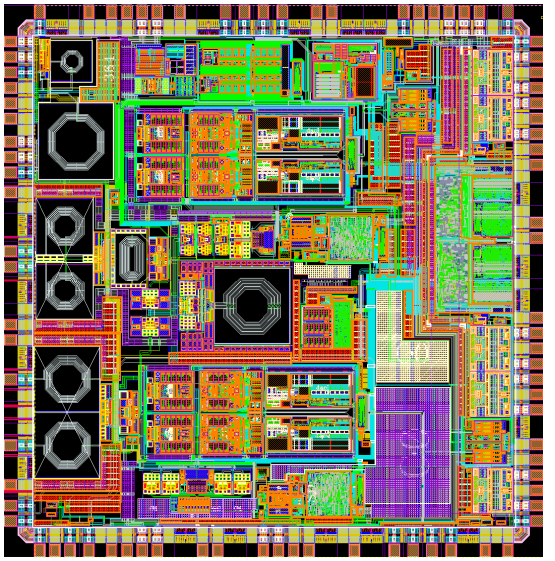


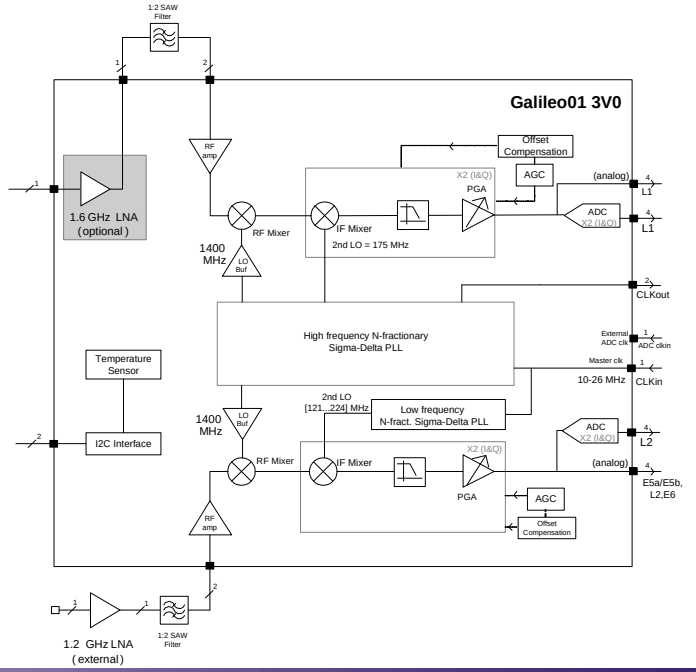
Signal	Carrier Frequency (MHz)
E1	1575.420
E6	1278.750
E5	1191.795
E5a	1176.450
E5b	1207.140

Signal	Receiver Reference Bandwidth (MHz)
E1	24.552
E6	40.920
E5	51.150
E5a	20.460
E5b	20.460

Chip Features

- **Supports Galileo, GPS and Glonass Positioning Systems**
- **Multiple Band Reception E1 / L1 / L2 / E5a / E5b / E6**
- **Dual band simultaneous reception e.g. :**
  - L1 plus L2,
  - L1 plus E5a or L1 plus E5b,
  - L1 plus joint reception of E5a+E5b
  - L1 plus E6
- **Low BOM count**
  - High integration level
  - Fully integrated PLLs including loop filters
  - Digital outputs (CMOS and LVDS)
- **Advanced architecture**
  - Zero IF
  - Embedded DC cancellation loop
  - Automatic Gain Control
- **Onboard temperature sensor for calibrated operation over extended temperature ranges**
- **1.8 V Single Supply ~70mW low power consumption**

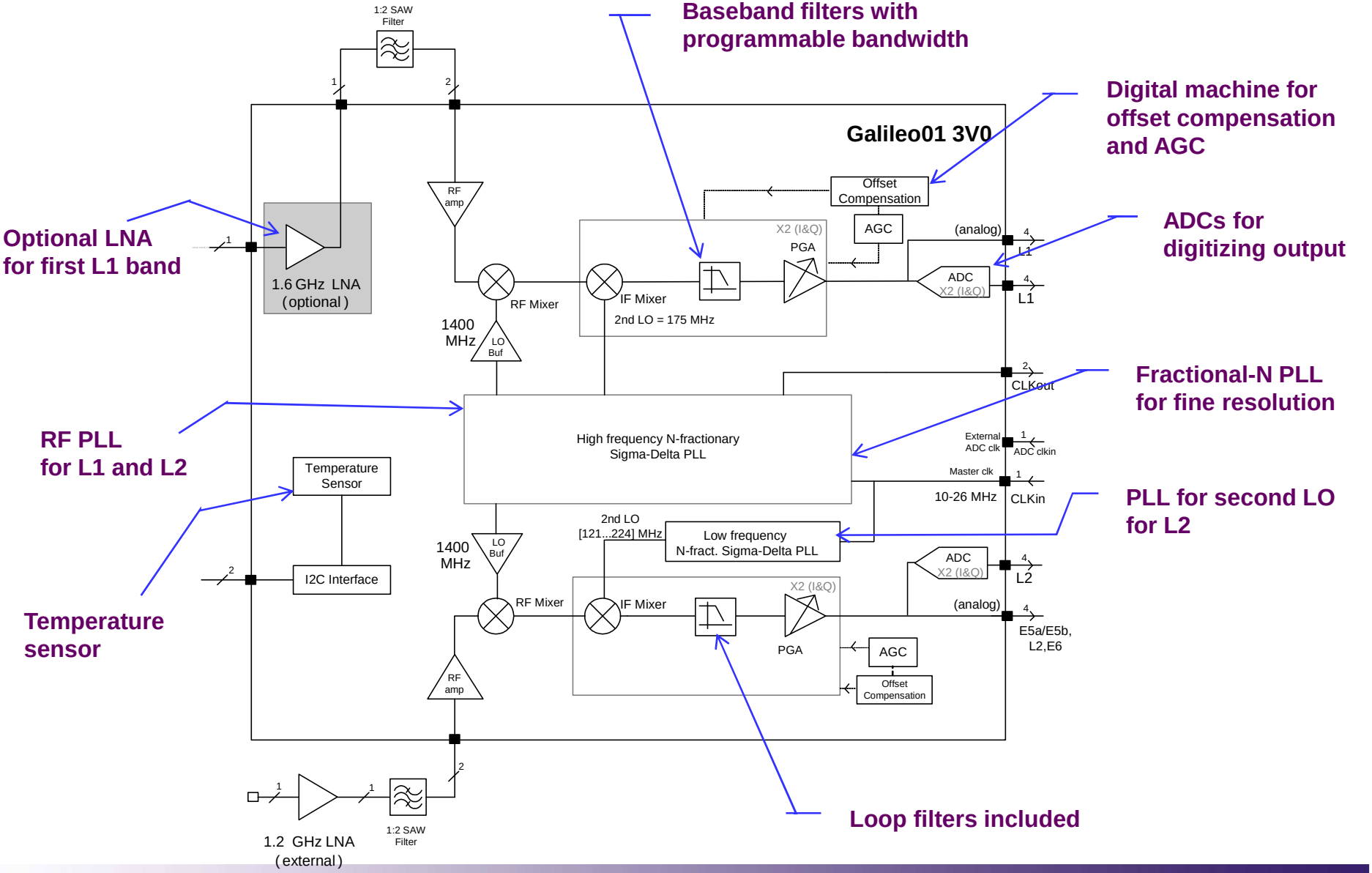




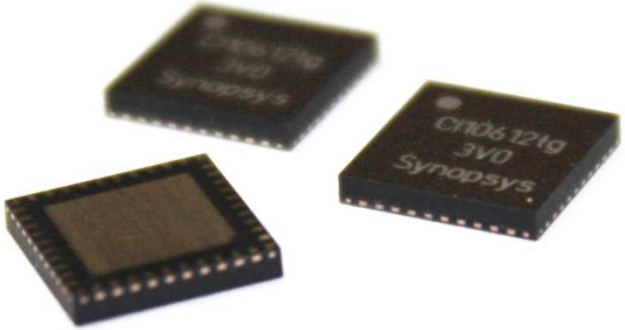
Chip Description

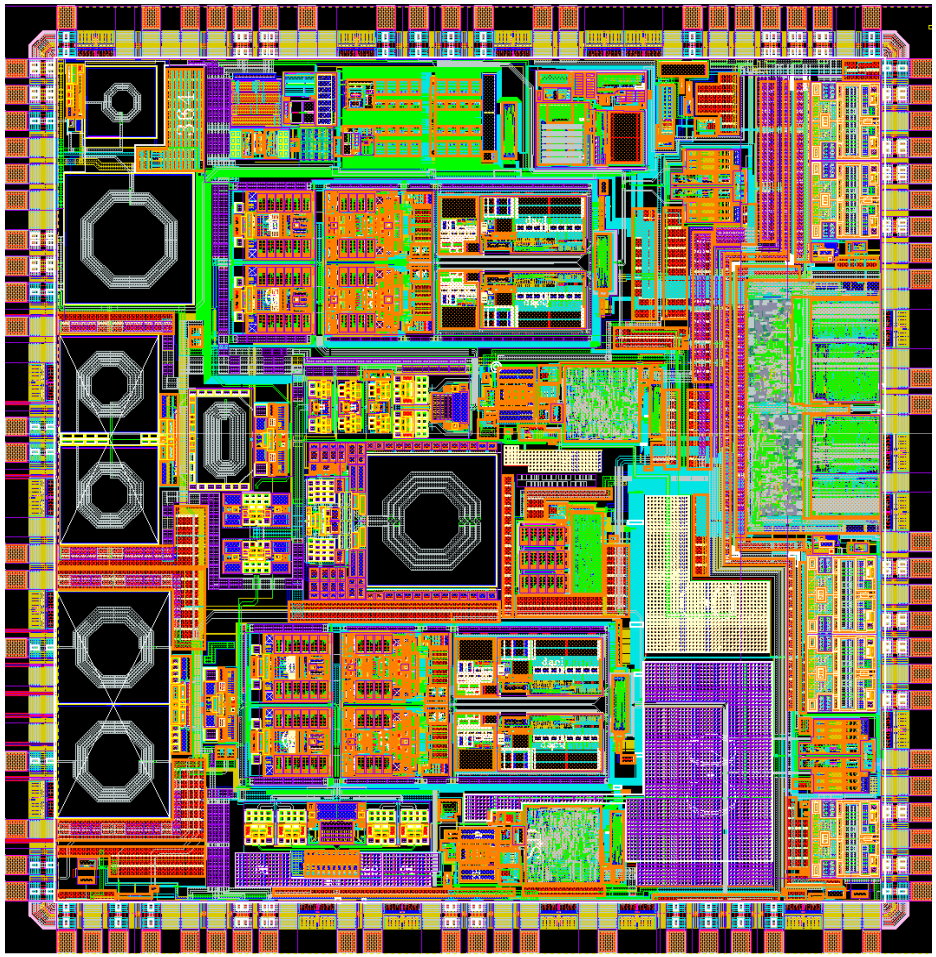
- **Two receiver chains for simultaneous operation in L1 and L2**
  - One receiver chain uses two mixers in a sliding-IF architecture to down-convert the L1 signal, where the second LO is a division by 8 of the RF VCO
  - The second receiver chain uses also two mixers, with an additional PLL to generate the second LO and tunes the L2 signals
  - The RF VCO is shared for both L1 and L2 chains
- **Two external SAW filters (one per chain) recommended for better robustness to out-of-band interferers**
- **2-bit flash ADC (sampled up to 112 MHz) for digital output**
  - CMOS or LVDS output available
  - Analog outputs before the ADC are also available
- **Automatic Gain Control and Offset Compensation of the baseband chain**
- **Temperature sensor for calibrated operation over extended temperature ranges**
- **System control and status monitoring through a serial interface**

Chip Block Diagram



Final Chip





1. Die

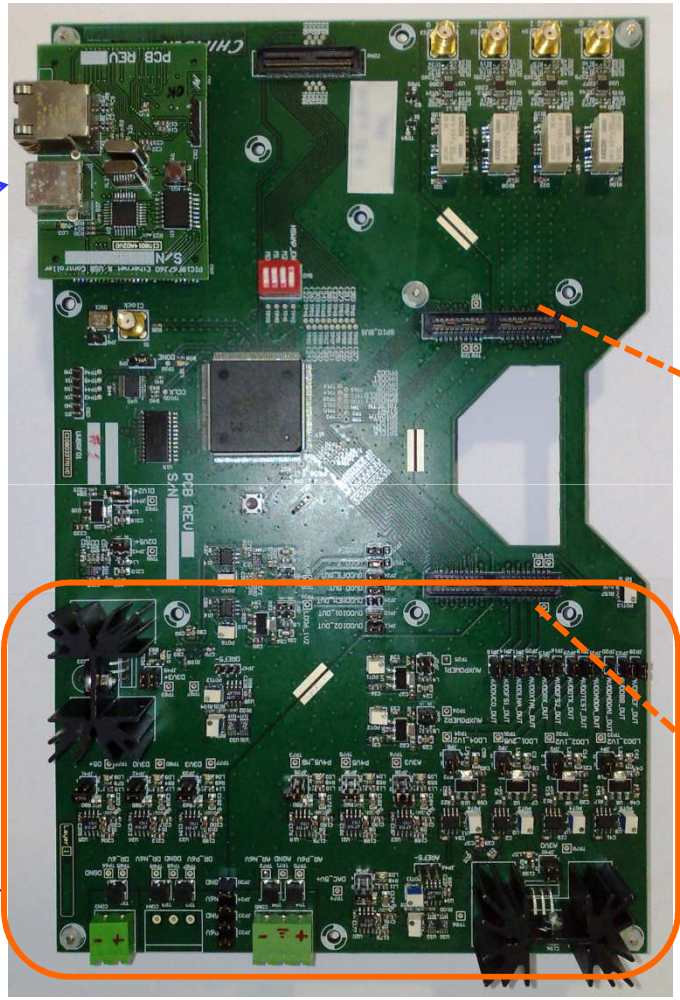
Die external dimensions: l , w , t	2880 x 2850x 0.9 [mm]
Minimum Bond Pad opening area: l , w	53 x 66 [um]
Minimum Bond Pad pitch	80 [um]
Silicon Version	3v0

2. Package

Type	QFN Molded
Number of Pins	**40**
Pin Pitch	0.5mm
Body: l , w	6mm x 6mm
Body Material	Plastic, RoHS Compliant

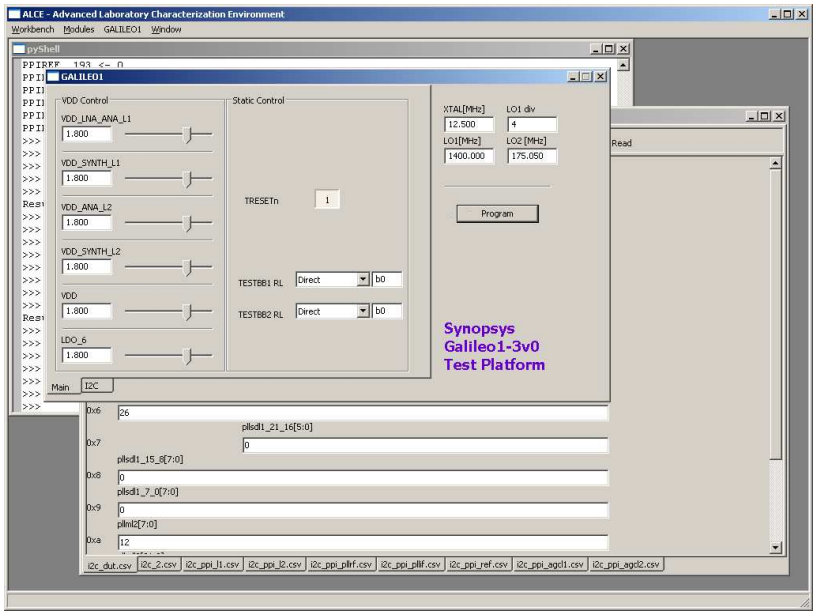
Demoboard

PC USB connection

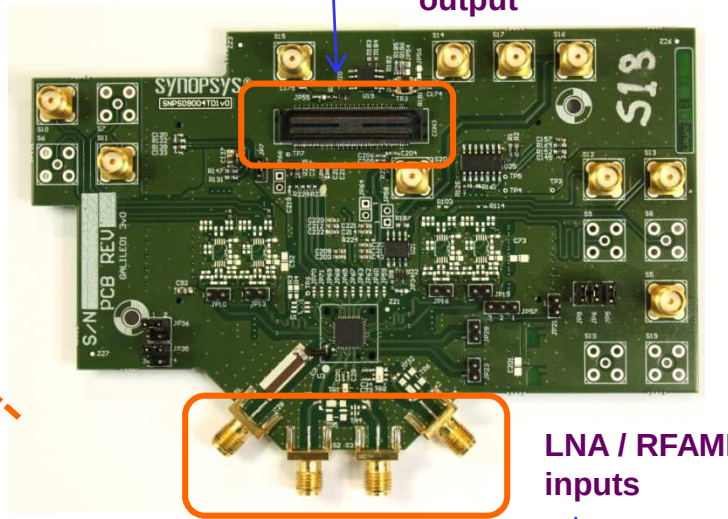


Power Supply Control

Control Software



ADC Digital output



LNA / RFAMP inputs

Current Consumption

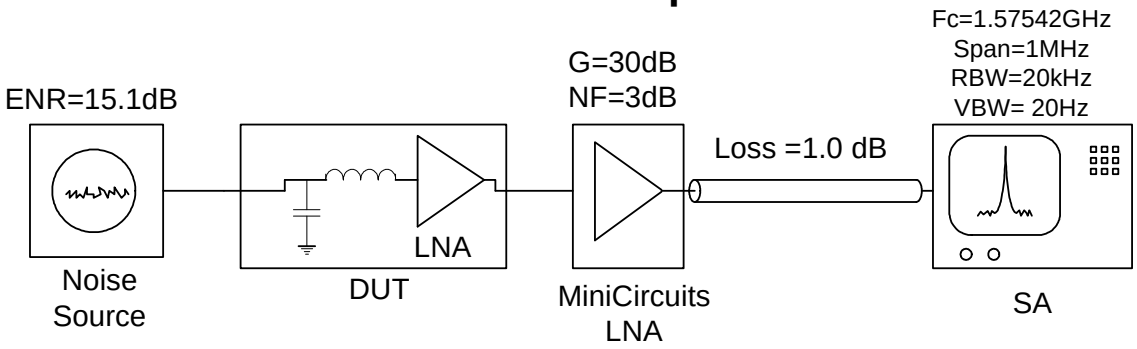
Parameter	Conditions	Consumption	Units
L1 Chain	Analog output	41	mW
L2 Chain	Analog output	31	
Simultaneous L1 & L2	Analog output	60	
Add-on for L1 LNA		5.5	
Add-on for digital output	CMOS	10	
	LVDS	45	

Very low receiver consumption

Added consumption for digital output to support 100 MSps outputs

Noise Figure Measurements

Measurement Set-up for LNA



Parameter	Conditions	Min	Avg	Max	Units
LNA Spot Noise Figure	Spot - Frequency 1575.58MHz	1.77	1.86	1.95	dB

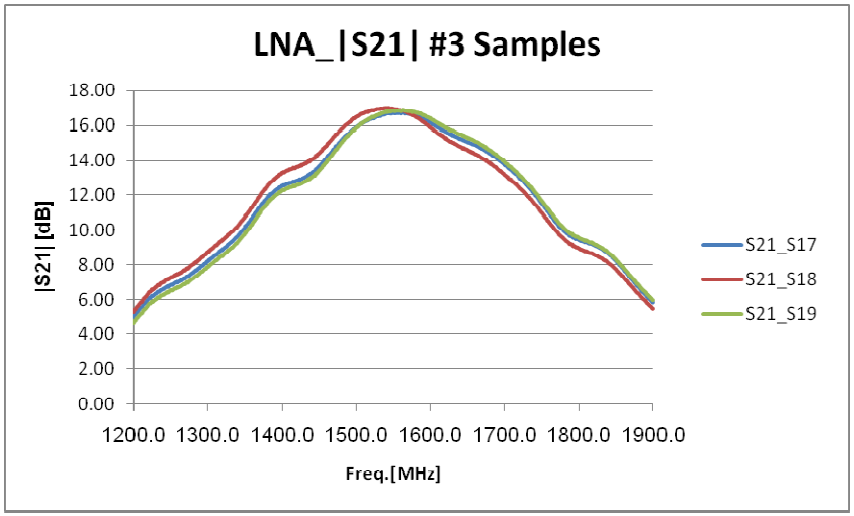
Parameter	Conditions	Min	Avg	Max	Units
LNA to BaseBand, Spot Noise Figure	Spot - Frequency 1577MHz	2.37	2.54	2.64	dB

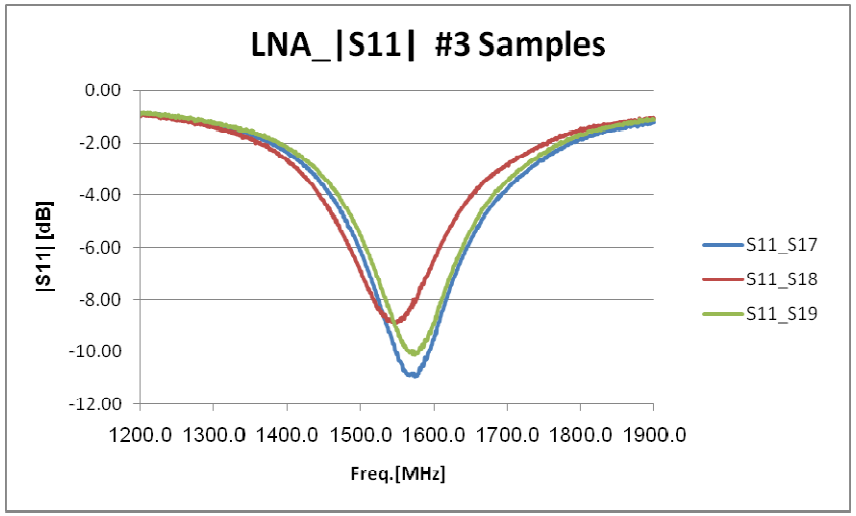
Better than 2.6dB for complete chain

Parameter	Conditions	Min	Avg	Max	Units
Noise Figure L1 band	Mixer input 1577MHz	6.5	6.7	6.9	dB
Noise Figure L2 band		7.2	7.4	7.6	

LNA S-Parameters

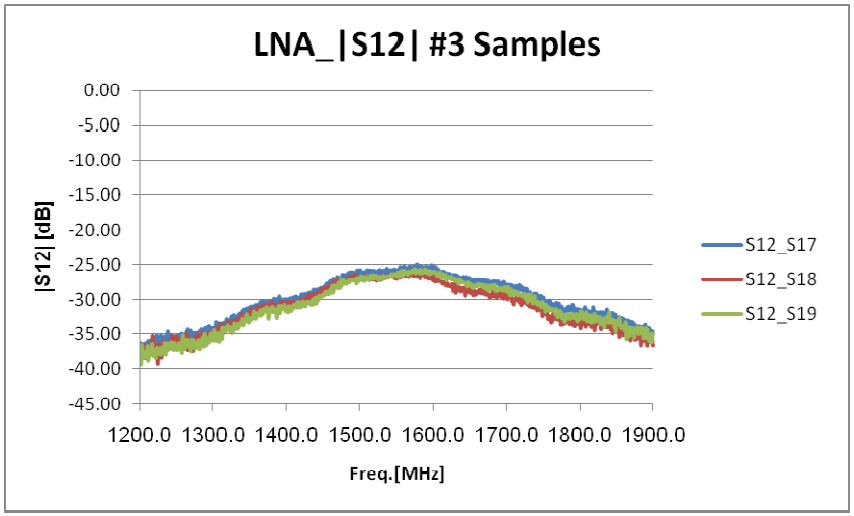
Parameter	Conditions	Min	Avg	Max	Units
LNA Gain (S21)	LNA input matched (Cp=2.4pF, Ls=9.8nH) @ 1575MHz	16.6	16.7	16.8	dB
LNA (S11)		-8.0	-9.5	-10.9	

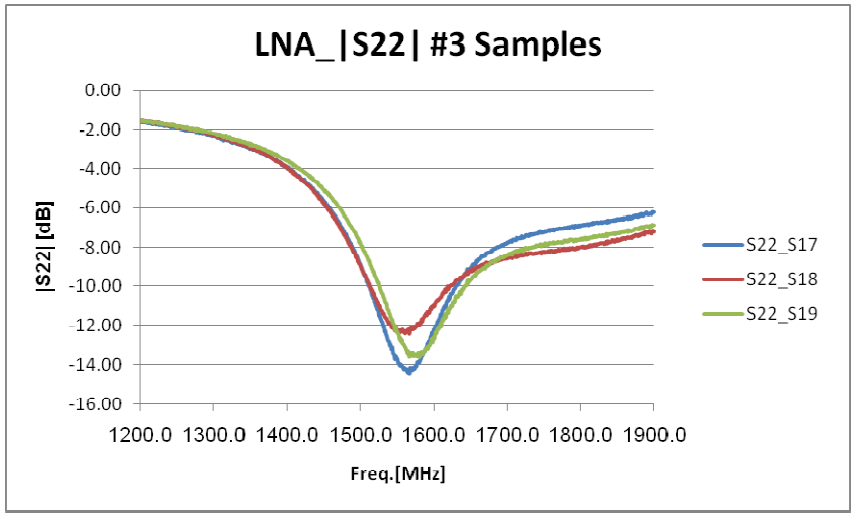




LNA S-Parameters

Parameter	Conditions	Min	Avg	Max	Units
LNA (S12)	LNA input matched (Cp=2.4pF, Ls=9.8nH) @ 1575MHz	-25.3	-26.0	-26.6	dB
LNA (S22)		-12.0	-13.1	-14.0	





Chain Gain without LNA

Parameter	Conditions	Min	Avg	Max	Units
Gain Max L1 band	PGA1,2 Gain=24+24 dB	92.3	93.8	94.9	dB
Gain Default L1 band	PGA1,2 Gain=12+12dB	70.2	71.4	72.3	
Gain Min L1 band	PGA1,2 Gain=0+0dB	44.7	45.9	46.4	

Parameter	Conditions	Min	Avg	Max	Units
Gain Max L2 band	PGA1,2 Gain=24+24 dB	89.1	91.1	92.4	dB
Gain Default L2 band	PGA1,2 Gain=12+12dB	65.9	67.2	68.2	
Gain Min L2 band	PGA1,2 Gain=0+0dB	41.5	42.6	43.3	

Including 16 dB in LNA, total chain gain achieves above 110 dB

IIP3 and 1dBCP Measurements

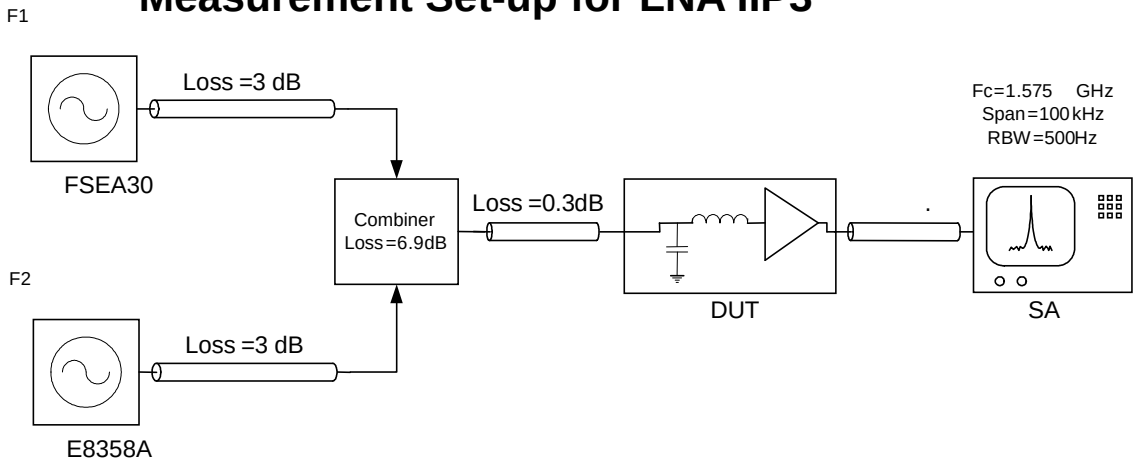
Parameter	Conditions	Min	Avg	Max	Units
IIP3 LNA	LNA input matching Cp=4.7pf and Ls=9.8nH	6.78	7.37	7.78	dBm

Parameter	Conditions	Min	Avg	Max	Units
IIP3 RF_Amp to PGA L1 Band	PGA1,2 Gain = 0+0 dB	-18.81	-18.15	-17.83	dBm
IIP3 RF_Amp to PGA L2 Band		-32.94	-32.73	-32.48	
1dBCP RF_Amp to PGA L1 Band		-63.50	-63.06	-62.80	
1dBCP RF_Amp to PGA L2 Band		-59.50	-59.22	-58.80	

Settings:

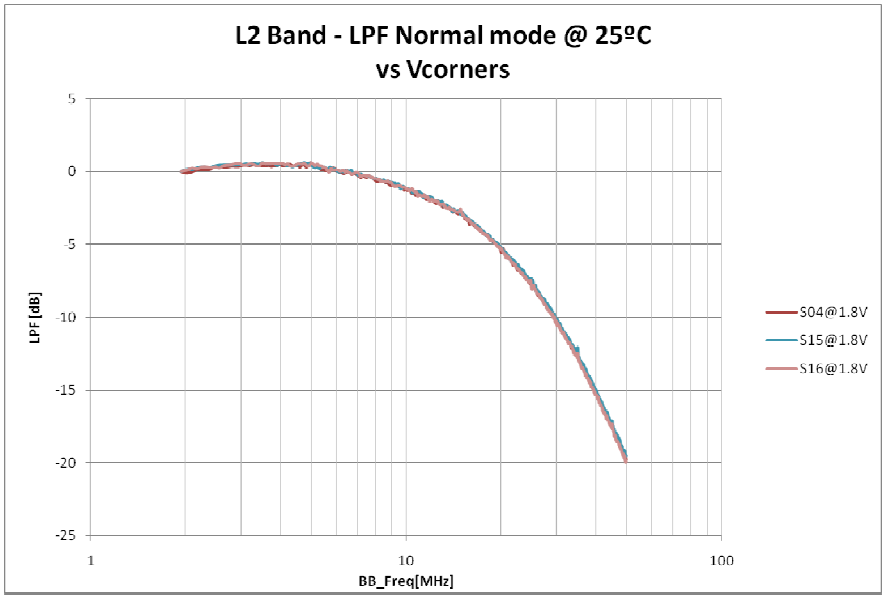
RFin=1575.42MHz.
RFin Interferer1= 1805.14MHz.
RFin Interferer2= 2034.86MHz.
RFin Interferer level = -30dBm

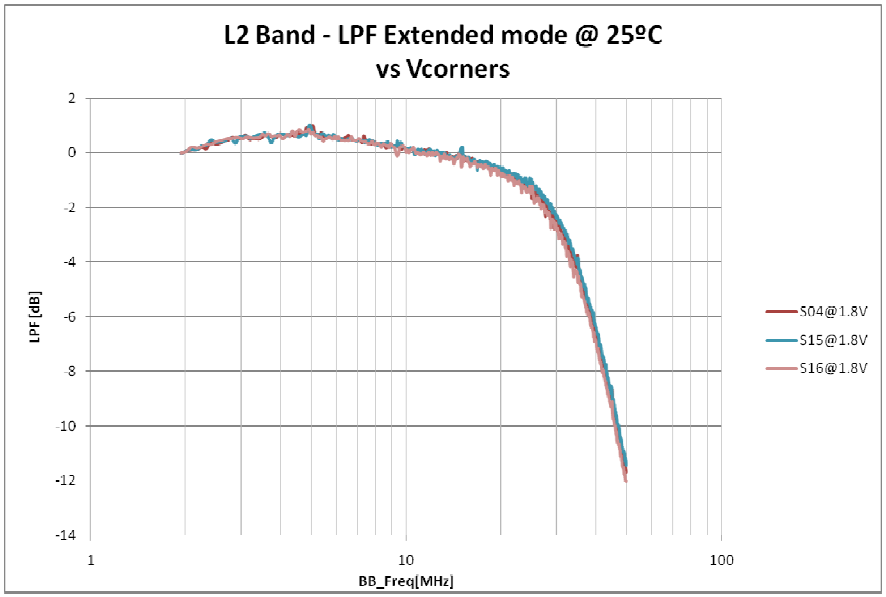
Measurement Set-up for LNA IIP3



Baseband Filters

Parameter	Conditions	Min	Avg	Max	Units
L2 LPF Bandwidth Normal Mode	PGA1,2 Gain=12+12dB	14	14	14	MHz
L2 LPF Bandwidth Extended Mode		29	29	29	





Bandwidth programmability for all Galileo bands including E6

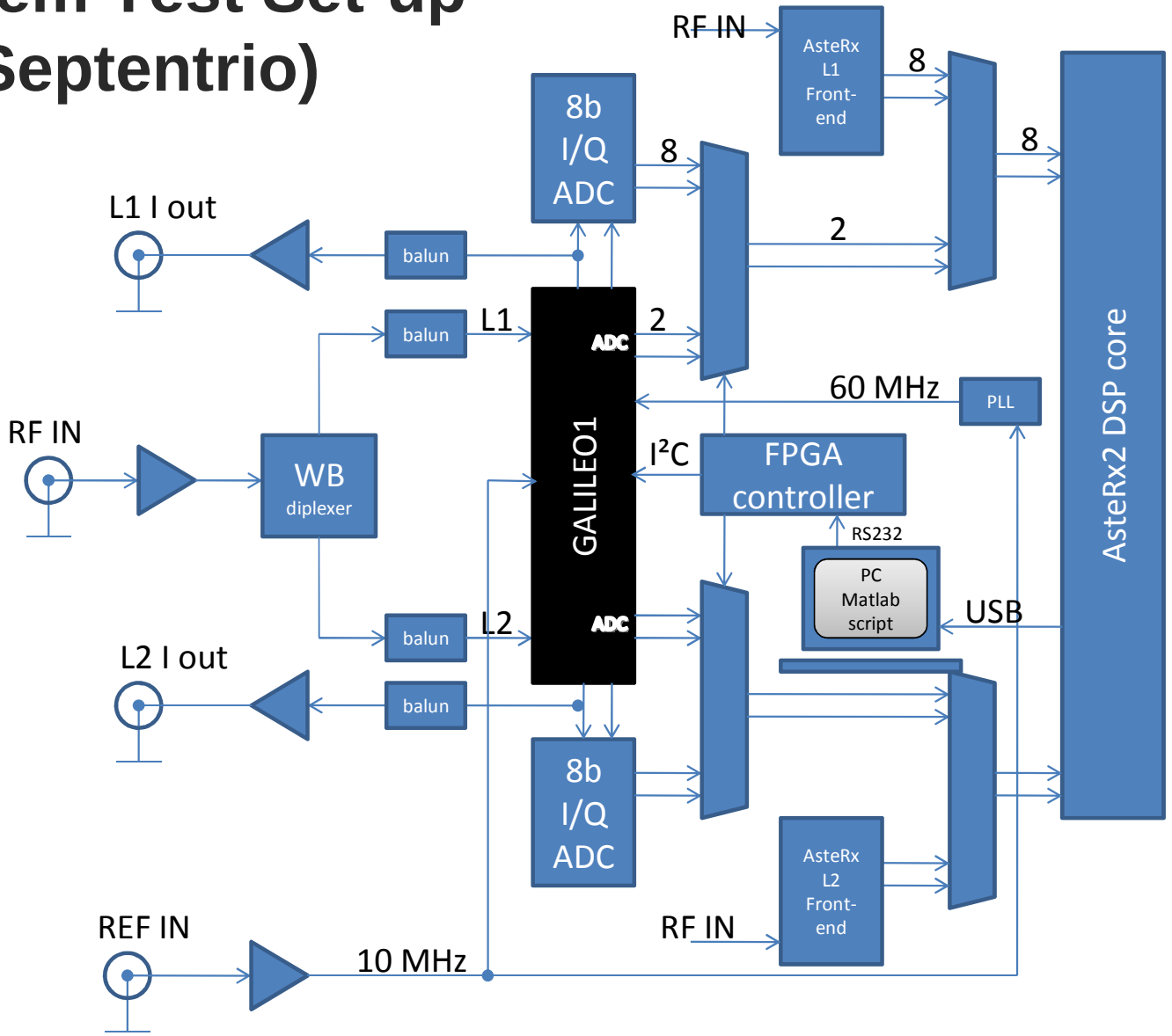
Phase Noise Measurements

Parameter	Conditions	Offset [kHz]	Min	Avg	Max	Units
PLL_L1 **Phase Noise (Down connversion)**	PGA1,2 Gain = 0+12 dB	10	-73.97	-73.34	-72.97	dBc/Hz
		100	-81.84	-81.66	-81.43	
		1000	-105.85	-105.69	-105.52	

Parameter	Conditions	Offset [kHz]	Min	Avg	Max	Units
PLL_L2 **Phase Noise (Down connversion)**	PGA1,2 Gain = 0+12 dB PLL2=121.62MHz	10	-74.90	-73.83	-73.06	dBc/Hz
		100	-74.70	-74.46	-74.17	
		1000	-102.05	-101.94	-101.74	
	PGA1,2 Gain = 0+12 dB PLL2=192MHz	10	-72.24	-71.90	-71.67	
		100	-74.66	-73.77	-72.93	
		1000	-102.83	-102.62	-102.43	
	PGA1,2 Gain = 0+12 dB PLL2=223.92MHz	10	-71.68	-70.76	-69.58	
		100	-74.64	-73.92	-73.25	
		1000	-102.47	-102.44	-102.41	

Always below -100dBc/Hz at 1MHz offset

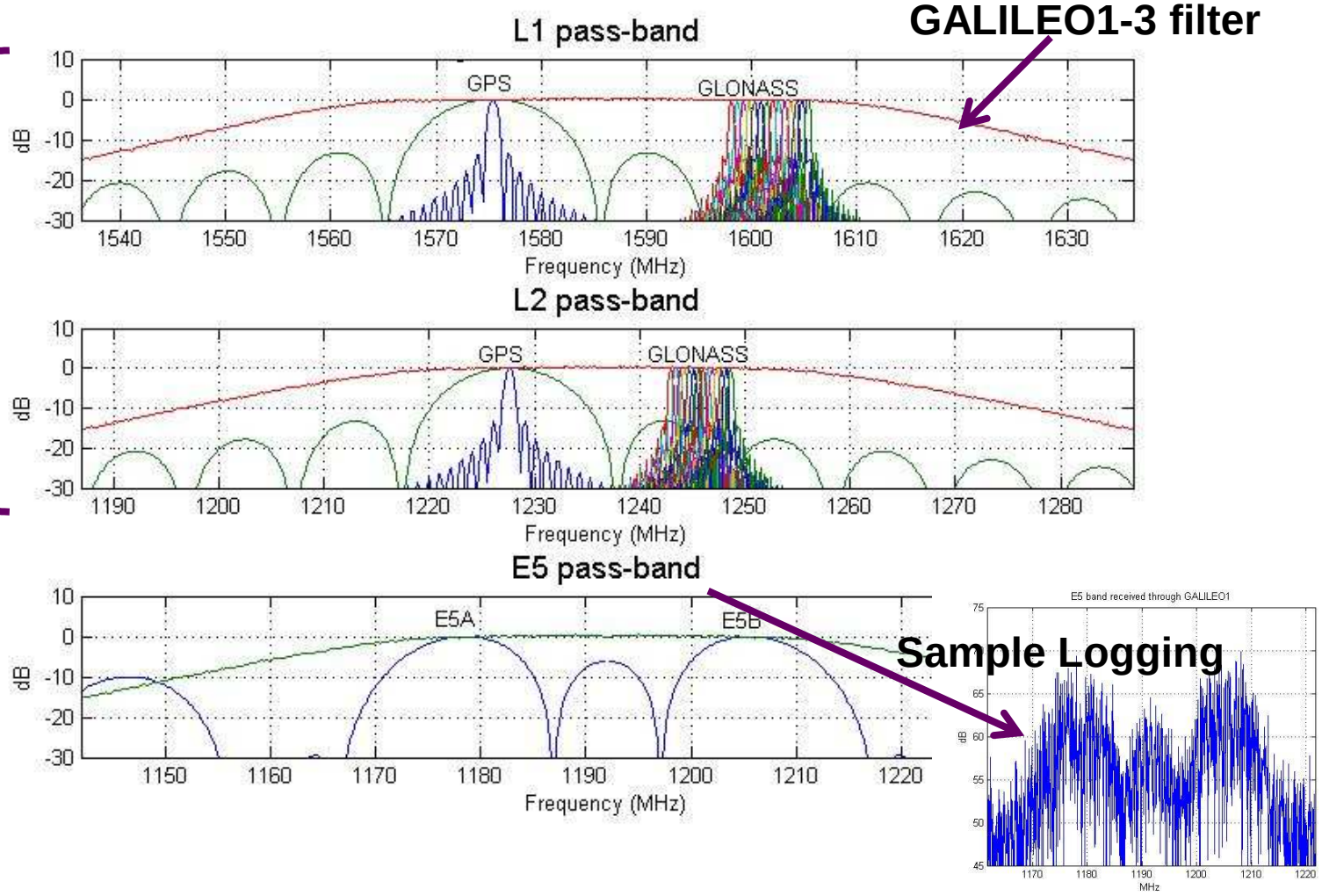
System Test Set-up (at Septentrio)



System Test Set-up, at Septentrio

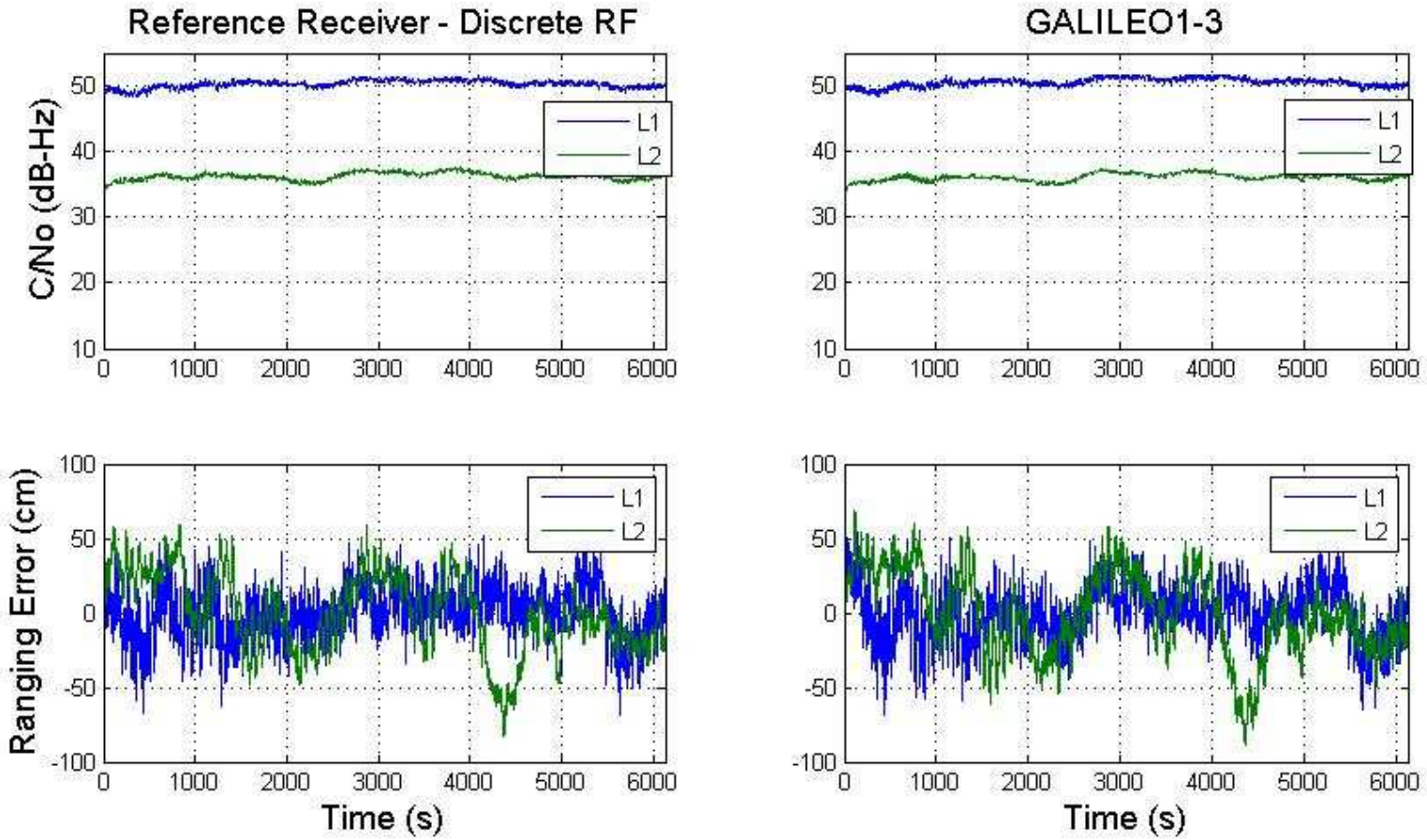
Two Bands Through one Channel

Configuration used in tests



GPS/GLONASS Configuration

- C/No and ranging performance

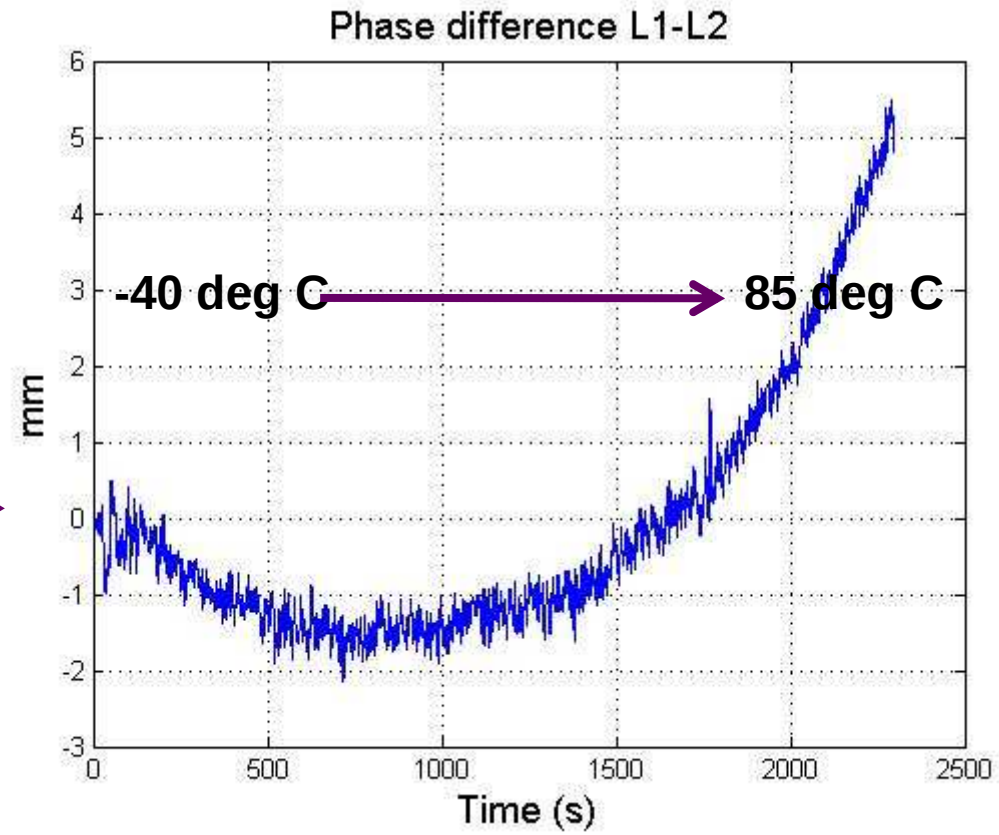


Temperature Stability

- **Excellent Stability of GNSS parameters (C/No, GD,...) for [–40, +85] ºC sweep**

Spirent
RFCS

Thermal Chamber



Conclusions and Next Steps

- **Silicon Characterization is complete**
  - Design is on-spec, no further redesign needed
- **System Validation is complete**
  - Design can be used in a production receiver – no showstoppers identified
  - Very good synthesizers – L1/L2/L5 without issues
  - Good interference isolation from internal ADC, even with CMOS output
  - Very low power dissipation
- **Next Steps**
  - Engineering Golden Samples
  - Volume Test
  - Qualification
  - Manufacturing and Product Engineering
  - Cost Model and Ramp-up Outlook

Questions?