# DSM ASIC Technology & HSSL (KIPSAT)

**Presented by**

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# OUTLINE

- Need for DSM 65nm
- Key IPs
- KIPSAT project phases/status
- Results
- On-going work
- Perspectives
- Conclusion

# Space needs DSM 65nm 1/2

- New Telecom Satellites need:
  - More channels
  - More data throughput
  - Less power
  - Less weight

- Answer:
  - High integration technology
  - High speed capability with low power
  - Mandatory Serial Links IP with > 5Gbit/s rate

# Space needs DSM 65nm 2/2

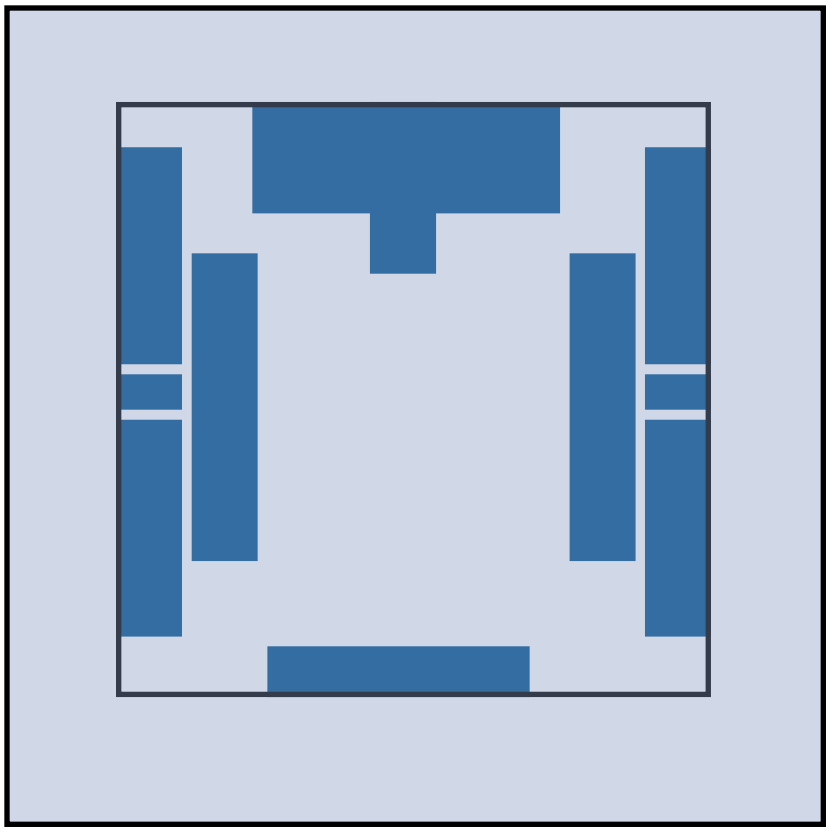
- Target Specs:
  - 10-30 Mgates
  - Low power
  - SerDes IP
  - Non ITAR
- ST 65nm offers:
  - 750 Kgates/mm2
  - 5.7nW/(MHz.gates)
  - Telecom ASICs with many 6.25-7.5GBit/s links.
  - European technology

+ Space specific requirements:

Long term and radiations Robustness

Viable Business Model with low volumes

# Key IPs



- High Speed Serial Link (HSSL or SerDes)
  - Replaces multiple wires by a single cable
  - Reduces ASIC pin-count
  - Optimizes data-throughput, power and Bit-Error-Rate
- LVDS I/Os
  - Allows to connect ADC/DACs or other ASICS from various technology
  - Low noise sensitivity and EMI generation

# KIPSAT project phases

- Contract ESA, ST prime with TAS, Astrium, ISD as partners

- Phase 1A
  - Technology Assessment
  - Design for Robustness methodology
  - HSSL IP selection
  - Quad-HSSL specifications

- Phase 1B
  - Quad-HSSL design and manufacturing of cut1
  - Library development plan for future ASICs
  - Electrical validation
  - Preliminary Radiation and Reliability evaluation

# KIPSAT status

- Phase 1A fully completed
  - No blocking issue to use ST 65nm for Space
  - Robustness maximization techniques defined
  - Preliminary tests anticipated on HSSL test vehicles
- Phase 1B started
  - Quad-HSSL “Quatuor” Design completed next April
  - Quatuor evaluation-board co-designed with ISD
  - Libraries needs analysis for future ASICs on going
  - Quatuor tests planned Q4-2010

# Results

# KIPSAT results

- 65nm Reliability:
  - ST Process Qualification Report was intensively reviewed by ESA, CNES and end-users reliability Experts.
  - No blocking issue among known Failures Modes:

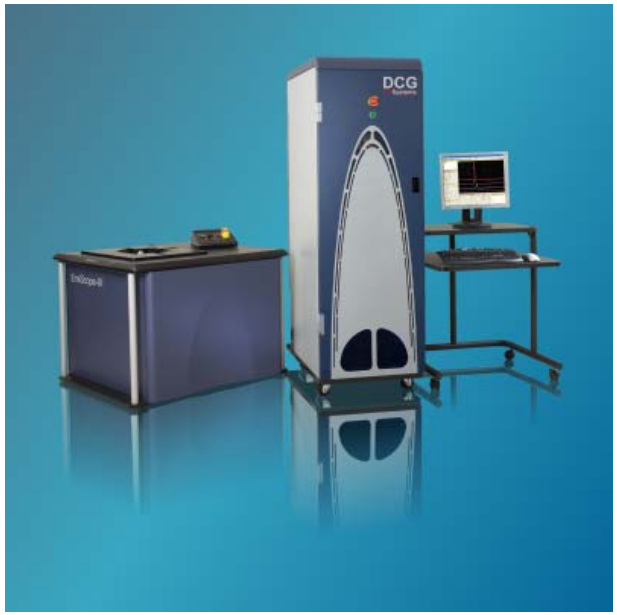
  EM, NBTI, HCI, SGR, TDVB, …
  - ST Design Kit offers Design-In-Reliability models to run simulations with contextual impact of ageing.
  - Future libraries with 20years ageing data are considered (10years today available).

# KIPSAT results

- 65nm under Radiations:
  - 2005-2007 radiations tests campaigns (ESA contracts) results on ST 130nm/90nm/65nm were reviewed in 2008 by ESA, CNES, end-user and ST Experts (Philippe Roche team for ST).
  - 65nm radiation assessment KIPSAT deliverable covers TID, Protons and Heavy Ions on large SRAM test vehicles + FlipFlop registers with hardened clock trees.
  - $10^{E}$-7 to $10^{E}$-8 cm2/bit  Cross-Section depending on cells type and patterns
  - TID shows no current increase up to 100Krad(Si)
  - No SEL up to 85MeV/mg/cm2, max Supply, 125°C Tj. With design option.
  - Mitigation techniques/methodologies described in a KIPSAT deliverable, being applied to Quatuor design.

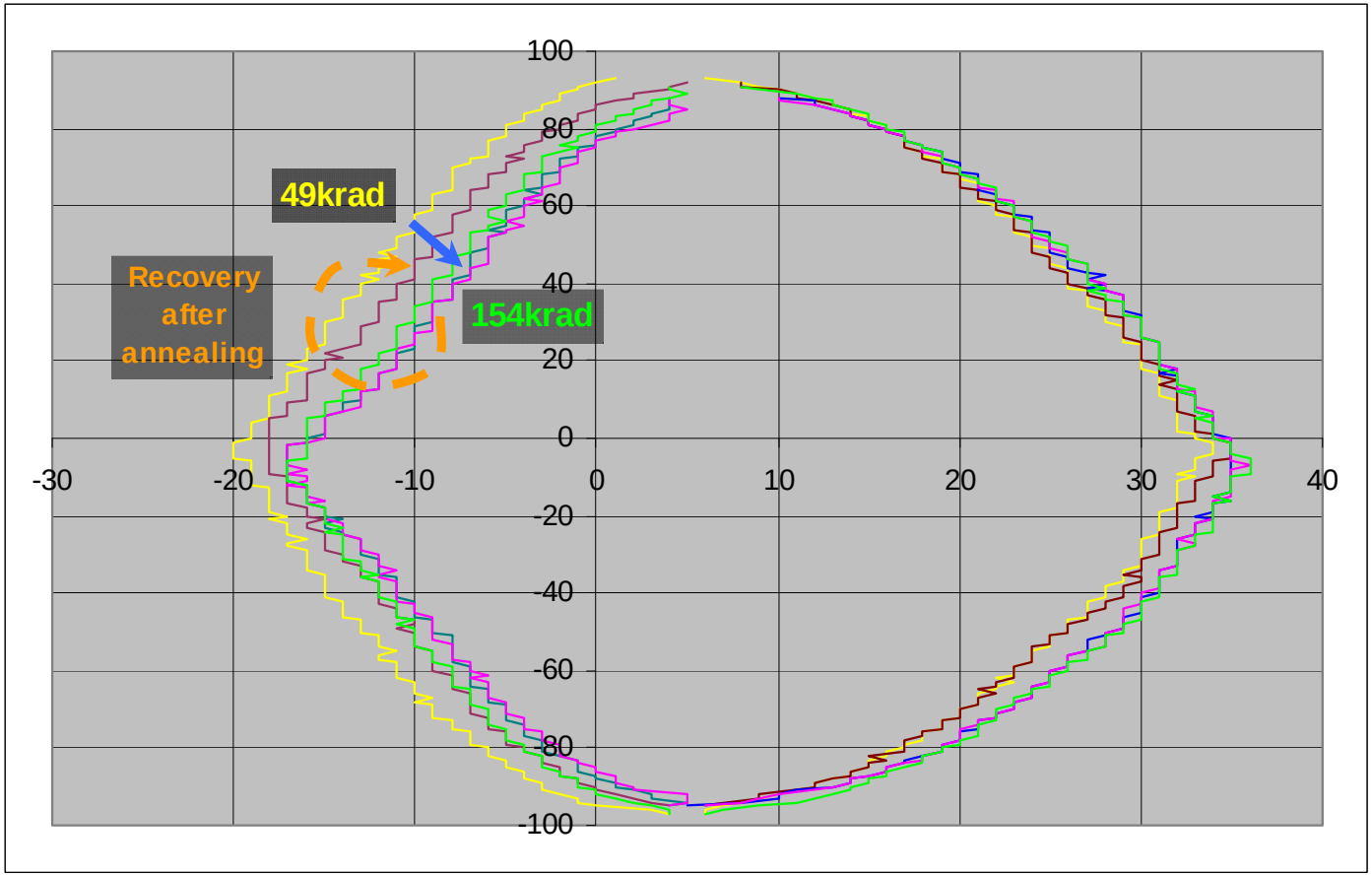
# KIPSAT results

- Extra measurements:
  - TID measurement on “native” HSSL test-chip
  - Heavy Ions exposure of SF
  - Laser tests on SF:



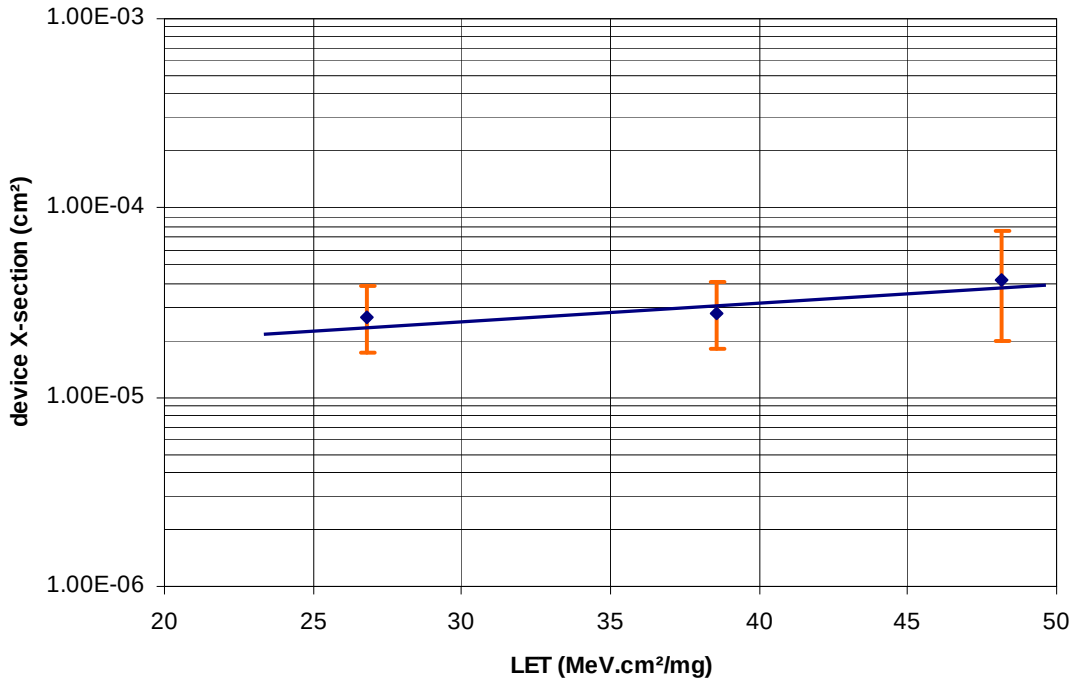
# TID test result on “native” HSSL

- TID up to 210krad(Si) at ENEA, Nov-Dec2009.
  - Small drift observed on inner eye measurement:



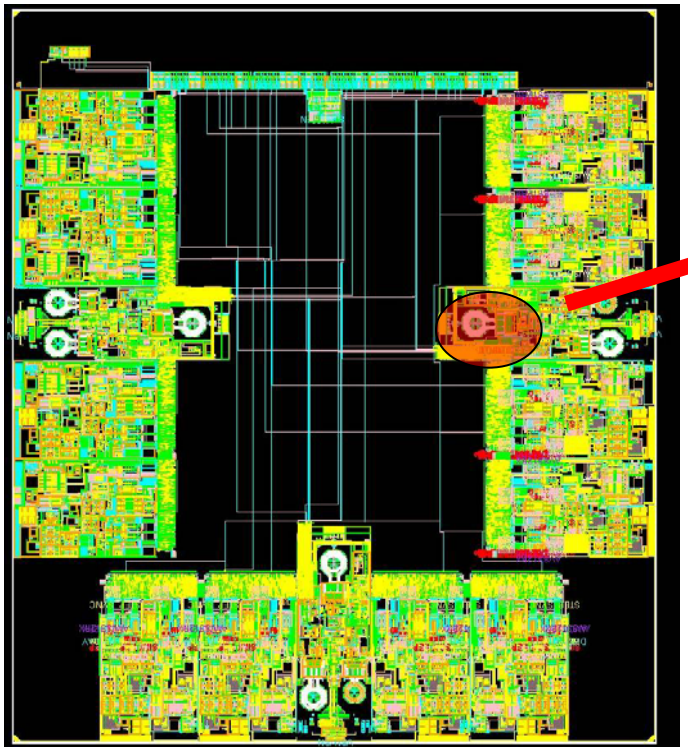
# Heavy Ions on “native” HSSL

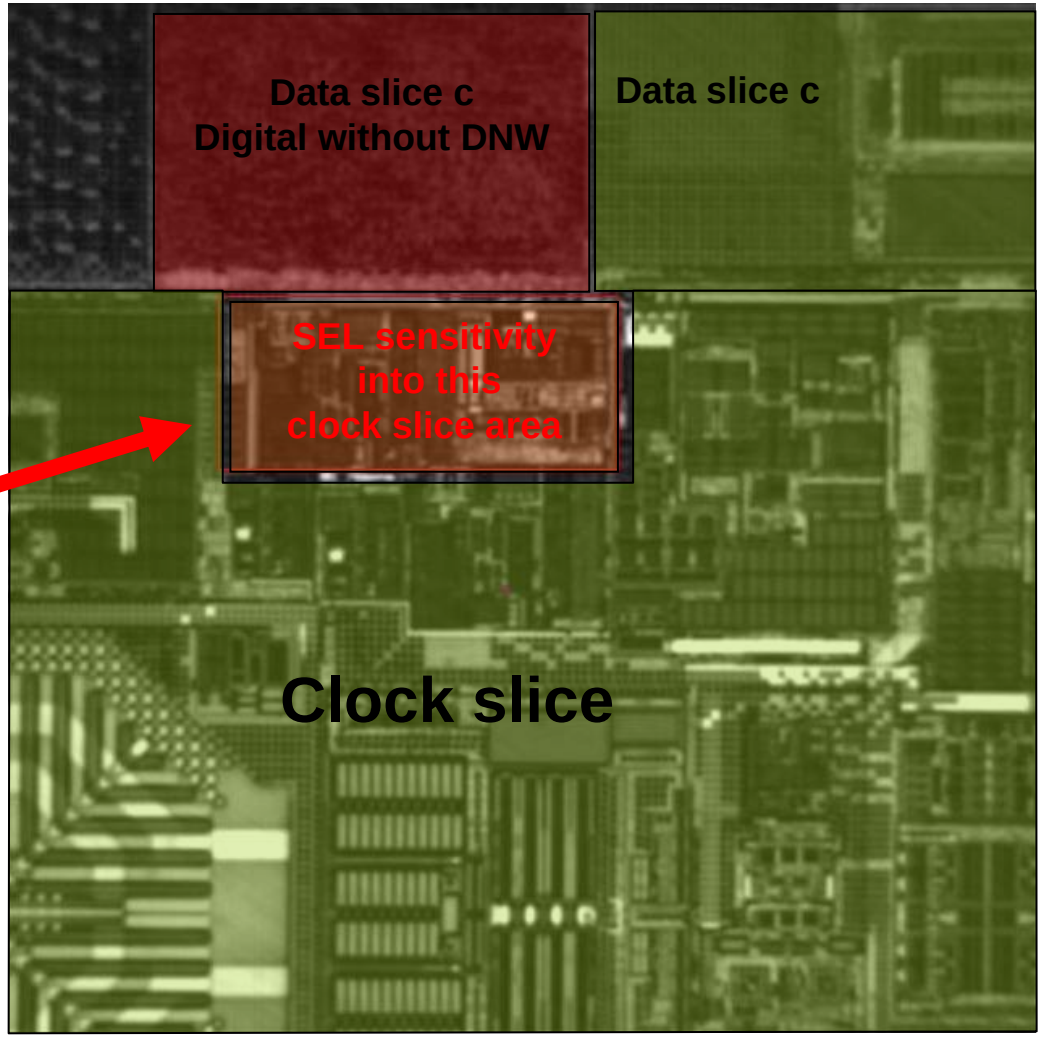
- Preliminary Tests ran @ GANIL Caen, F.
  - SEL observed but foreseen on 1.2 volt supply
  - No SEL below 1 volt on 1.2 volt power supply
  - Tentative Cross-section:



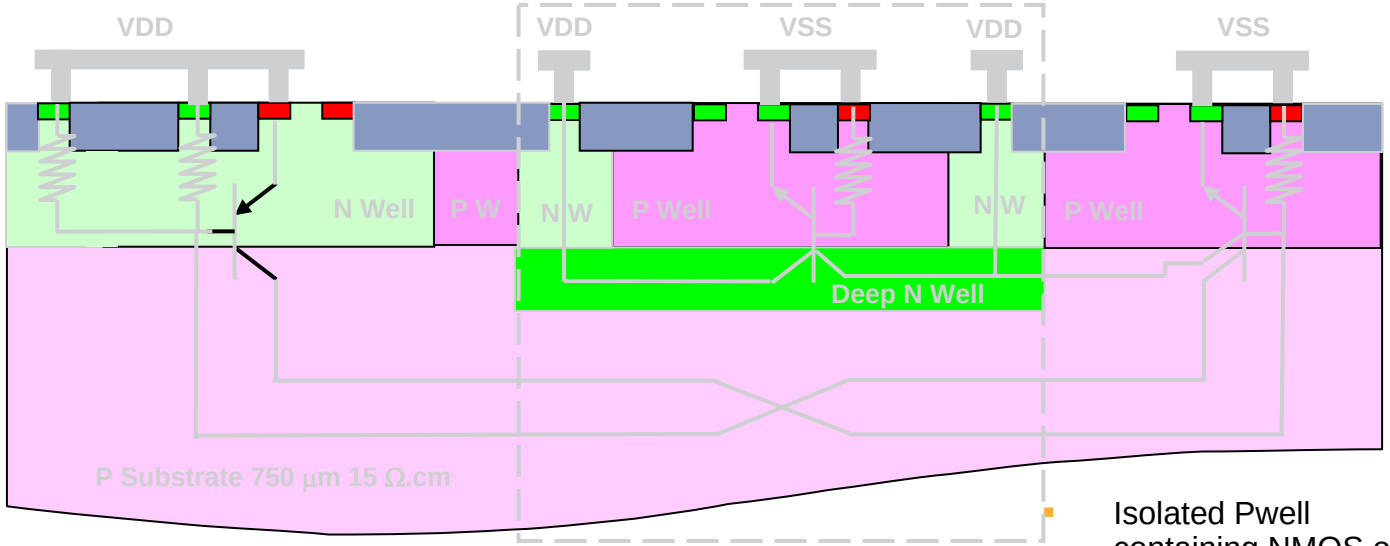
# SEL localization by Laser test

Native HSSL TV:

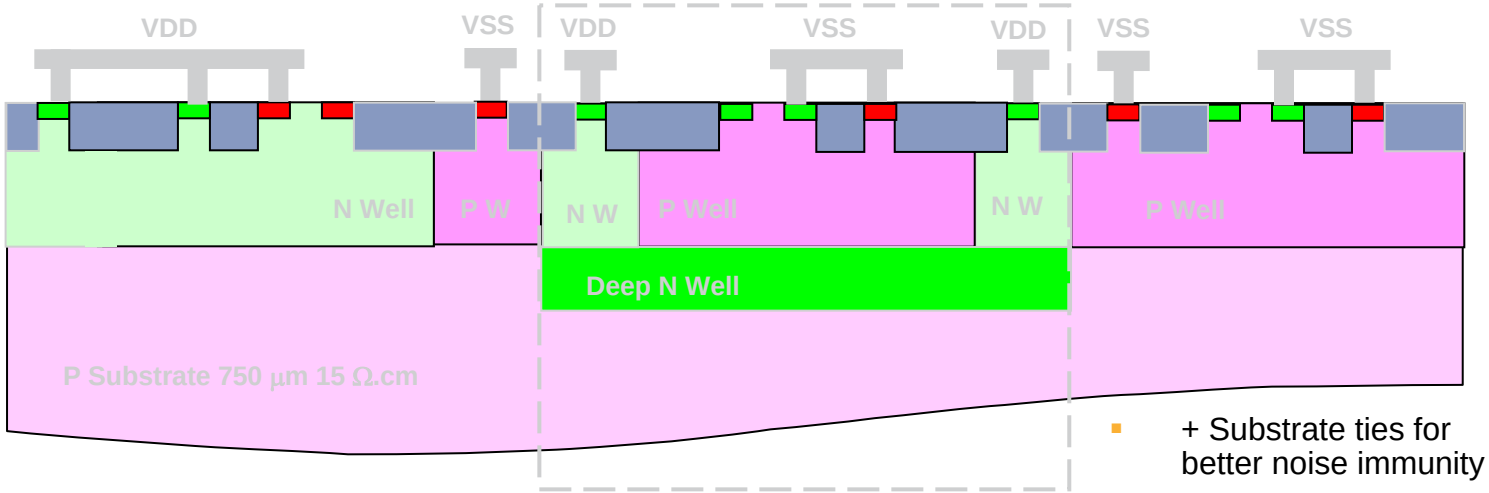




# ISLAND IMMUNE TO LATCH-UP

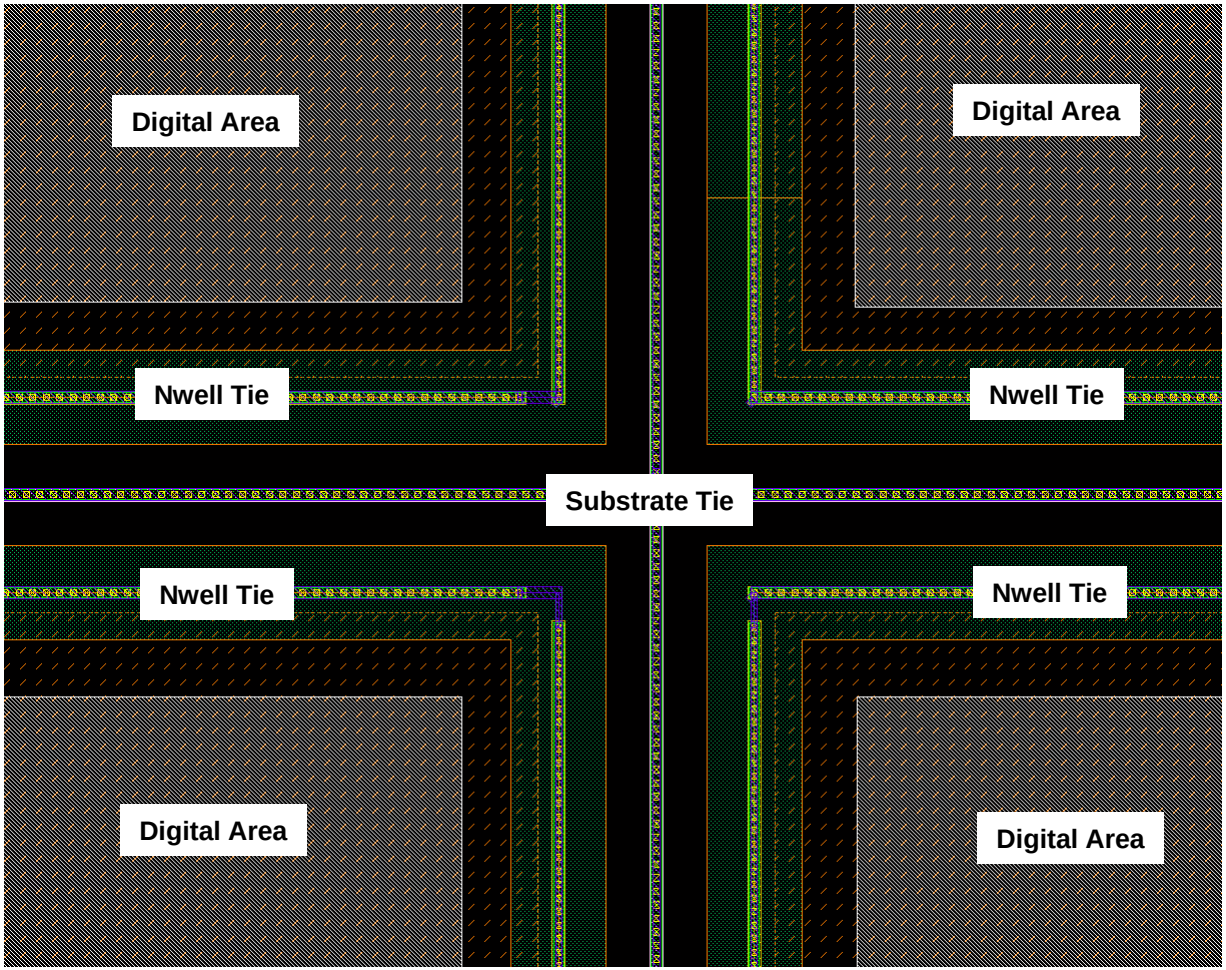



- Isolated Pwell containing NMOS only




- + Substrate ties for better noise immunity

# DEEP Nwell FRAGMENTATION IN DIGITAL SECTION




Deep Nwell with Nwell collector ring and substrate ties grid

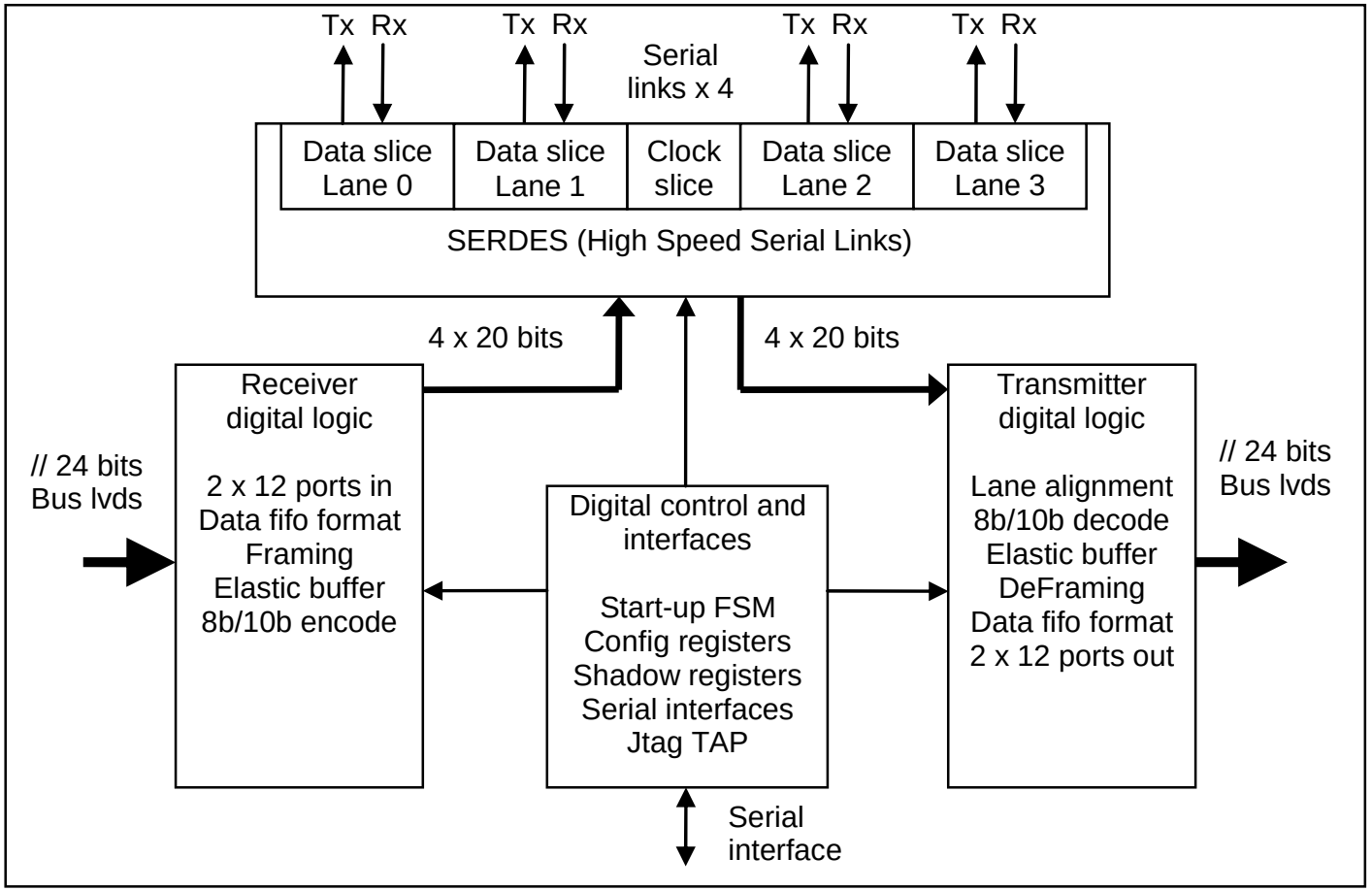
# SEL prevention rules

- Analogue section and LVDS I/Os
  - Isolated Pwell containing NMOS only
    - Latch-up immunity by design
    - Penalty : area increase, but on few cells
- Digital section
  - Complete deep Nwell coverage
  - Deep Nwell fragmentation
  - Substrate ties grid
- Standard I/Os
  - No change

# ON-going work

# Quatuor design finishing

- Quatuor block diagram:



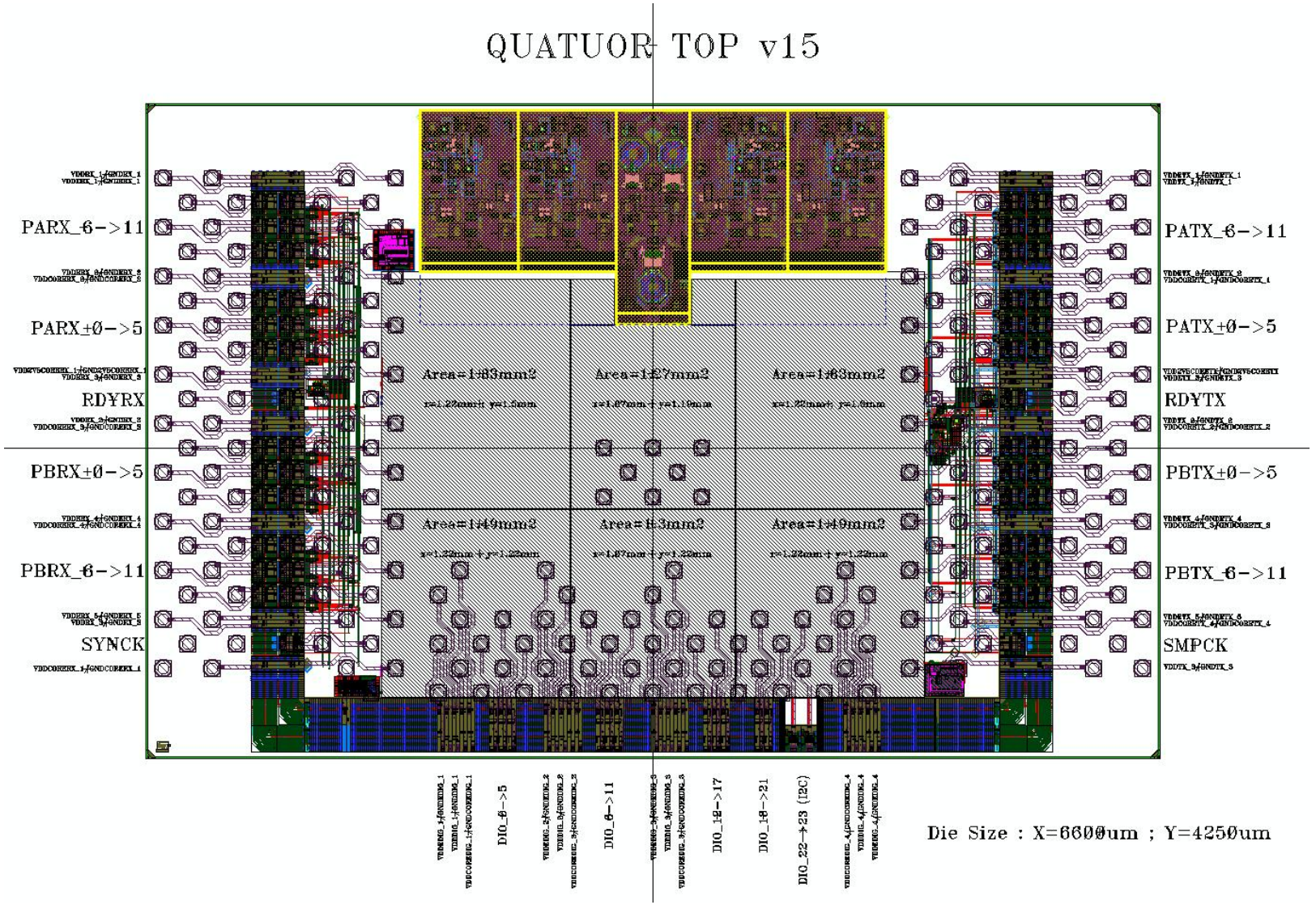
# Quatuor features

- Datapath by-passable functions:
  - Scrambler: single polynome
  - Framer: configurable length
  - Disparity: 8b10b
  - Aggregation: 4 modes
  - Bit inverter for all LVDS inputs/outputs
  - Asynchronous and synchronous modes
- BIST of datapath:
  - PRBS16 generator and monitor onto both LVDS input and output ports

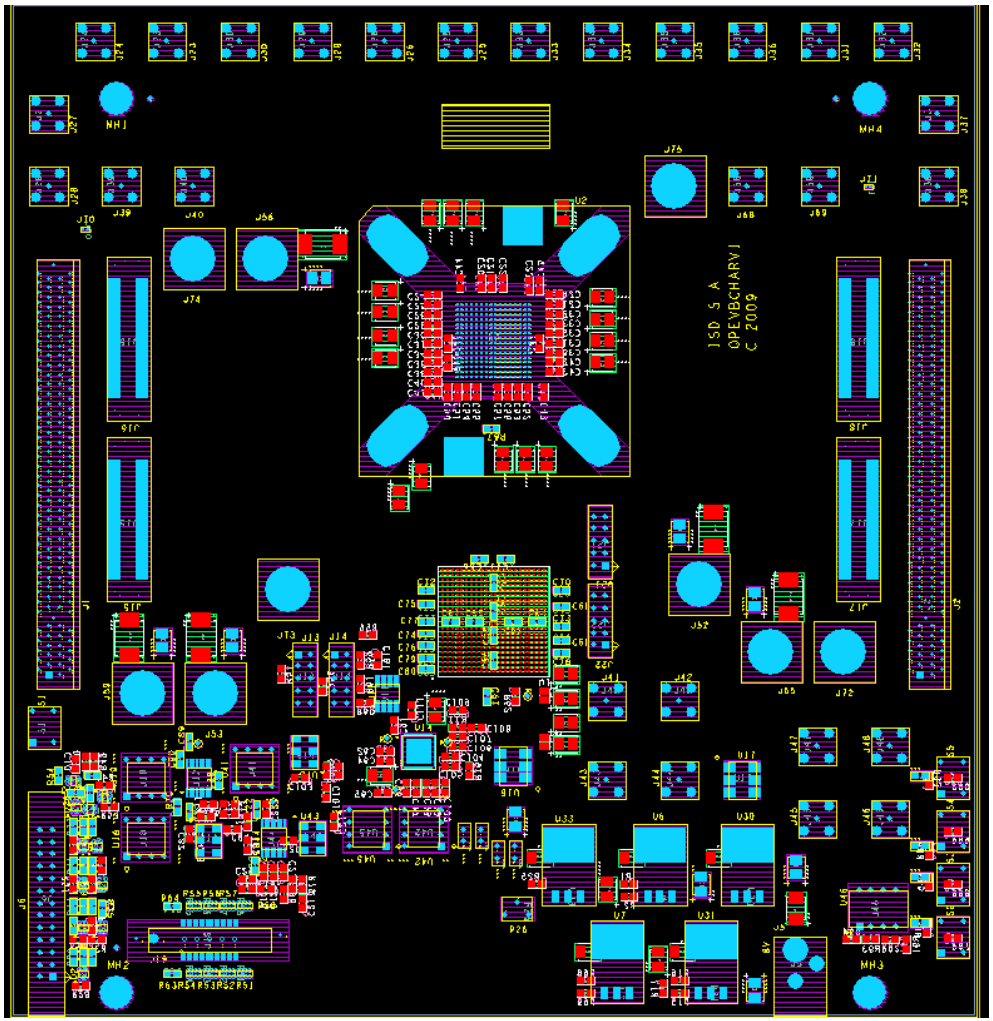
# Quatuor features

- Control
  - DFE hardcoded state machine for Serdes
  - ROM and RAM code for basic FSM data+inst execution for Serdes address space only
  - Scrubber FSM to monitor and/or correct any corrupted (SEU) bit in Serdes configuration registers
  - Serial ports: MDIO, JTAG, I²C, UART, SPI (from ISD)
  - Parallel port: 8bits address and data muxed Test Interface Controller
  - Base registers of 120 x 16 bits to configure and enable test logic of Quatuor

# Quatuor Layout view



# Evaluation board designed by ISD




- New Layout trial on going
  - LVDS skew now OK
- Board shape 20 x 21 cm

# 65nm ASIC Library Development

- Analysis of end-users needs in KIPSAT deliverable in good progress
- Preliminary library-cells test-chip design:
  - SRAMs with DeepNwell and ECC
  - Several types of Rad-Hard FFs (patents pending)
  - Specific clock-tree cells
  - Combinatorial cells

…Will be ready for same run than Quatuor (end April 2010)

# Perspectives/Conclusions

# DSM65nm ASIC technology Perspectives

- Quatuor cut1 will be fully measured in Q4 2010
- Quatuor cut2 and ESCC preliminary evaluation proposed to EC FP7 (seems rejected)
- Library-cells preliminary test-chip measurement campaigns under investigation with CNES, ESA in 2010 and early 2011.
- Telecom Structured ASIC Base development proposed to FP7 in Dec2008.
- First ASIC library test-chip possible in 2011 with:
  - Final Space-std-cells
  - Metal-customizable Space-cells
  - PLL, DDR
- High pin count Flip-chip packaging solution

…depending on proposals outcomes with CE, ESA, CNES, gvts. And industrial priorities.

# Conclusions

- KIPSAT is THE baseline project which permits:
  - Assessment of the ST 65nm for Space
  - Complete measurements of a high perf quad-HSSL
  - Definition of ASIC library needs and start of development of set of Rad-Hard cells
  - To grow the technical team dedicated to space DSM within ST/APM
- KIPSAT is not sufficient to secure 65nm DSM technology viable offer to end-user for ASICs.
- We must add the future stones together with correct level of budget, roles, schedule…

# Thank you!

- Special thanks to:

S.Lavastre, F.Badets, C.Lorin, S.Ramet, V.Cosnier, B.Affour, V.Visan, G.Gasiot, S.Clerc, P.Roche…

- See ST space products at:

www.st.com/aerospace