# 2010 ESA Microelectronics Presentation Days

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# Al.N. LGA625 PACKAGE DEVELOPMENT AND ESCC EVALUATION/QUALIFICATION

## CNES contract: 04/1643/01

**ESTEC, Noordwijk, March 30th to April 1st**

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# ALN LGA 625

# PACKAGE TECHNOLOGY RATIONALES

- First package of a series, w.o. rigid bond with board: LGA625
- 625 lands with 1.27 mm pitch and 35*35 mm body size
- Drawback of the non-rigid bond: the power heat dissipation can no longer transfer through the columns and spread out on the board => reliability impact
- Initially considered mitigation means
  - An heat-sink on top of the package for improved dissipation
  - A more thermally conductive ceramic: $Al_2O_3$ (l = 17 W/m.K) is replaced by AlN (l = 150 W/m.K) to help conduction from die to heat-sink
  - A larger lid seal ring area for better ceramic-lid thermal conductivity



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# DEVELOPMENT PLAN

- **Validation of the seal ring and lid option with package A**

- **Development and manufacturing of the B package options for the manufacturing of:**
  - **B1: 40# with the Tyndall PMOS4 test chip and the available lands interconnected through a daisy chain scheme for board level validation by the customer**
  - **B2: 2 batches of FM using an existing customer ASIC chip for qualification purpose without having to wait for the final ASIC design completion and manufacturing**

- **Development of the final package C for the end application and manufacturing of the first batch of FM to be used as a third lot for the package qualification**



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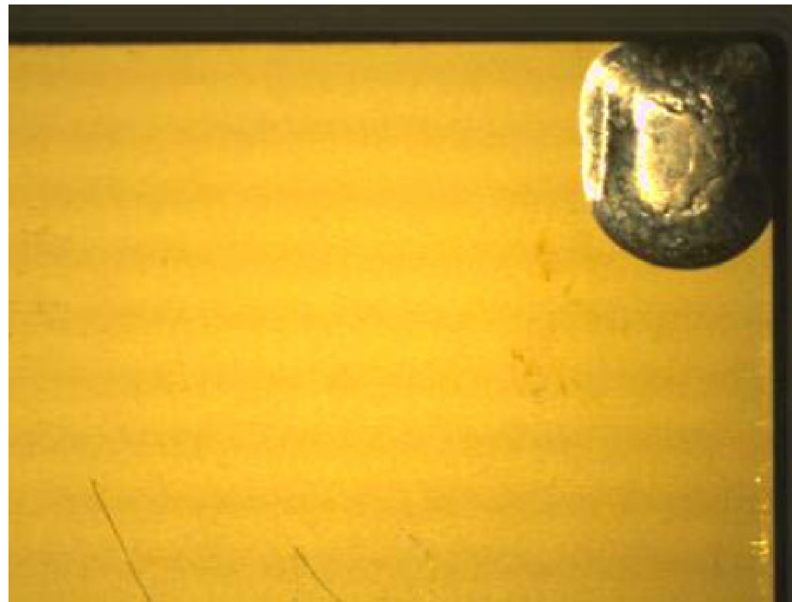
# PACKAGE A:
# 5 mm SEAL RING FEASIBILITY

- 3 trial lots using all the same package:
  - Trial #1: 5mm Kovar Combo lid (3#)
  - Trial #2: 2mm Kovar Combo lid (3#) – e2v standard
  - Trial #3: 5mm AlN Combo lid same lid/preform size (2#)

# PACKAGE A:
# 5 mm SEAL RING FEASIBILITY

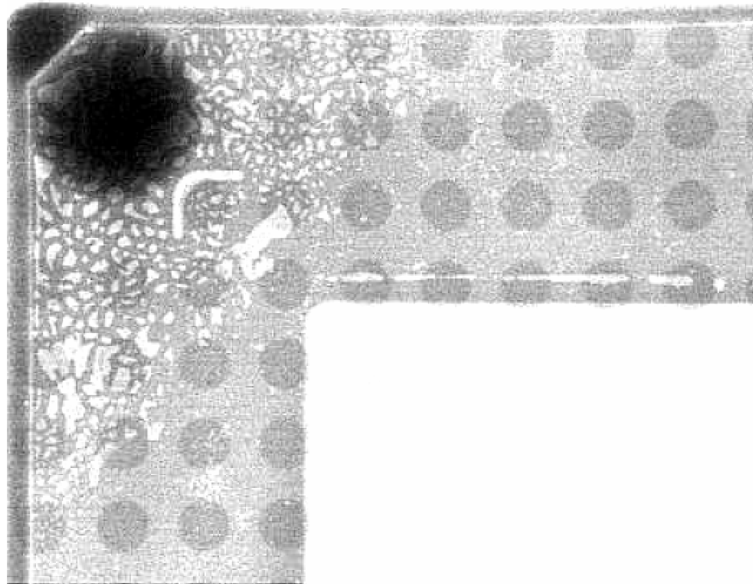
- **TRIAL 1 RESULTS (Kovar 5mm) (1/2)**
  - **Visual inspection: Solder alloy overflow on the top of the lid**



**3 rejects / 3 parts**

# PACKAGE A:
# 5 mm SEAL RING FEASIBILITY

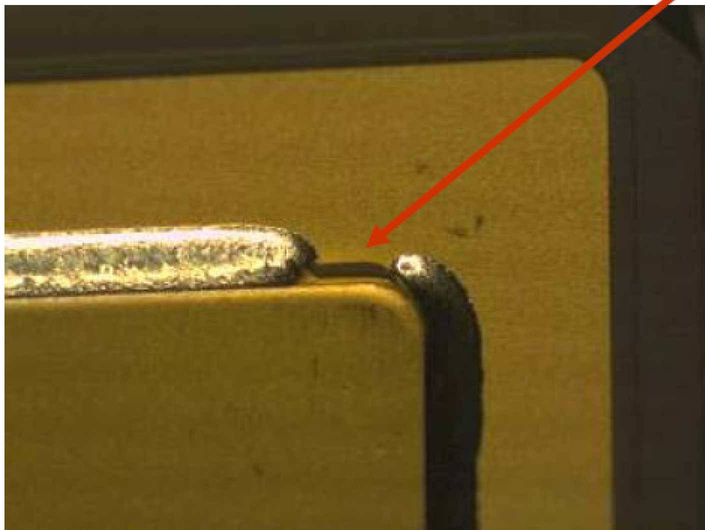
- **TRIAL 1 RESULTS (Kovar 5mm) (2/2)**
  - **X-rays: sealing fillet reduction by 70%**

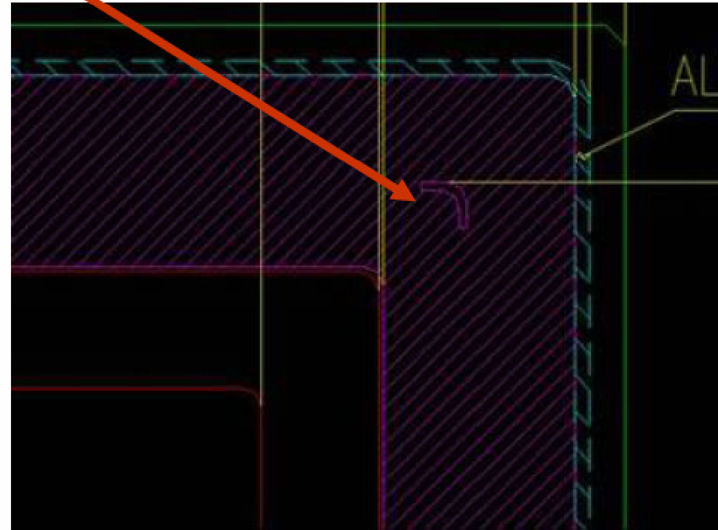


**Acceptance criteria: Sealing filet width reduction < 50%**
**1 reject / 3 parts**

# PACKAGE A:
# 5 mm SEAL RING FEASIBILITY

- **TRIAL 2 RESULTS (Kovar 2mm) (1/2)**
  - **Visual inspection: Incomplete solder fillet due to alignment mark**

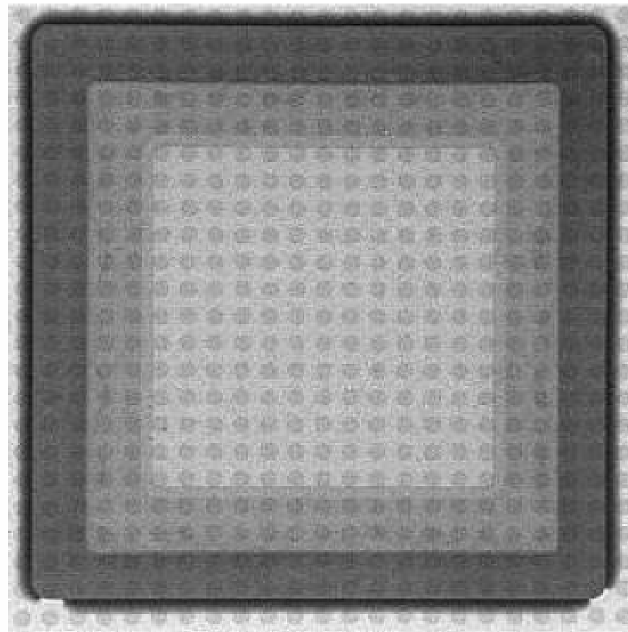





**3 rejects / 3 parts**

# PACKAGE A:
# 5 mm SEAL RING FEASIBILITY

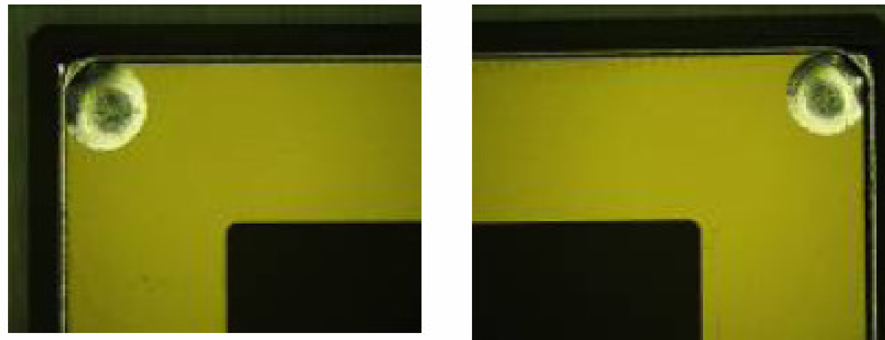
- **TRIAL 2 RESULTS (kovar 2mm) (2/2)**
  - **X-rays:sealing fillet reduction by 10%**



**Acceptance criteria: Sealing fillet width reduction < 50%**
**0 reject / 3 parts**

# PACKAGE A: 5 mm SEAL RING FEASIBILITY

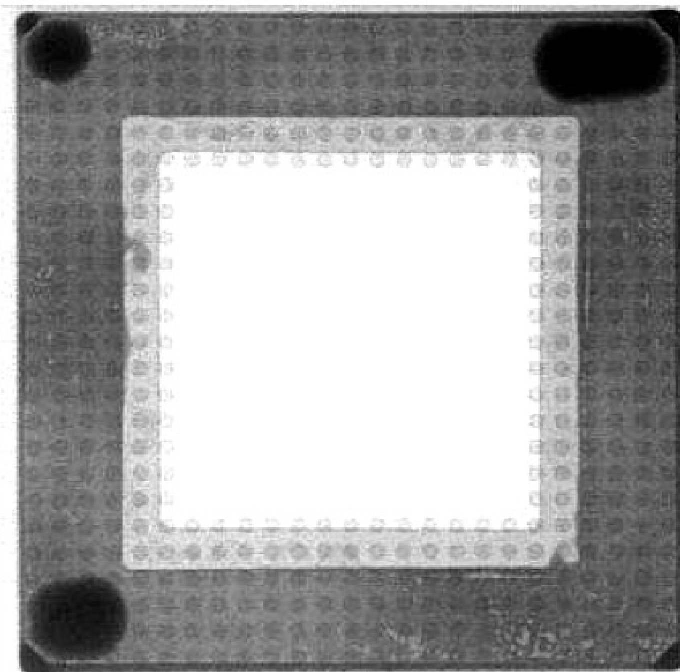
- TRIAL 3 RESULTS (AIN same size lid/preform) (1/2)
  - Visual inspection: solder alloy overflow on the top of the lid

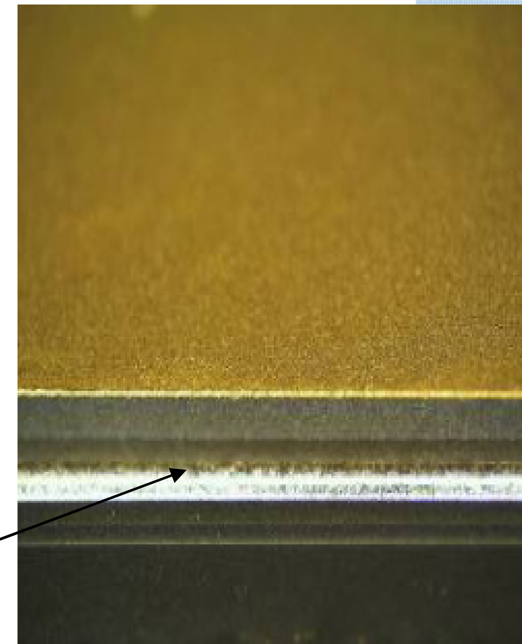


**2 rejects / 2 parts**

# PACKAGE A:
# 5 mm SEAL RING FEASIBILITY

- **TRIAL 3 RESULTS (AIN 5mm) (2/2)**
  - **X-rays:sealing fillet reduction by 40%**

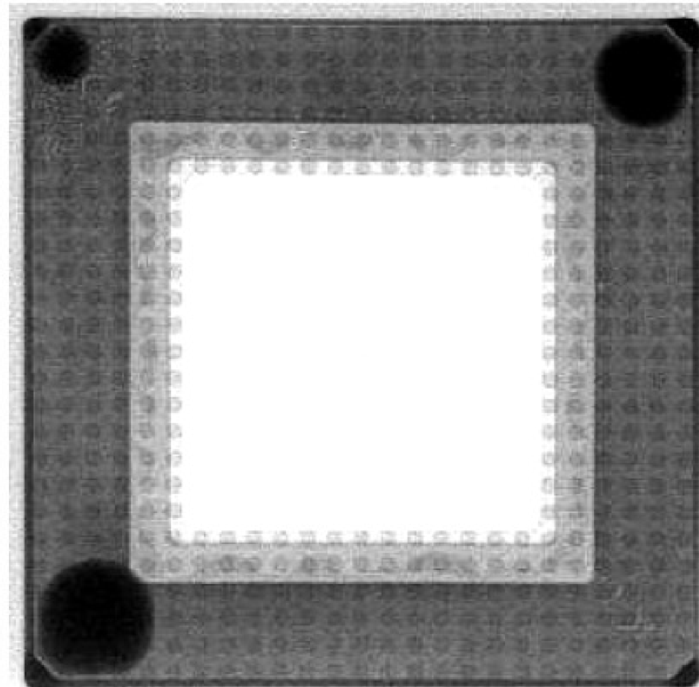





**Acceptance criteria: Sealing filet width reduction < 50%**
**0 reject / 2 parts**
**Because of the convex solder filet, a 4$^{th}$ trial was done for mitigating it**

# PACKAGE A: 5 mm SEAL RING FEASIBILITY

- TRIAL 4 RESULTS (AIN 5mm combo lid with lid smaller than preform size)
  - X-rays:sealing fillet reduction by 50%



**Acceptance criteria: Sealing filet width reduction < 50%**
**0 reject / 2 parts**

# PACKAGE A: 5 mm SEAL RING FEASIBILITY

- **Results:**
  - No pin hole whatever lid configuration is
  - No configuration fully compliant with space standards (solder alloy overflow)
  - Only 2mm Kovar combo lid OK after some process improvements

| | IVE | X-rays | Conclusion |
|---|---|---|---|
| 1 | 3 rejects | 1 reject | Fail |
| 2 | 0 | 0 | OK |
| 3 | 2 | 0 | Fail |
| 4 | 2 | 0 | Fail |



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# PACKAGE A: 5 mm SEAL RING FEASIBILITY

- 5mm seal ring: additional tests were performed to mitigate the solder alloy overflow
  - Standard process: use of 4 clips 1.5 pound
  - Trial 1: reduce the number of clips down to 2

    →No improvement (16 rejects / 20 parts)
  - Trial 2: reduce the clips pressure down to 1 pound

    → No improvement (18 rejects / 20 parts)

- Conclusions

Recommendation was to go ahead with 2mm kovar option



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# PACKAGE A:
# 5 mm SEAL RING FEASIBILITY

- **Validation and reliability tests**
  - ✓ Cavity co-planarity characterization
  - ✓ Die attach tests
  - ✓ Seal ring characterization – hermeticity
  - ✓ Thermal cycling (300 cycles)
  - ✓ Fine and gross Leak
  - ✓ Vapor content (3#)
  - ✓ Micro-sectionning (2#)
  - ✓ PIND tests
  - ✓ Visual inspection & X-rays
  - ✓ Stud pull test (10#)

- **Conclusions**

**Process is compliant with space quality level**



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# Daisy chain packages (B1): manufacturing and delivery

- The aim of this was to validate the assembly of the packages on the boards
- This package is worst case compared to the final package from a thermal point of view:
  - Smaller die (10*10 mm instead of 14*14)
  - Smaller ceramic thickness (3mm instead of 6mm)
- This package includes a thermal die, PMOS4 from Tyndall with:
  - Heater resistor (up to 12W)
  - Temperature reference diodes (3 per die)
  - Strain gauges (6 per die)



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# Daisy chain packages (B1): manufacturing and delivery

- We proceeded with the procurement of the PMOS4 thermal die, the test socket & board
- We set the package specification, designed and procured it
- We packaged the PMOS4 die to produce 40#, tested them and shipped them to the customer for evaluation of their assembly on flight boards
- B1 thickness is 3mm and is a worst case for thermal & mechanical evaluation with respect to the 6mm for the C package which will allow for a better heat conduction



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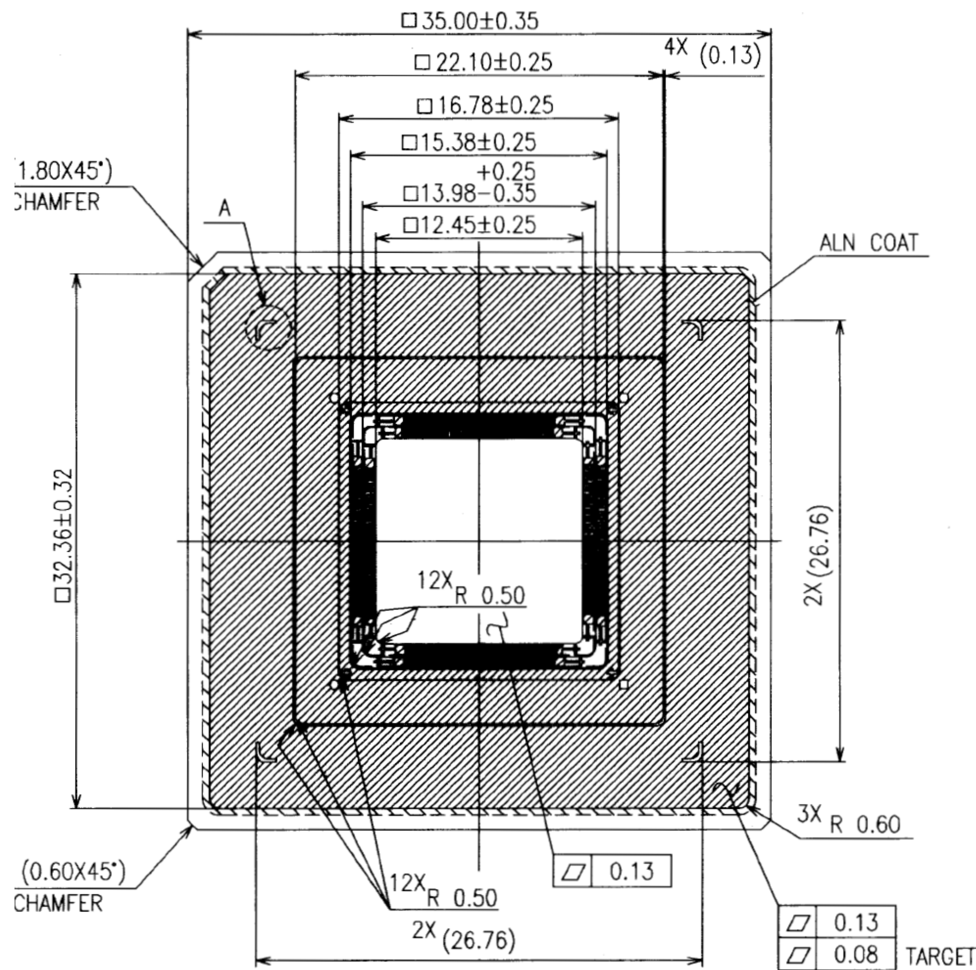
# PACKAGE B1
# THERMAL DIE + DAISY CHAINS

- **Package design (1/2)**



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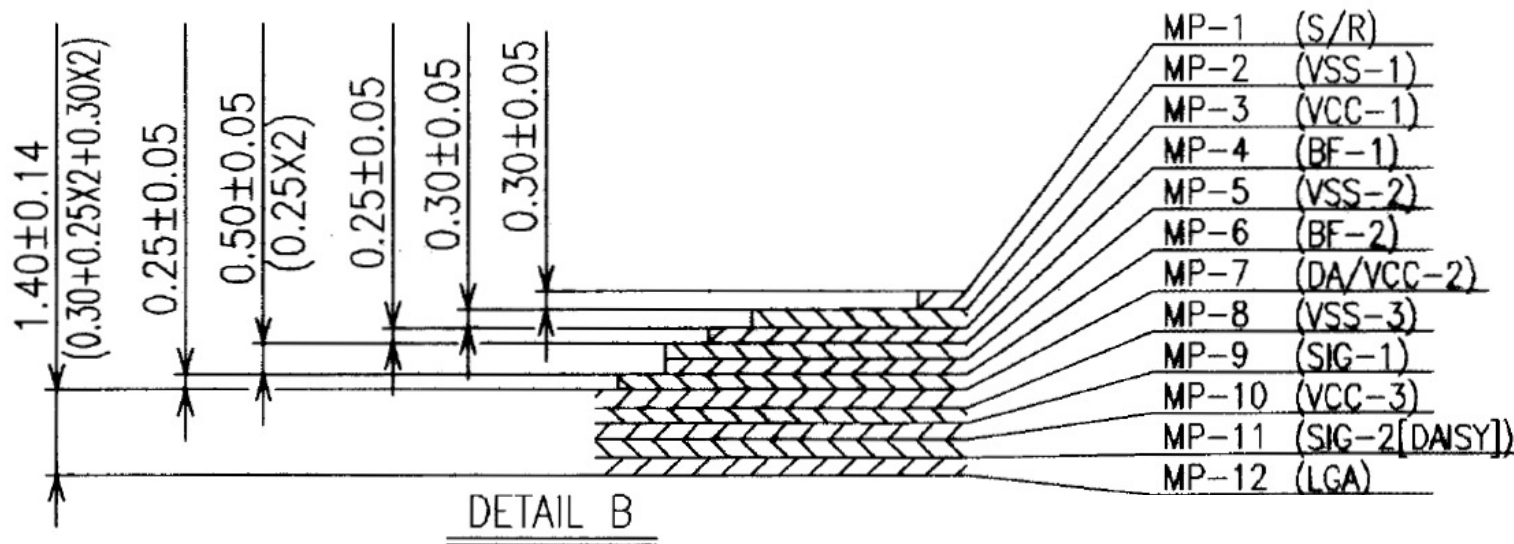
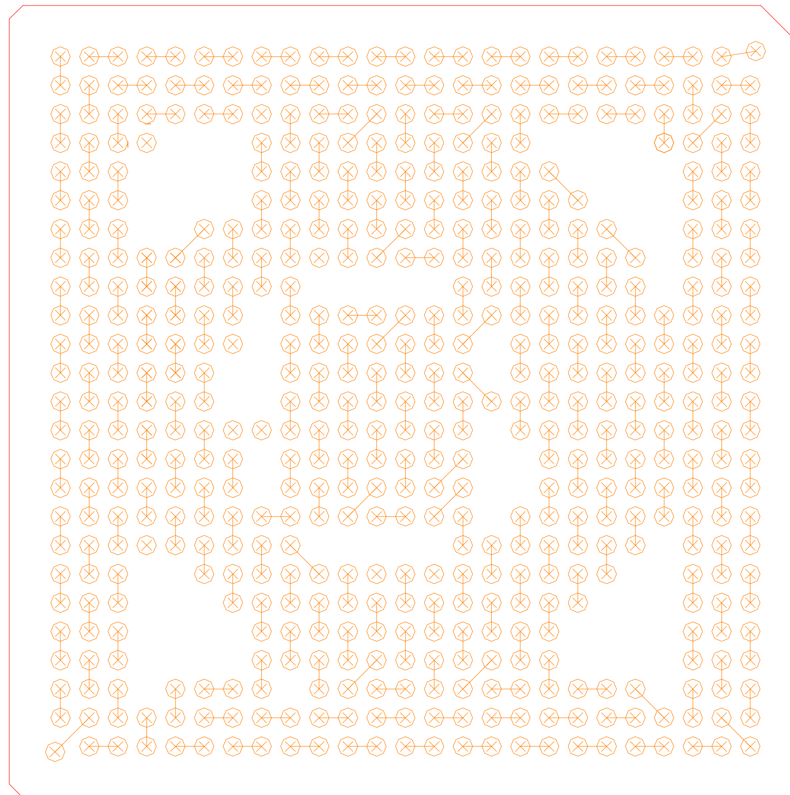
# PACKAGE B1
# THERMAL DIE + DAISY CHAINS

- **Package design (2/2)**



# PACKAGE B1
# THERMAL DIE + DAISY CHAINS

- 540 unused pins are daisy chained as follow





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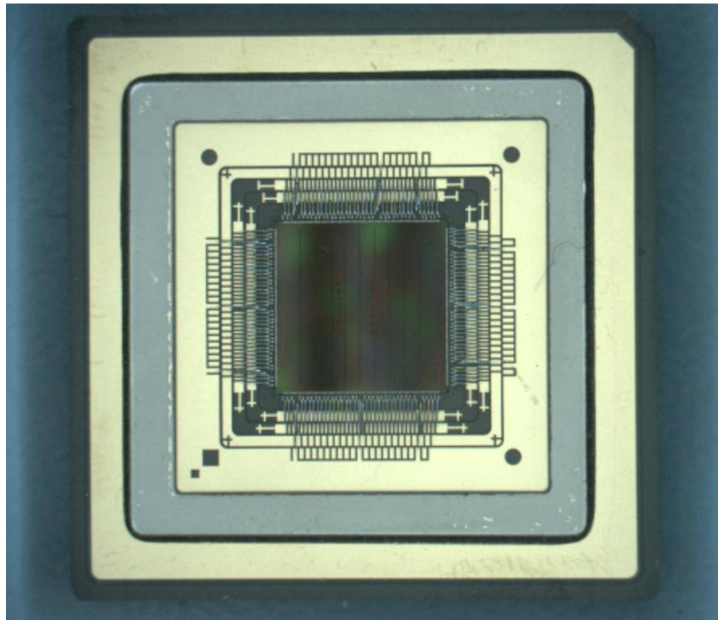
# Package B2 manufacturing

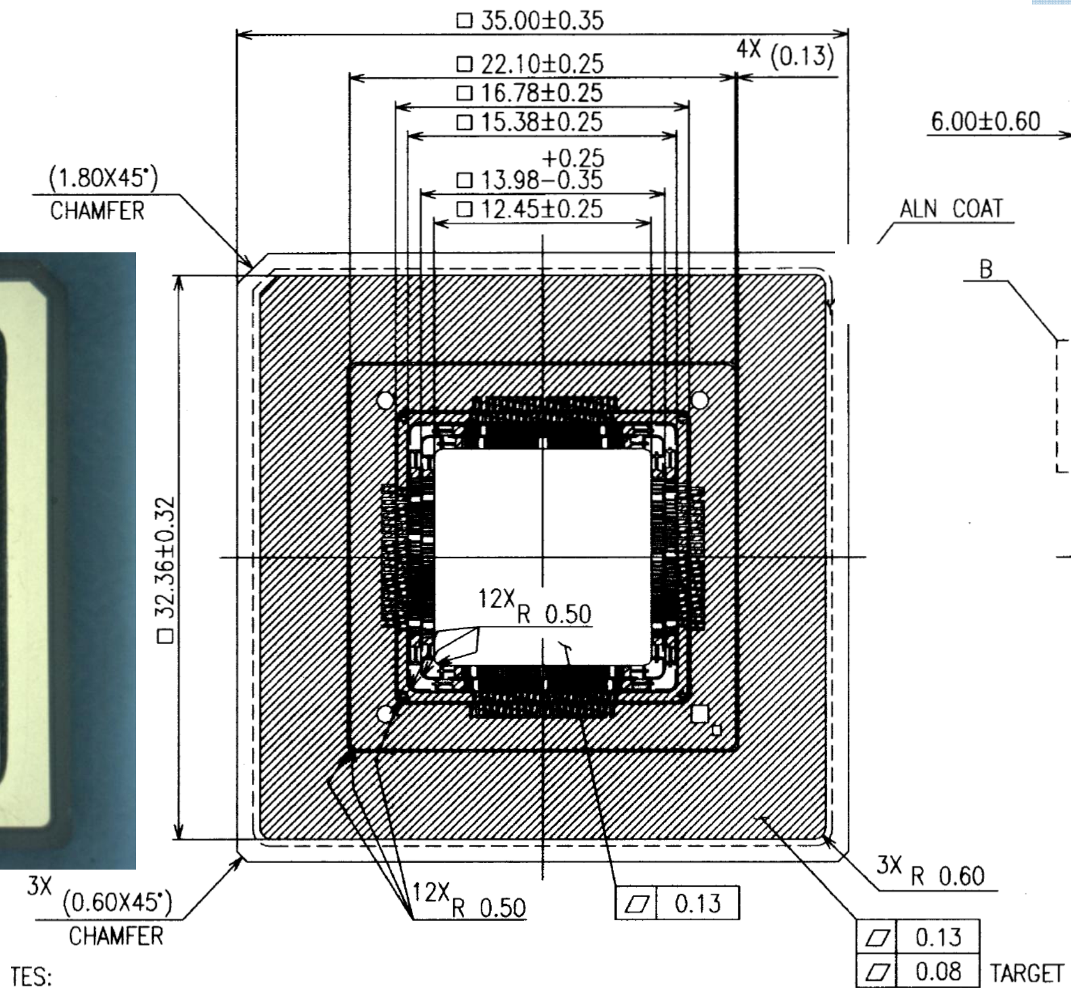
- The aim of this package is to start the qualification of the final package (1st and 2nd lot) with an available ASIC die
  - Same thickness than final package (6mm), same seal ring...
  - Only cavity size is different

- No parts have been delivered to the customer, only the qualification tests report

# Package B2 manufacturing

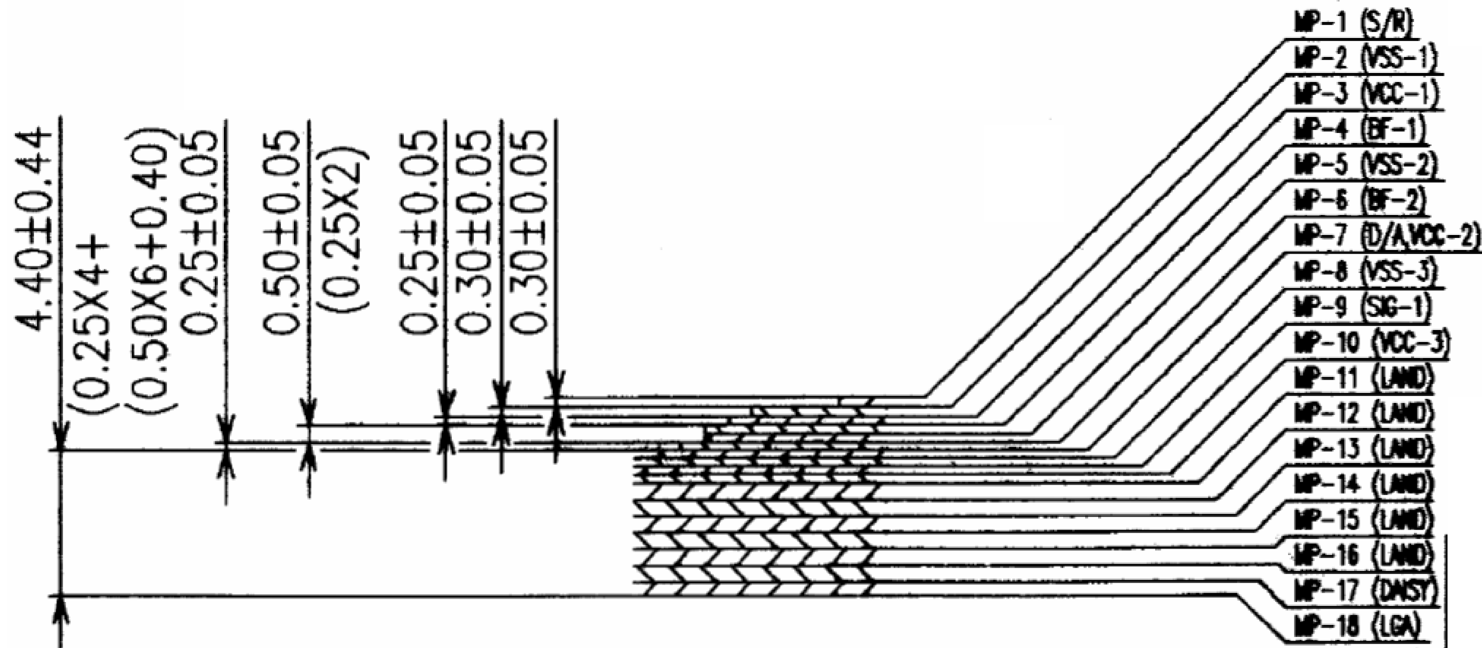
- **Package design (1/2)**





# Package B2 manufacturing

- Package design (2/2)



# Package B2 manufacturing

- Die manufacturing and probe
- B2 Package specification, design and procurement
- Lot 1 was assembled, tested to QML V and CNES CSI'd
- Lot 2 was assembled, tested to QML V and CNES CSI'd
- First and second lots qualification on going

# Package C: QML-V manufacturing

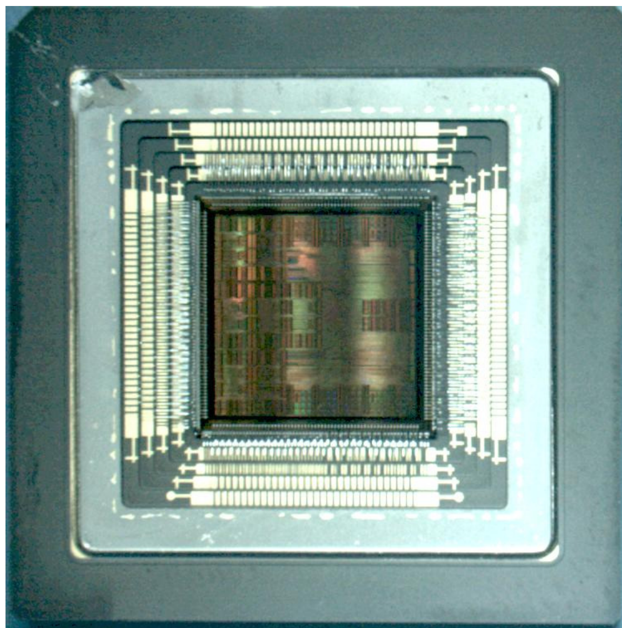
| | |
|---|---|
| End customer ASIC manufacturing | Completed |
| Package C design and procurement | Completed |
| End customer ASIC industrialization | Completed |
| Lot 3 assembled and CNES precaped | On going (1) |
| ESCC qualification test plan | Completed (2) |
| Lot 3 CNES CSI | 10W18 |

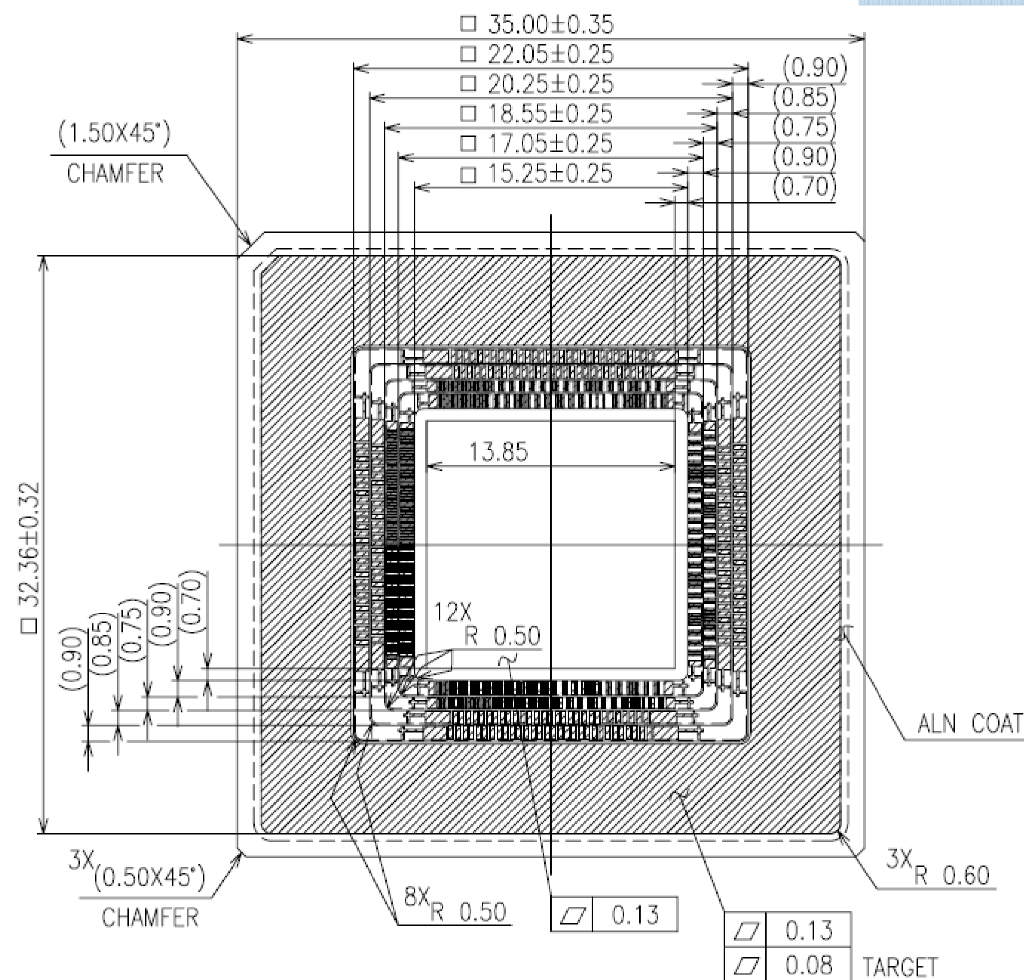
(1) Reference L4.2: ADF-PL-R1003-ALN, 2009 December – AIN LGA package – Assembly Inspection Report

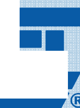
(2) Reference L3.1: ADF-PL-R0994-ALN, 2008 December – AIN LGA package qualification and Evaluation test plan

# Package C: QML-V manufacturing

- **Package design (1/4)**

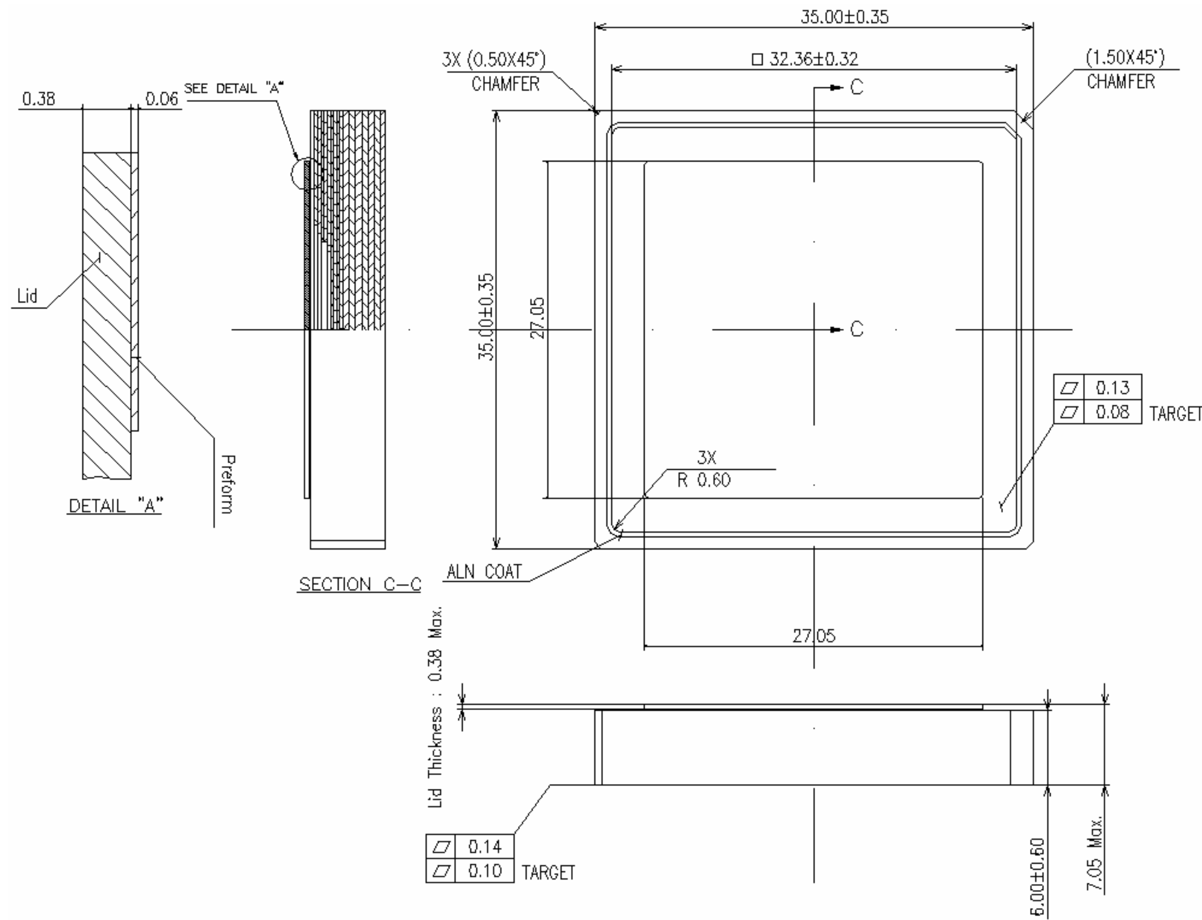




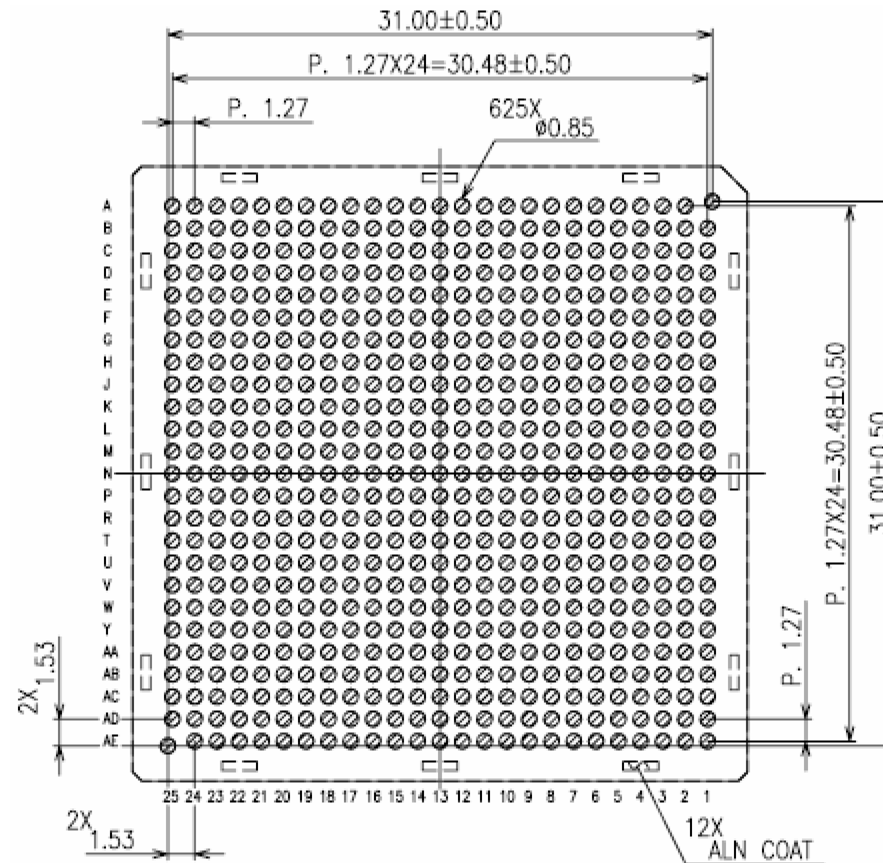
# Package C: QML-V manufacturing

- Package design (2/4)



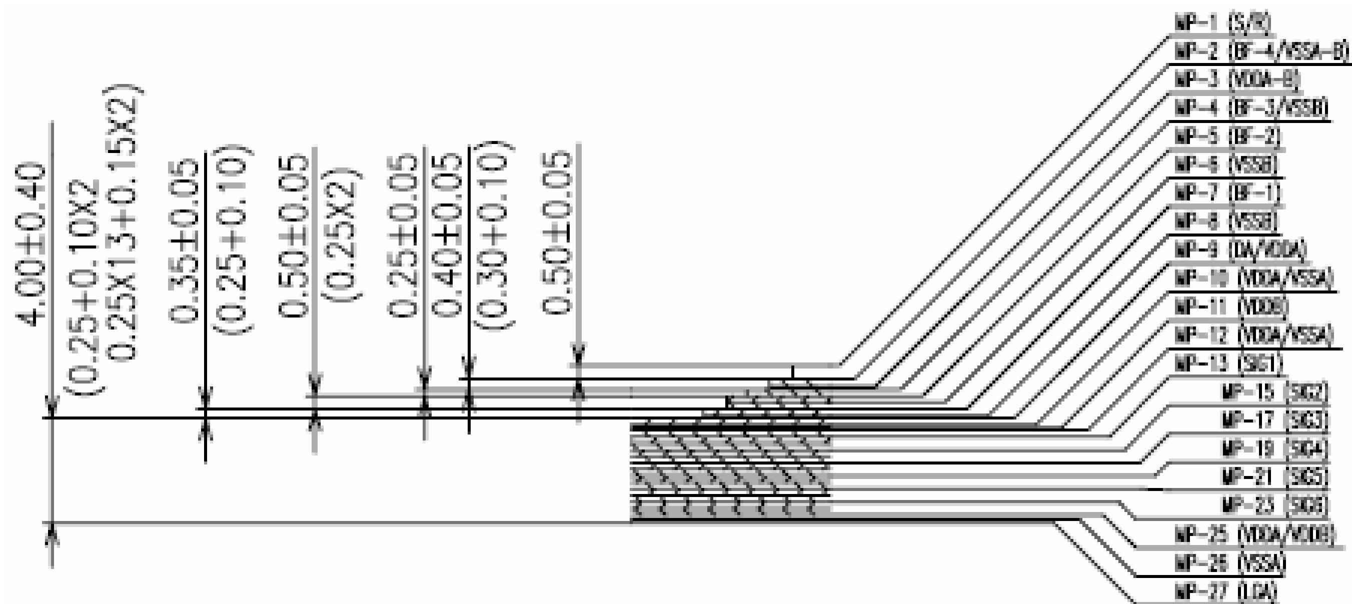
# Package C: QML-V manufacturing

- **Package design (3/4)**



# Package C: QML-V manufacturing

- **Package design (4/4)**




- **The 27 layers were necessary for a good matching of the LVDS**



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# ESCC QUALIFICATION STATUS

| | |
|---|---|
| ■ Lot 3 parts ready for qualification | 10W19 |
| ■ Atmel qualification completed | 10W25 |
| ■ Atmel qualification report | 10W26 |
| ■ ESCC evaluation completed | 10W33 |
| ■ PID | 10W35 |

# SPACE PACKAGES OFFERING & ROADMAP



Pin count / year of introduction

SP2GA=Short Pin PGA

# THANKS TO …

- Jean-Louis Venturin and David Dangla, CNES, who managed to make and manage this contract

- Valérie Briot, ATMEL, who managed it!