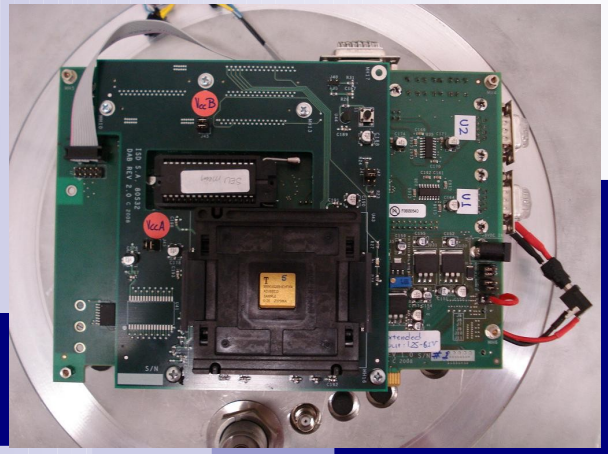


80S32 Functional and Performance Validation

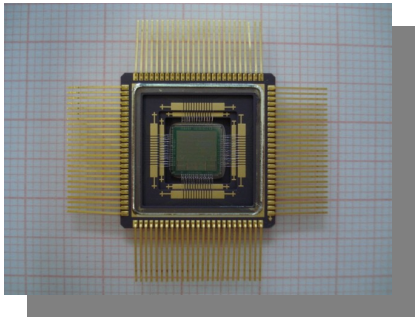
Microelectronics Presentation Days 2010

Integrated Systems Development

30 March – 1 April 2010, ESA, ESTEC

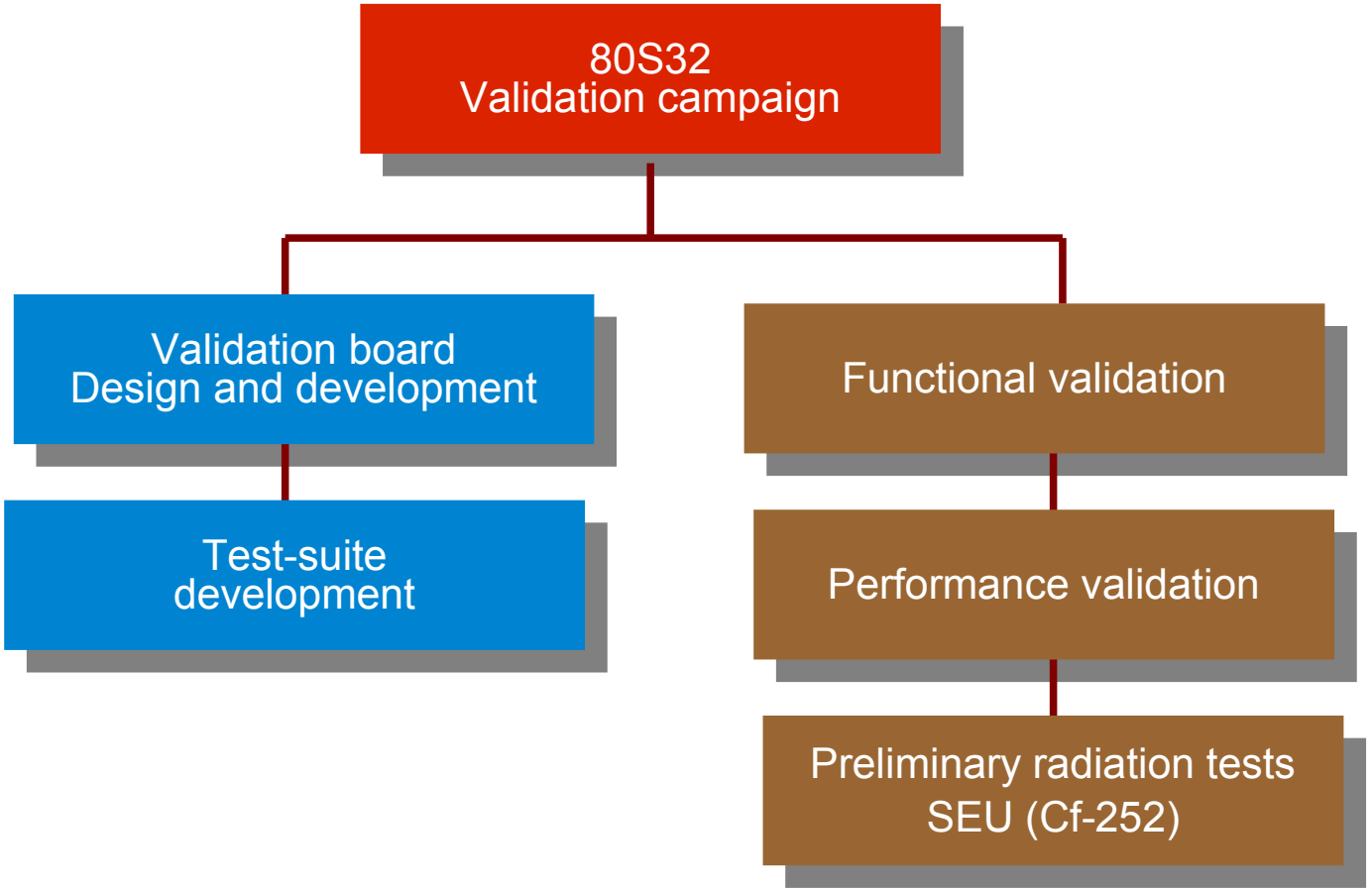
ISD
Integrated Systems Development S.A.

80S32 component overview



- **Aim of the activity**
  - Functional and performance validation of ADV80S32 engineering devices
- **ADV80S32**
  - 8-bit microcontroller developed by ADV engineering for ESA
  - Extended timers
  - USART interfaces
  - Interrupt inputs
  - De-multiplexed address/data buses
  - Extended addressing range
  - SEU protection of memory cells
  - Includes a hardware CRC calculation engine compliant to CCSDS TM/TC standard
  - **Technology**: Temic/Atmel 0.5um radiation hardened gate array technology (MG2RT)

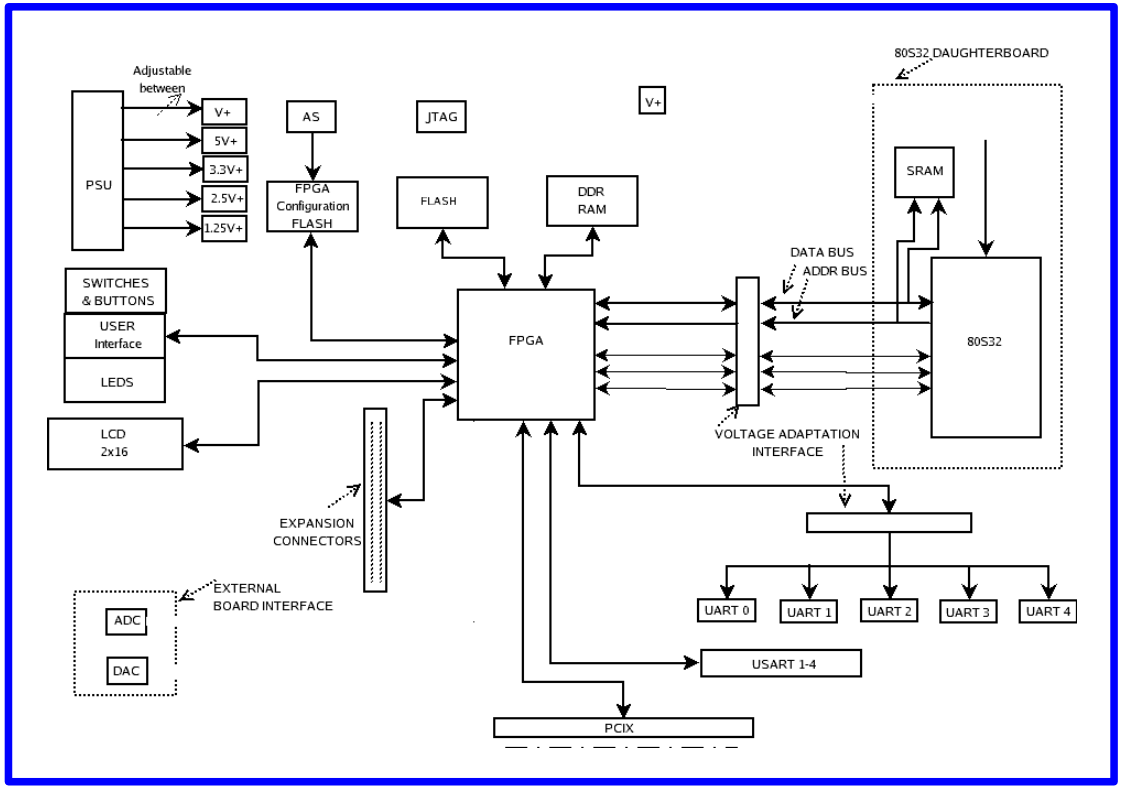
Validation campaign overview



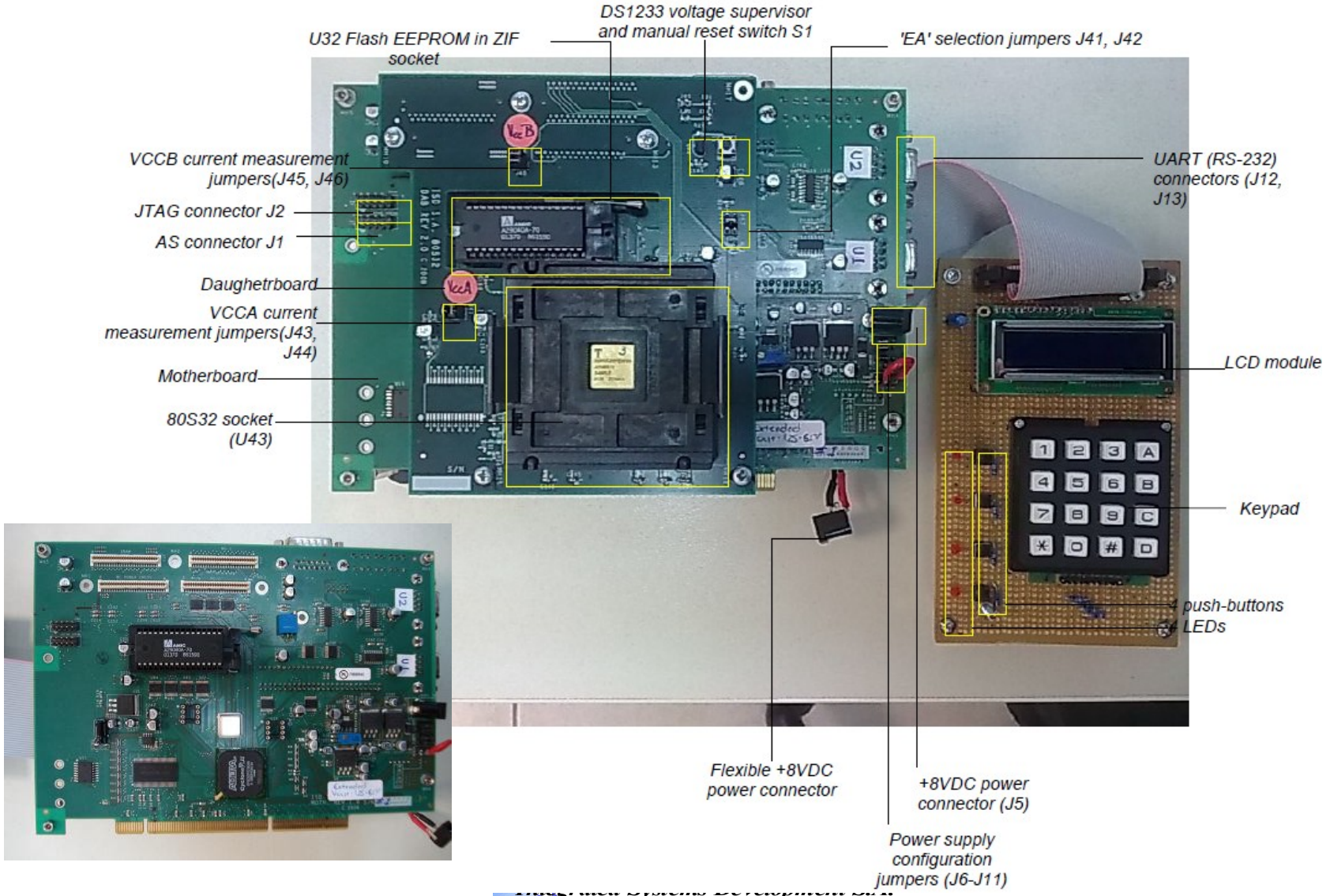
Validation Board architecture

- Modular architecture → Motherboard + DUT daughterboard
- Motherboard includes an FPGA for stimuli generation, data routing, data monitoring and peripheral handling.
- FPGA : Altera Cyclone-II™ series
  - 50,528 LE
  - 109 GPIO pins available on the daughterboard
- 256 Mbit DDR SDRAM
- 512K x 8bit Flash on ZIF socket
- Custom developed remote keypad enables remote control of the DUT
- UART and USART interfaces
- PCI-X card edge connection for high speed data communications
- DUT daughterboard supports onboard SRAM and hosts a DUT in a socket.

80S32 Validation board block diagram



Validation board implementation



Functional and Performance Tests

- **Functional Tests**
  - Verify the backward compatibility with the standard Intel™ 8032 core.
  - Check the correct operation of the additional features: CRC engine, extended internal memory, interrupt management, timers and serial interfaces.

- **Performance Tests**
  - Distinct typical tasks:
    - Matrix arithmetic
    - Signal processing
    - Sorting/searching algorithms
  - Dhrystone and Whetstone synthetic workloads

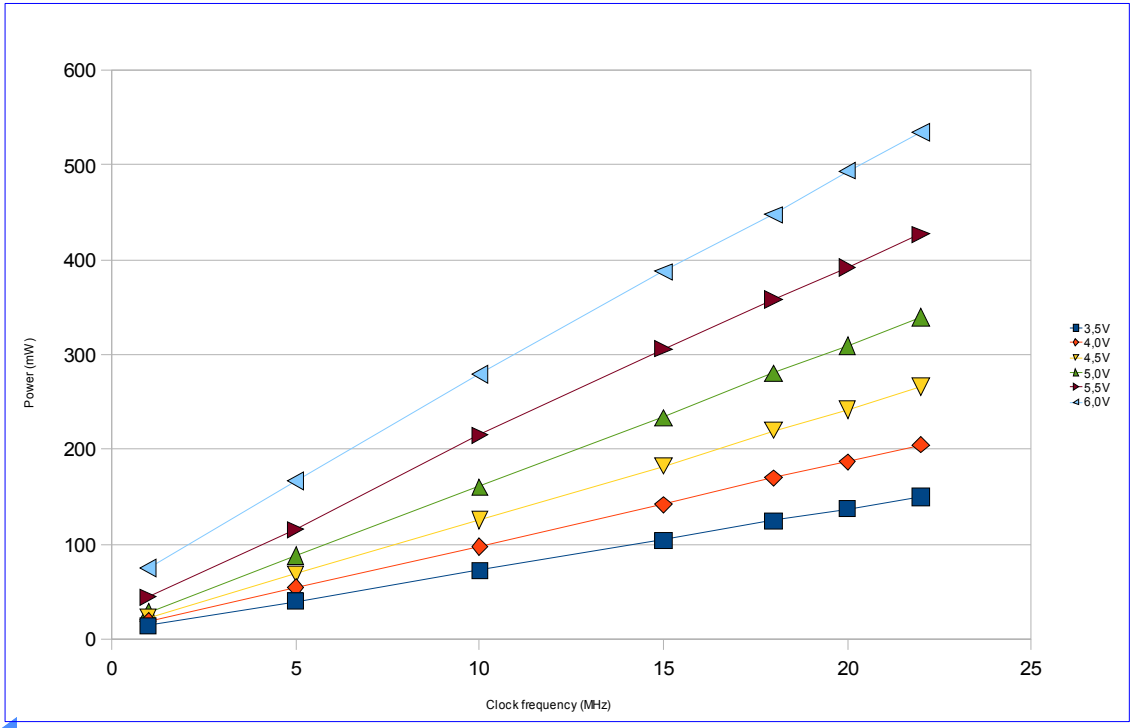
Category	Passed	Problematic	Failed
Internal Memory	4	1	-
External Memory	1	-	-
Timers/Counters	17	-	-
Serial Ports	8	-	-
Interrupt controller	-	1	-
CRC Accelerator	1	-	-
Boot PROM	-	-	1
Instruction Set	28	-	-
Perfromance	24	-	-
Overall	**96.51%**	**2.33%**	**1.16%**

Power supply measurements

- Objective → characterize 80S32 uC in terms of power consumption under specific activity and operating conditions.
- Characterization along a two-dimensional voltage and clock frequency range by simultaneous monitoring of package temperature.

f_{CLK}(max) = 22 MHz	
Vs (V)	**P (mW)**
4.5 (min)	266
5.0 (typ)	339.2
5.5 (max)	427

Power consumption at f_{CLK} = 22MHz



Bugs & Problems report

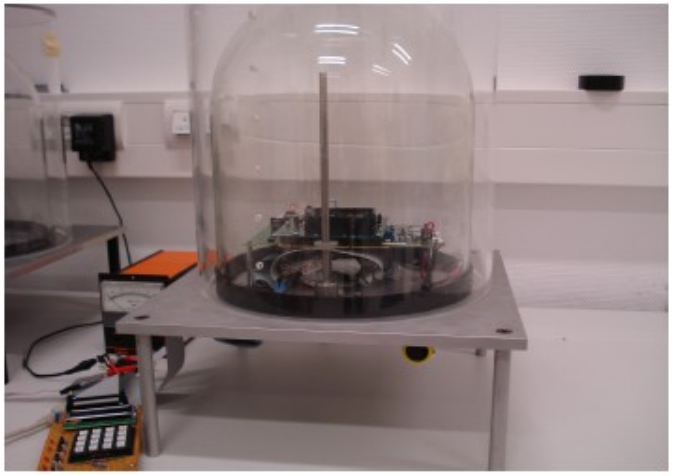
- Difficulty to run code in EDAC mode
- Parallel port P0 cannot be configured as general purpose I/O
- Interrupts IE2, IE3 & IE4 once triggered by software, they cannot be cleared
- USART interrupts are raised prematurely
- Default values (power-up or reset) of some registers are different from those described in the datasheet
- A number of output pins are defined in the datasheet as floating, though they should be tied to VSS
- Reset pin is defined in the datasheet as active low, whereas it should be active high.

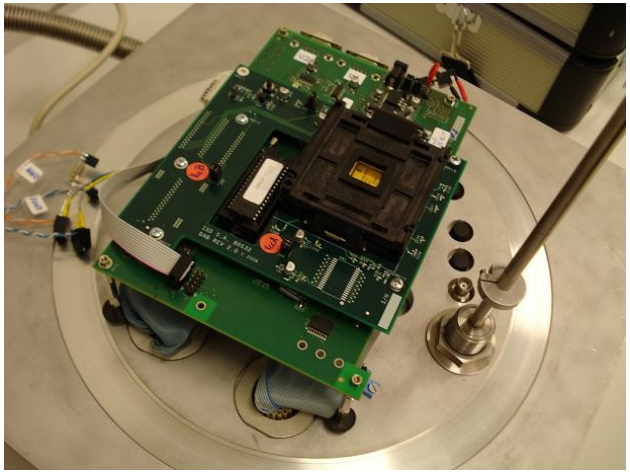
SEU radiation test campaign

- SEU radiation campaign successfully completed at ESA-ESTEC on January 2009 by utilizing the Cf-252 test facility.

http://microelectronics.esa.int/components/comppage.htm#80S32
http://microelectronics.esa.int/cgi-bin/finalreport.cgi

- The tests were conducted under vacuum conditions inside a suitable bell-jar radiation chamber.
- During the tests, the DUT was remote controlled via the remote keypad, while the error logging was performed by a host PC via the UART port.





SEU test results

- During the three-day testing period a number of recoverable errors were detected at the internal memory of the device.
- Two test runs were launched and only corrected errors have been detected.
- Two interrupts on SW normal execution were observed (crashes on both test runs) → may be assumed to be SEU events in flip-flops.

Metrics	1st RUN	2nd RUN
Total duration (t)	12h	19h 31m
Corrected RAM errors (e)	7	42
Uncorrected RAM errors	0	0
Possible flip-flop SEU events	1	1
Upset rate er (upsets/ sec)	1.62×10^{-4}	5.98×10^{-4}
Test cross-section X (cm^2)	3.90×10^{-6}	1.43×10^{-5}
Cross-section per bit Xb (cm^2/bit)	4.31×10^{-9}	9.40×10^{-9}

Conclusions

- **Functional validation**
  - Most parts of the 80S32 have been found to work properly
  - A few functional problems have been discovered requiring description, available as an errata to the datasheet.
  - The most serious issue remains the impossibility to generate valid executables featuring EDAC support when compiled from C-sources → further investigation required in order to identify a possible patch to the compilation tools.
- **Performance validation**
  - Error-free operation up to clock frequency of 22MHz measured at a maximum temperature of 41.5ºC in the range of 4.5-5.5V supply voltage.
- **Power consumption**
  - The power consumption at 5.0V is about 16mW/MHz
- **Radiation tolerance**
  - SEU error rates stay far below the SEU cross-sections provided by Atmel for the MG2RT technology and the 80S32 uC has been shown to exhibit very good radiation tolerance.