DTP ASICs experience feedback
Developed under ARTES3 ESA contract

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Summary

- Context
- ASICs description
- Lessons learned
- Design flow
- Focus on C-based Architecture Synthesis
- Focus on Physical Synthesis
- Conclusion
Standard DTP architecture

High Data Rate Transfer Between Functions (x Gbps)

ADC \rightarrow DEMUX \rightarrow MUX \rightarrow DAC

\( 1 \rightarrow n \rightarrow n \)

2n converters

Core Signal Processing (Hundreds of ASICs)

Very High Throughput
CHAN ASIC

- MUX or DEMUX operation
- Main features

<table>
<thead>
<tr>
<th>Name</th>
<th>CHAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Working Frequency</td>
<td>Up to 350 MHz</td>
</tr>
<tr>
<td>Technology</td>
<td>ATC18RHA (ATMEL 0,18 µm)</td>
</tr>
<tr>
<td>Matrix</td>
<td>ATC18RHA95_504D (double padring) (4.8 M usable gates)</td>
</tr>
<tr>
<td>Package</td>
<td>MCGA</td>
</tr>
<tr>
<td>Core Power Supply Voltage</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Periphery Power Supply Voltage</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Estimated Power Consumption</td>
<td>9 W</td>
</tr>
<tr>
<td>Measured Power Consumption</td>
<td>6 W</td>
</tr>
</tbody>
</table>

- Prototypes delivered in 09/2009
- Prototypes fully tested on the DTP EQM
CHAN LAYOUT

- > 100 memory blocks
- 2 PLLs
- More than 48 clock domains
### SW ASIC

- **Switch operation**
- **Main features**

<table>
<thead>
<tr>
<th>Name</th>
<th>SW</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Working Frequency</strong></td>
<td>Up to 150 MHz</td>
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<tr>
<td><strong>Technology</strong></td>
<td>ATC18RHA (ATMEL 0,18 µm)</td>
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<tr>
<td><strong>Matrix</strong></td>
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<td>3.3 V</td>
</tr>
<tr>
<td><strong>Estimated Power Consumption</strong></td>
<td>6.2 W</td>
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<tr>
<td><strong>Measured Power Consumption</strong></td>
<td>5.8 W</td>
</tr>
</tbody>
</table>

- **Prototypes delivered in 03/2009**
- **Prototypes fully tested on the DTP EQM**
SW ASIC main features (2/2)

SW Layout
- some memory blocks
- 1 PLL
- > 20 clock domains
Lessons learned (1/2)

MCGA package
- difficulties to place n and p balls of LVDS signal close to each other
  - Atmel had to “grope” to obtain expected results
- No detailed RLC model of this package at the beginning of the project
  - Very long time to obtain this RLC model => ask it at the early beginning of the project

Pads
- No internal adaptation resistor between n and p pins in RX LVDS pads
  - These resistors had to be placed directly on the board
- No 2.5V pads library available at the beginning of the project
  - Use of 3.3V instead. This 2.5V library is now available
Lessons learned (2/2)

Clock trees
- CHAN had a lot of generated clocks (>48) and it was difficult to set an efficient approach with Atmel for the layout constraints
  - Many iterations but in the end, fully successful design
- MX04Dx and MX02Dx multiplexer rise/fall delay are not balanced
  - Clock pulse width issue on high frequency clock. Necessity to use standard logic cell instead of multiplexers on clock trees.

Memories
- Issue with the memories when the awt pin is used (timing arc seen by Synopsys between di and do in functional mode)
  - Use of set_disable_timing command
ATC18RHA design flow

- Spec level
  - Specification and C model creation
  - C-based architectural synthesis
  - IPs integration
  - Logic Synthesis with default WLM
  - Scan insertion
  - RTL Simulation
  - Early Floorplanning
  - Physical Synthesis
  - Static Timing Analysis
  - Formal Proof
  - Simulation
  - Timing driven Layout
  - Static Timing Analysis
  - Simulation
  - Formal Proof
  - TOS references generation
  - ASC Manufacturing

- RTL level
  - Optional parallel validation flow: FPGA/emulation
  - Gate-level pre-layout
  - Post layout level

- Precision RTL (Mentor)
  - Workshop Forte (Sun)
  - Catapult SL (Mentor)
  - HDL Designer (Mentor)
  - Rule checker (Synopsys)
  - ModelSim (Mentor)
  - Test coverage (Mentor)
  - Design Compiler
  - DFT compiler, Tetramax (Synopsys)
  - IC Compiler (Synopsys)

- Thalès Design
- Thalès Verification
- Thalès Logic Synthesis
- Activity under manufacturer responsibility
FOCUS ON

C-BASED

ARCHITECTURE SYNTHESIS
Standard flow

Processing requirement

Algorithm study matlab, C/C++

C/C++ algorithm coding

Algorithm requirement

Algorithm architectural study

C/C++ (C TB) algorithm simulation

stimuli

bit to bit comparison

res

FPGA techno evaluation

ASIC techno evaluation

RTL VHDL algorithm coding

RTL VHDL (VHDL TB) algorithm simulation

res
Catapult SL – C flow

Processing requirement

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Catapult SL

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Constraints script

Lib ASIC

Lib FPGA
Catapult SL –C flow

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Constraints script
FOCUS ON

PHYSICAL SYNTHESIS
Physical Synthesis

Why to use Physical Synthesis?

- From 0.18 µm technology, timings after layout can’t be accurately predicted with a logical synthesis (at least 50 % of time spent in net)

- Potential timing problems need to be anticipated in order to avoid too many iterations with the foundry and so increase cost and schedule of layout phase

- In case many hard macros have to be placed

- In case of very congested designs
IC Compiler flow

Foundry
- Libraries
- Calibration factor
- Matrix definition (DEF)

Design Compiler
Topo netlist (verilog)

Timing constraints
file (SDC)

Macros placement
constraints (DEF)

IC COMPILER
(Synopsys)

Reports
- Congestion map
- Timing reports

Post-placement
netlist (verilog)

Timing
constraints file (SDC)

Placement of std cells
(DEF)
Conclusion

- Very interesting ASIC designs using all the capabilities of ATC18RHA technology
- Layout activities very complex having led to improvements in methodology / tools / TAS-Atmel team skills => already effective in on-going designs
- Strengthened experience on the ATC18RHA development flow, including Physical Synthesis and C-based Architectural Synthesis
- First use of CGA packages
- First run success for both designs : fully tested on EQM of DTP