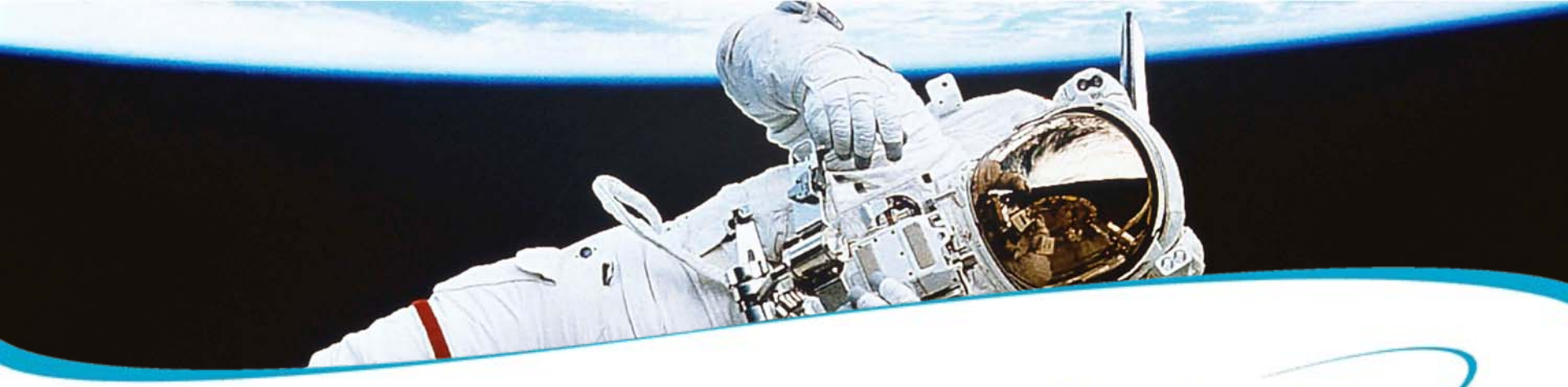


Microelectronics Presentation Days 2010

ThalesAlenia Space
A Thales / Finmeccanica Company

DTP ASICs experience feedback

Developed under ARTES3 ESA contract

Emmanuel Liégeon

Manager of ASIC/FPGA Design Group

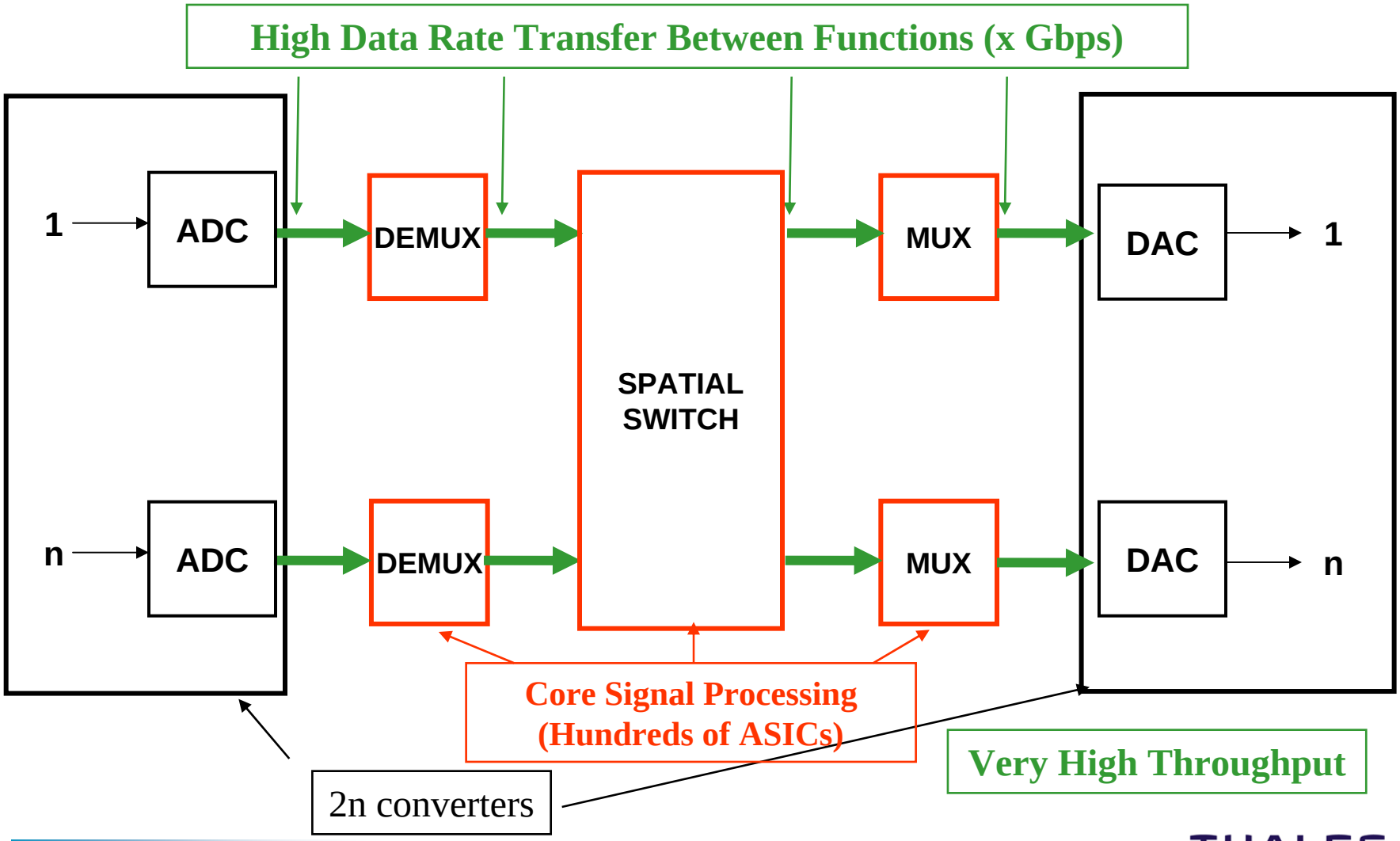
Thales Alenia Space Toulouse

THALES

Summary

- Context
- ASICs description
- Lessons learned
- Design flow
- Focus on C-based Architecture Synthesis
- Focus on Physical Synthesis
- Conclusion

Standard DTP architecture



CHAN ASIC main features (1/2)

CHAN ASIC

- MUX or DEMUX operation
- Main features

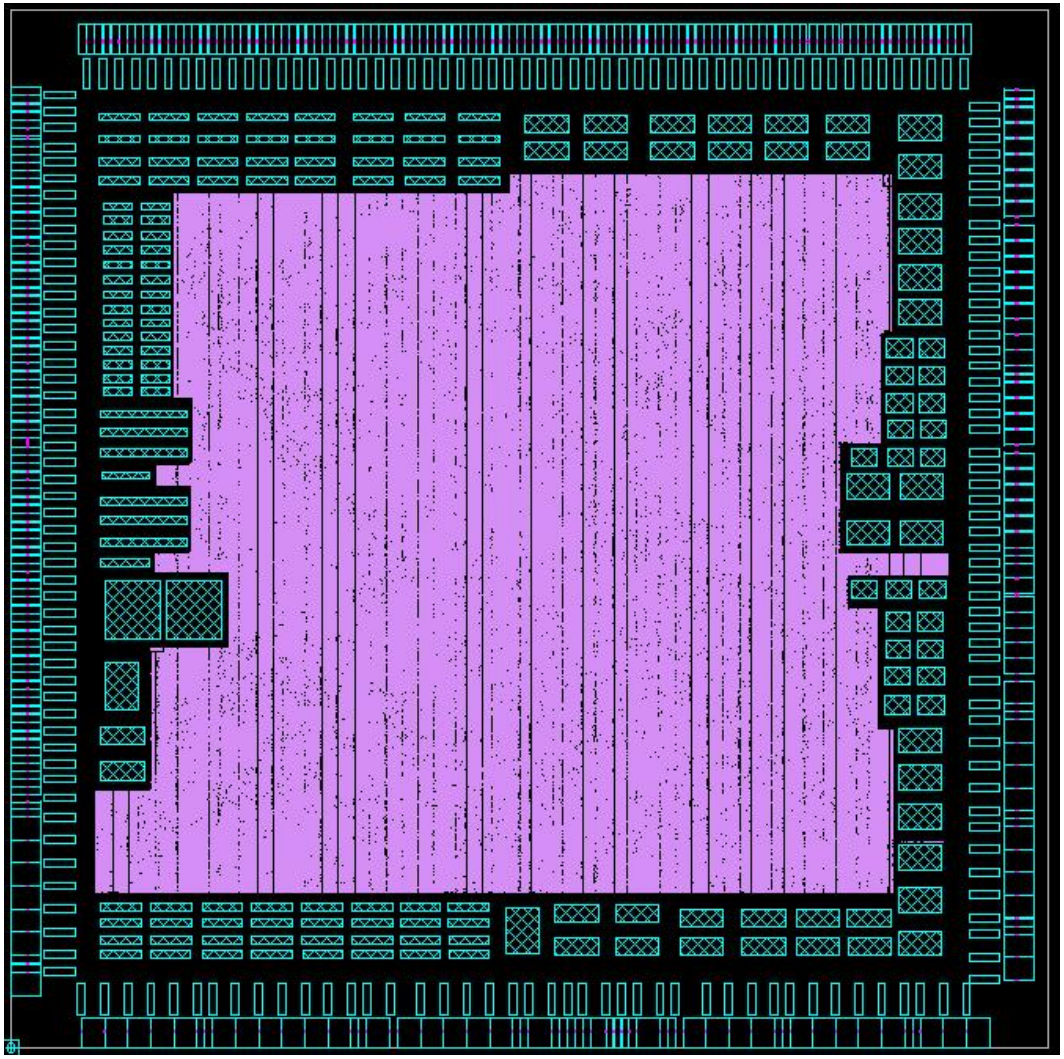
Name	CHAN
Working Frequency	Up to 350 MHz
Technology	ATC18RHA (ATMEL 0,18 µm)
Matrix	ATC18RHA95_504D (double padring) (4.8 M usable gates)
Package	MCGA
Core Power Supply Voltage	1.8 V
Periphery Power Supply Voltage	3.3 V
Estimated Power Consumption	9 W
Measured Power Consumption	6 W

- Prototypes delivered in 09/2009
- Prototypes fully tested on the DTP EQM

CHAN ASIC main features (2/2)

CHAN LAYOUT

- > 100 memory blocks
- 2 PLLs
- More than 48 clock domains



SW ASIC main features (1/2)

SW ASIC

- Switch operation
- Main features

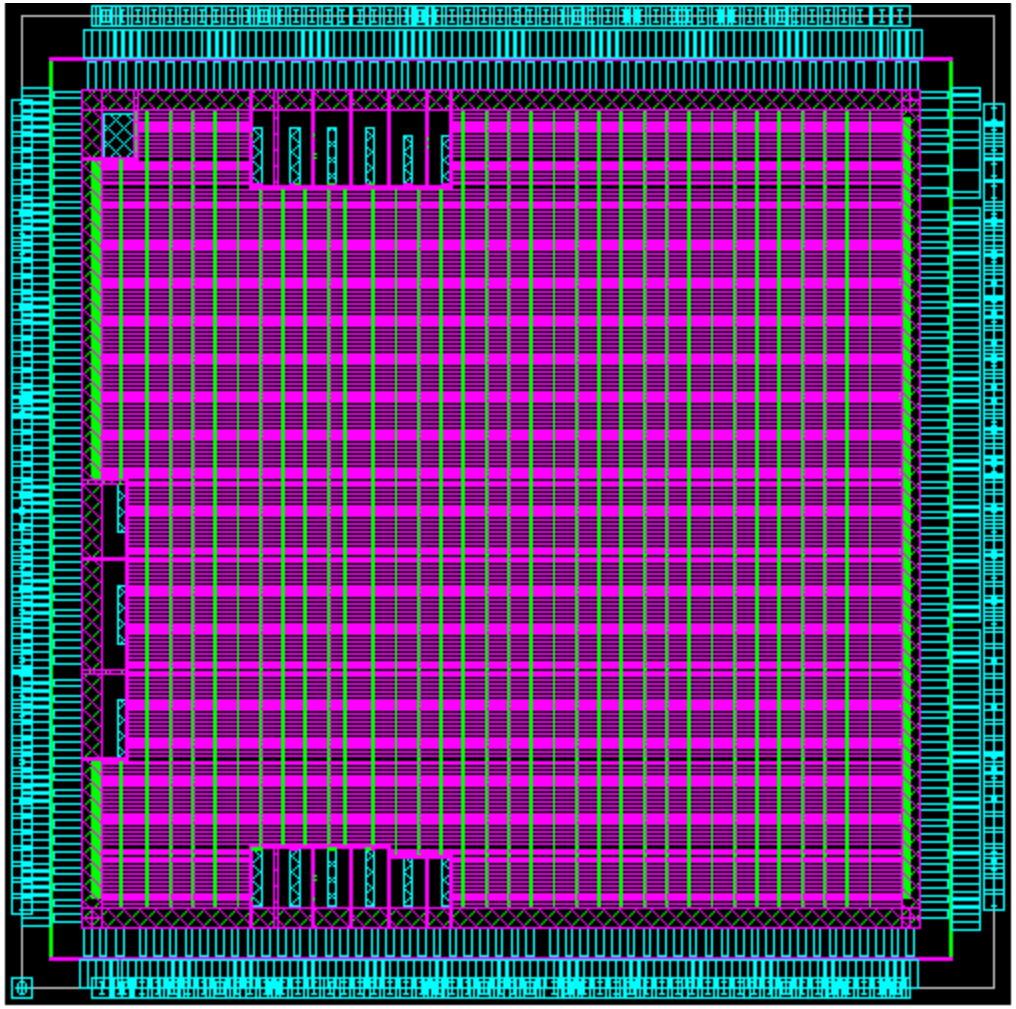
Name	SW
Working Frequency	Up to 150 MHz
Technology	ATC18RHA (ATMEL 0,18 µm)
Matrix	ATC18RHA95_504D (double padring) (4.8 M usable gates)
Package	MCGA
Core Power Supply Voltage	1.8 V
Periphery Power Supply Voltage	3.3 V
Estimated Power Consumption	6.2 W
Measured Power Consumption	5.8 W

- Prototypes delivered in 03/2009
- Prototypes fully tested on the DTP EQM

SW ASIC main features (2/2)

SW Layout

- some memory blocks
- 1 PLL
- > 20 clock domains



Lessons learned (1/2)

MCGA package

- difficulties to place n and p balls of LVDS signal close to each other
  - Atmel had to “grope” to obtain expected results
- No detailed RLC model of this package at the beginning of the project
  - Very long time to obtain this RLC model => ask it at the early beginning of the project

Pads

- No internal adaptation resistor between n and p pins in RX LVDS pads
  - These resistors had to be placed directly on the board
- No 2.5V pads library available at the beginning of the project
  - Use of 3.3V instead. This 2.5V library is now available

Lessons learned (2/2)

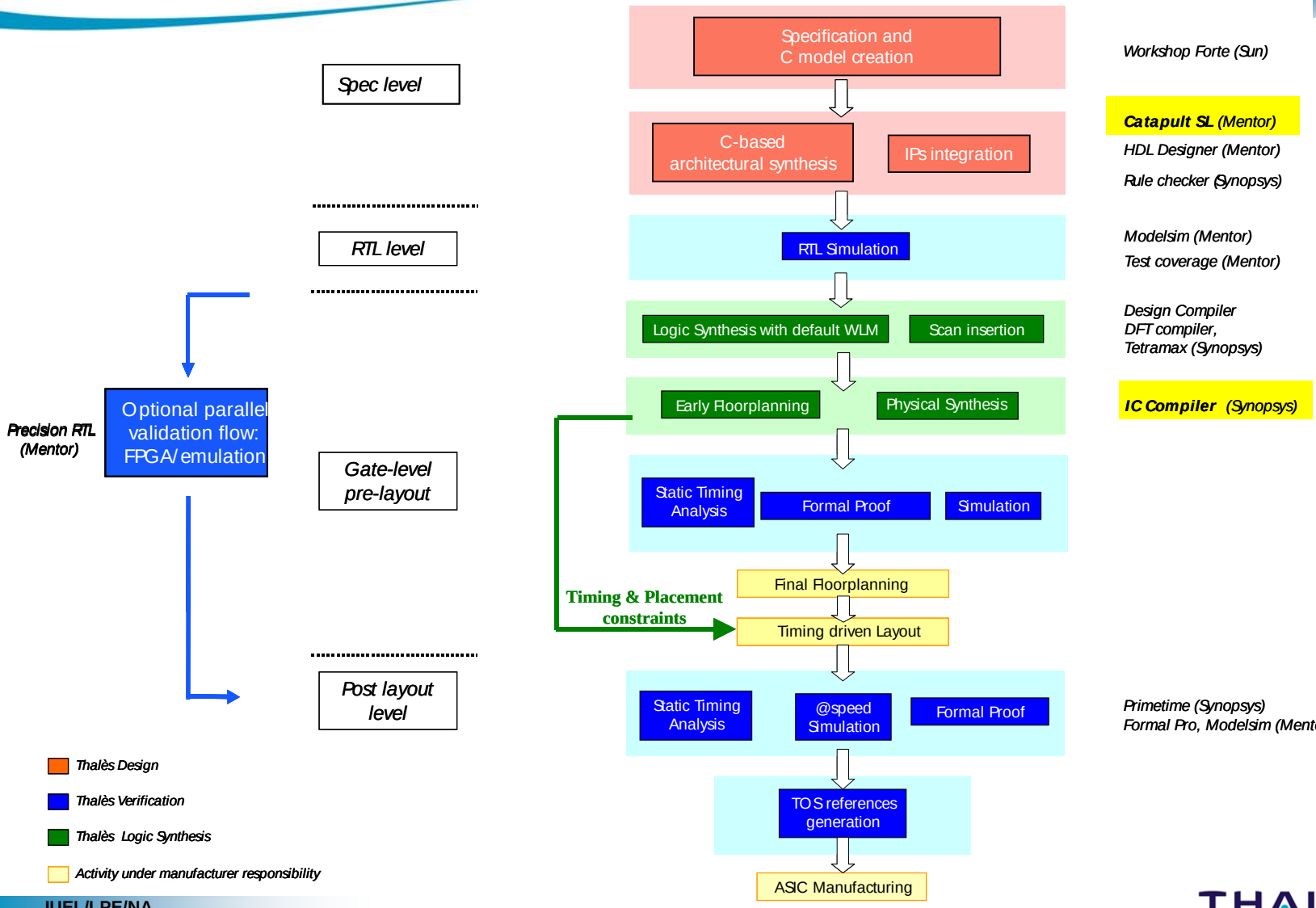
Clock trees

- CHAN had a lot of generated clocks (>48) and it was difficult to set an efficient approach with Atmel for the layout constraints
  - Many iterations but in the end, fully successful design
- MX04Dx and MX02Dx multiplexer rise/fall delay are not balanced
  - Clock pulse width issue on high frequency clock. Necessity to use standard logic cell instead of multiplexers on clock trees.

Memories

- Issue with the memories when the awt pin is used (timing arc seen by Synopsys between di and do in functional mode)
  - Use of set_disable_timing command

ATC18RHA design flow

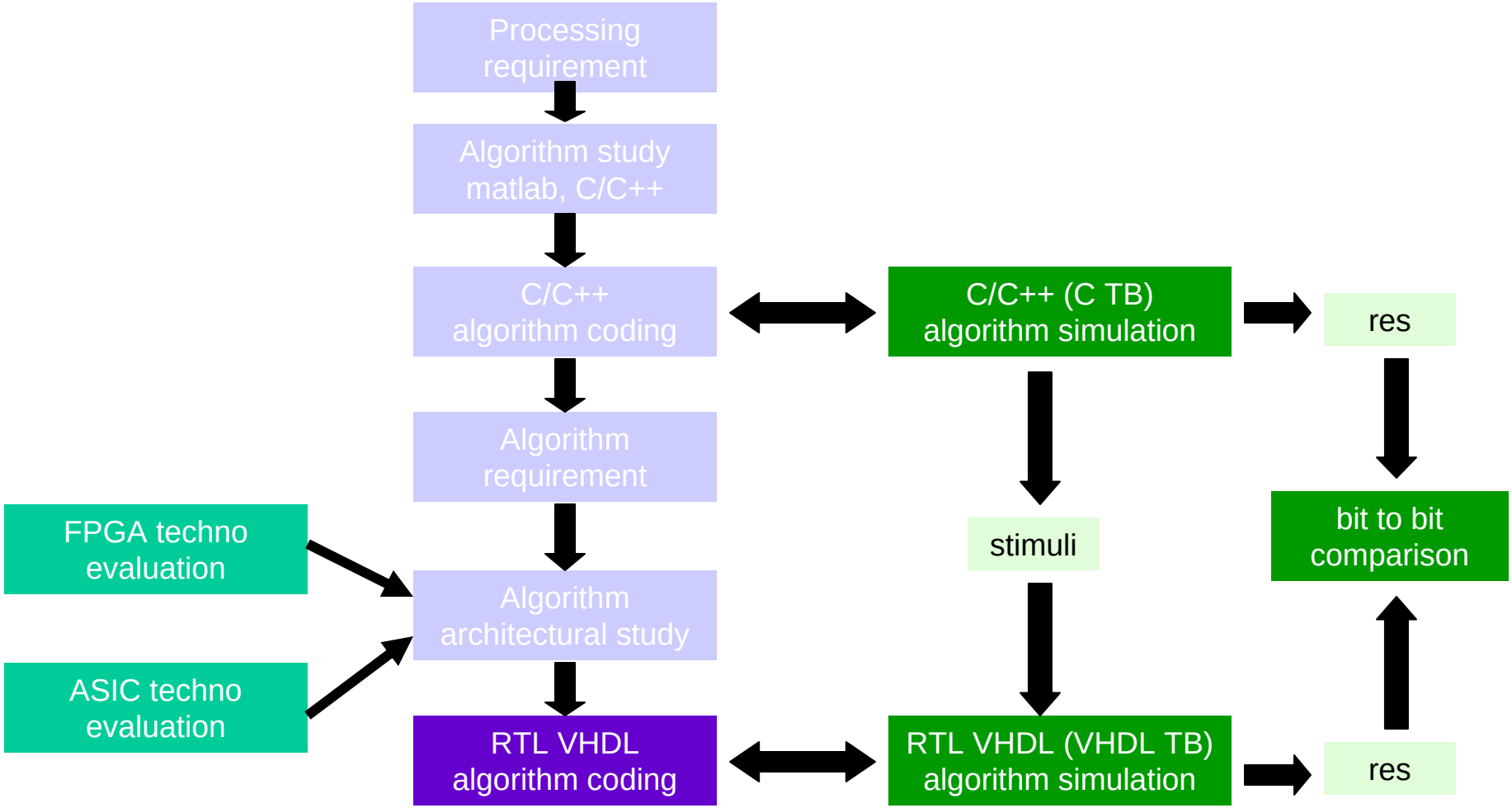


FOCUS ON

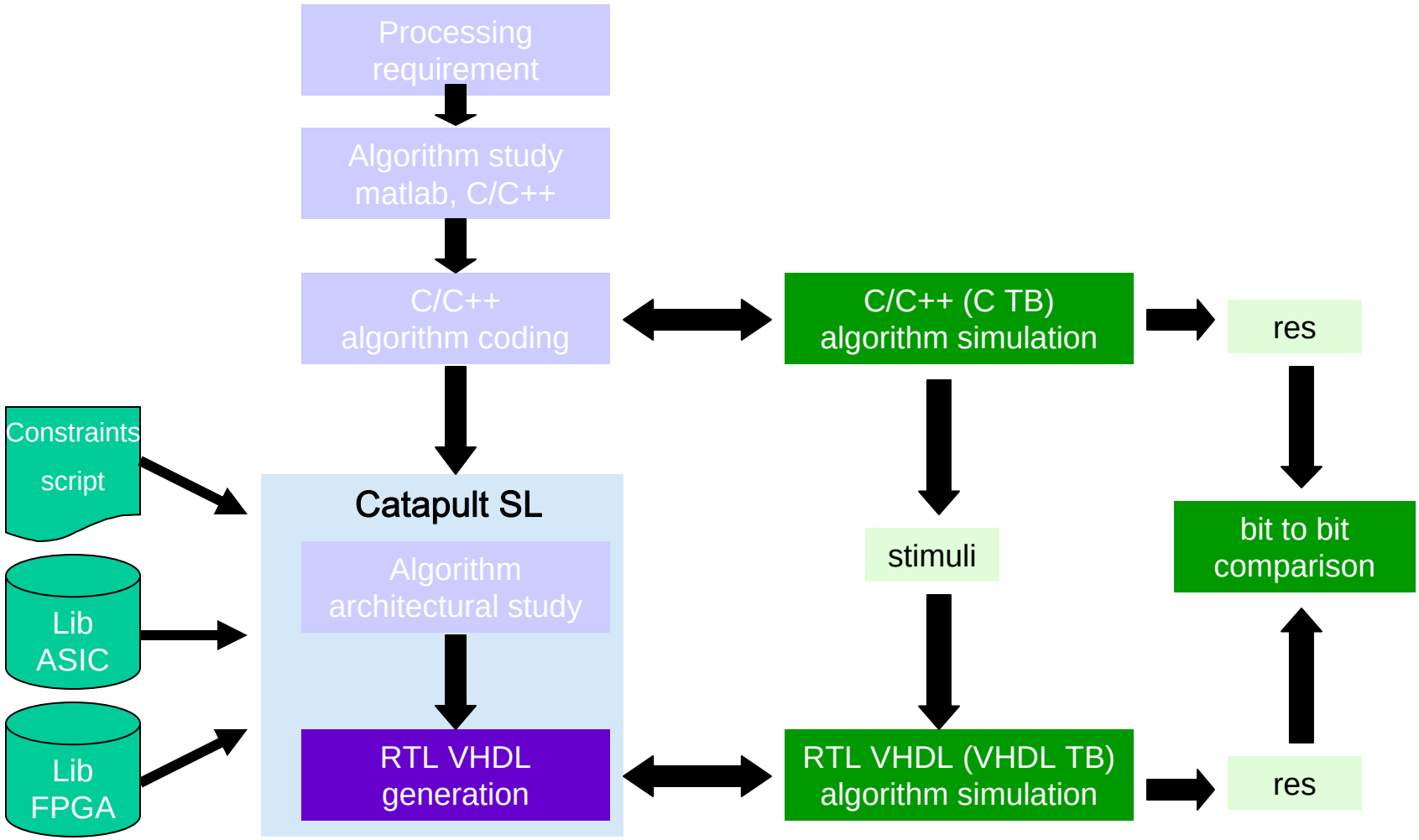
C-BASED

ARCHITECTURE SYNTHESIS

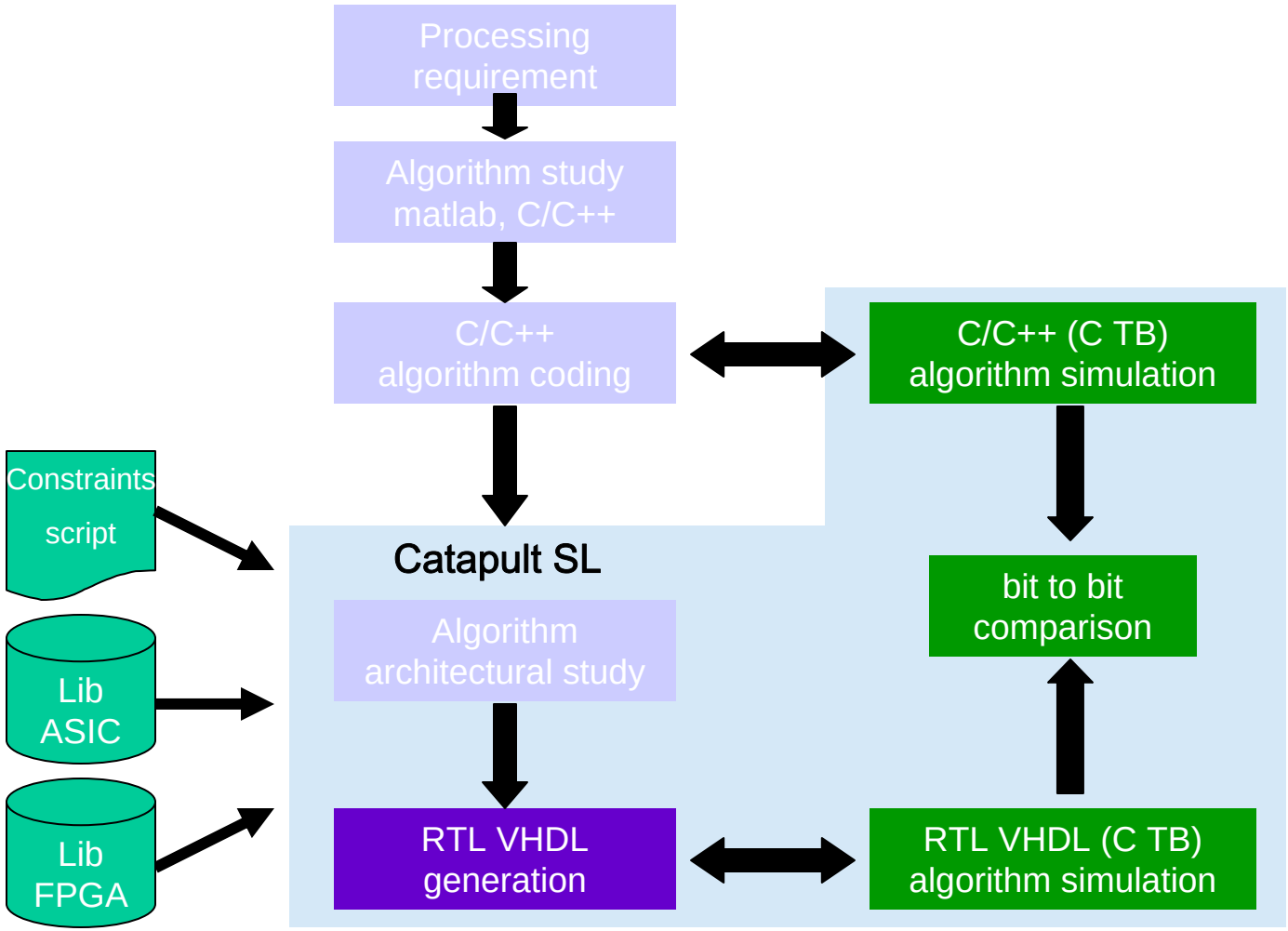
Standard flow



Catapult SL –C flow



Catapult SL –C flow



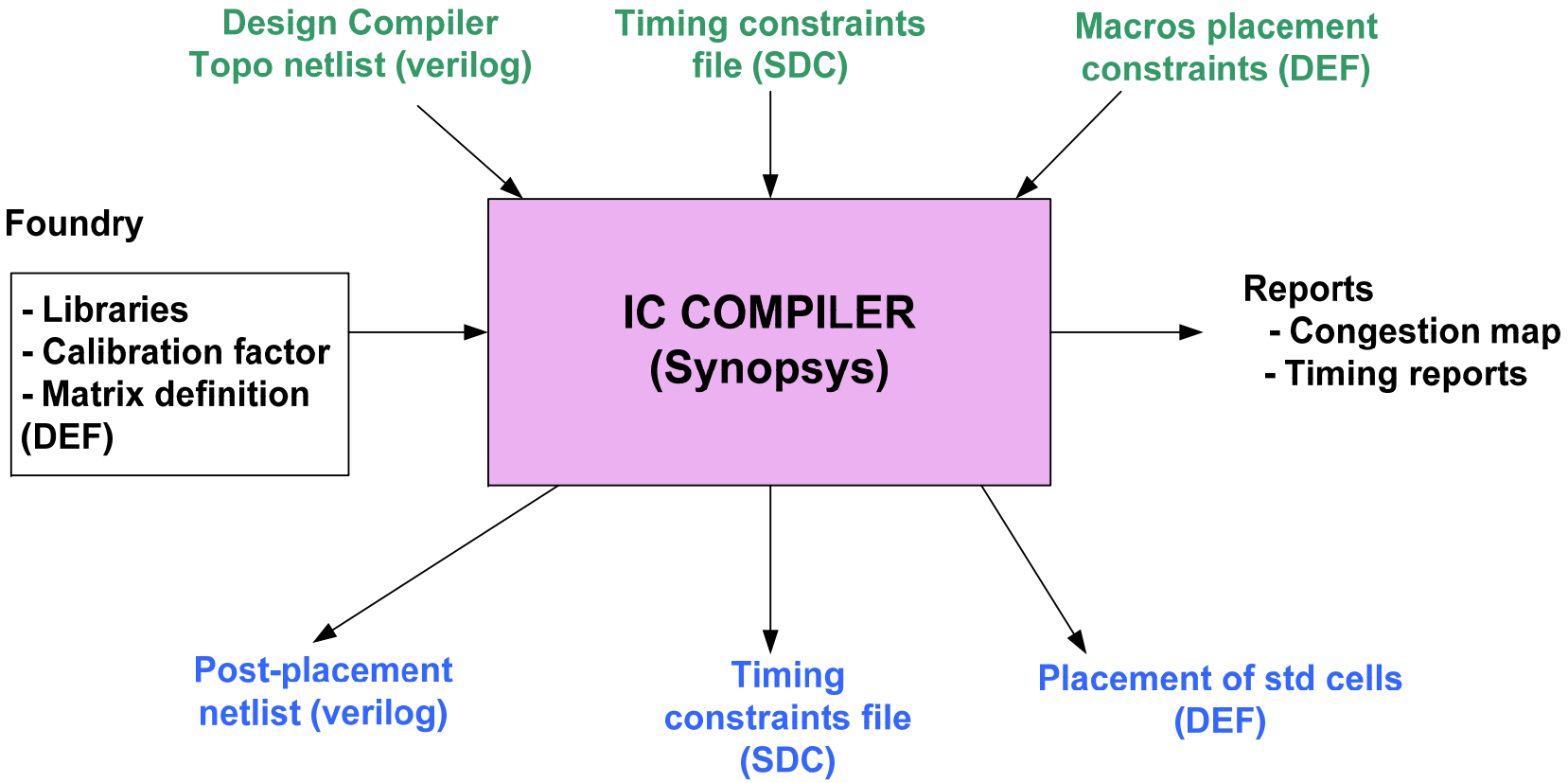
FOCUS ON

PHYSICAL SYNTHESIS

Why to use Physical Synthesis ?

- From 0.18 µm technology, timings after layout can't be accurately predicted with a logical synthesis (at least 50 % of time spent in net)
- Potential timing problems need to be anticipated in order to avoid too many iterations with the foundry and so increase cost and schedule of layout phase
- In case many hard macros have to be placed
- In case of very congested designs

IC Compiler flow



Conclusion

- Very interesting ASIC designs using all the capabilities of ATC18RHA technology
- Layout activities very complex having led to improvements in methodology / tools / TAS-Atmel team skills => already effective in on-going designs
- Strengthened experience on the ATC18RHA development flow, including Physical Synthesis and C-based Architectural Synthesis
- First use of CGA packages
- First run success for both designs : fully tested on EQM of DTP