SCOC3
Spacecraft Controller On a Chip with LEON3-FT

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Agenda

- **SCOC3 Features & Architecture**
- **Development status**
- **Lessons learnt**
- **Follow-up activities**
- **Conclusion**

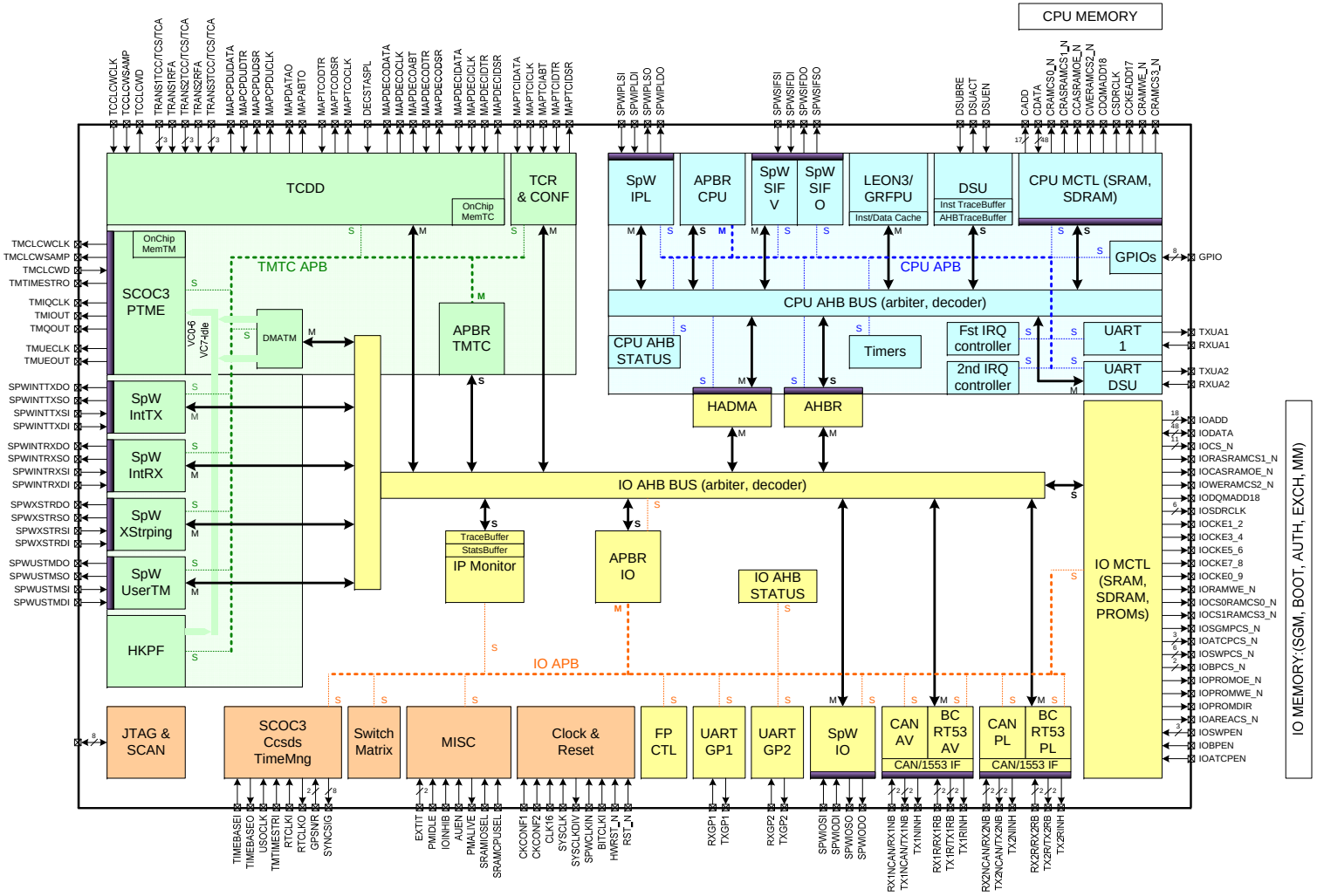
Some SCOC3 features

- SCOC3 is a System-On-Chip for Spacecraft Control and Data Handling, featuring:
  - The LEON3-FT processor (68MIPS@80MHz) with GRFPU-FT,
  - CCSDS TM/TC interfaces,
  - Various on-board interfaces (7 x Spacewire-RMAP, 2 x CAN, 2 x 1553, 4 x UART),
  - Time management and Event routing.

- Internal communication is distributed over a double AMBA-AHB bus structure with two separate *external IO* and *processor* memory ports. The two buses are linked by inter-bus bridges.

- **SCOC3 integrates functions which were before on several ASICs – small size in a qualified CCGA package, low power consumption and rad-tolerant technology.**

SCOC3 Architecture



A dual AHB bus architecture

- Latency and data throughput performances of on-chip data transfers are achieved with a system of two cross-coupled AHB buses (CPU AHB and IO AHB) =>
  - Reduced number of bus agents on each bus,
  - Improves timings (maximum clock frequency),
  - Allows operating the two buses at different clock frequencies,
  - Two memory ports (*external IO* and *processor*) to keep maximum performance of the processor

- Any master on the CPU AHB bus can access the APB busses and IO AHB. It is then possible to control SCOC3 through the UART DSU interface.

TM/TC interfaces integration

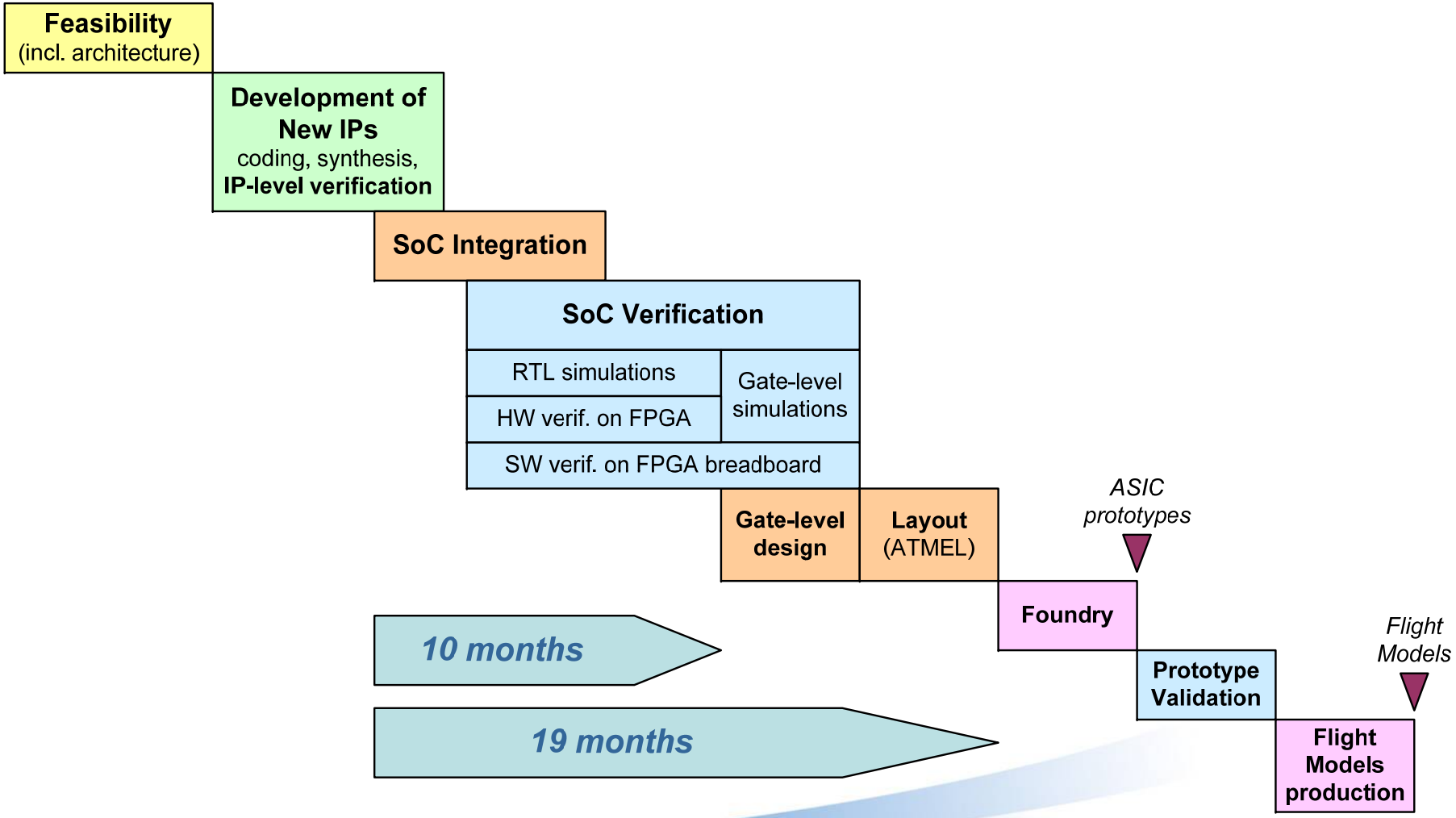
- **One of the main key points of SCOC3 is the integration of the complete CCSDS TM and TC protocols and interfaces.**

- TCDD (Packet Telecommand Decoder)
  - Provides all the functionalities of the TC system
  - A local memory enables to deal with authentication

- STME (SCOC3 Packet Telemetry Encoder)
  - Provides all the functionalities of the ground telemetry system (PTME),
  - The functionalities have been wrapped into a single module including an internal memory buffer.

- **SCOC3 can work as a powerful processor with the most needed peripherals including CCSDS TM/TC, or as a whole CCSDS TM/TC chip.**

SCOC3 Development



Development status and commercialisation

- Status:
  - SCOC3 is manufactured by ATMEL. Prototypes received in May 2009.
  - After an important hardware, software and system Prototype Validation, the first ASIC run has been declared successful in October 2009.
  - SCOC3 is now fully characterised and used for ASTROTERRA and SEOSAT computers.
  - SCOC3 Flight Models available in May 2010.

- Commercialisation:
  - SCOC3 is available and commercially released for any platform computers projects.

Lessons learnt: package

- The SCOC3 ASIC is based on a CCGA472 package. There have been problems in the space industry with the NTK interposer (SCI) for this package.
- As an alternative to the SCI NTK interposer used with current ATMEL CCGA package, SCOC3 could be also procured at LGA package: Hermetic package delivered with no columns.
- This alternative is under analysis at ASTRIUM, and would allow to assemble LGA with other columns than the NTK ones.

SCOC3 gate level characteristics

- SCOC3 matrix: ATC18RHA95_504D (pad limited choice)
- Matrix size: 13x13=169 mm²
- **Chip size area in the matrix (pads, logic, hard blocks): 57.7 mm²**
- Number of logic gates: 1.8 Mgates
- Number of DFFs: 55000
- Number of memory bits: 2.2 Mbits equivalent to 1.8 Mgates

Lessons learnt: tools

- Difficulty to estimate the real feasibility of such an ASIC due to the margins taken at each level (system, design, foundry)
- In the end, the ASIC is using less resources than planned in the matrix which is a good point for power consumption but is a drawback from a system/design estimation point of view.
- Synopsys dc_shell is not enough to perform good timing estimations. The use of dc_topo is greatly recommended.
- Formal proof/equivalence checking is now a *must have* rather than a *nice to have*.

Follow up activities (1)

- **SCOC3 will be established as an Application Specific Standard Product available to all users in the ESA member and participating states, and the following SW tool roadmap will be developed.**

- The software activity consists in developing:
  - A hardware software interface layer which is independent of the real time operating system.
  - A board support package adapted to the RTEMS operating system
  - Driver software functions which allow the use of main input output peripherals.
  - Interface test applications which will be delivered with the provided board.
  - A software environment development and RTEMS operating system associated tools.

Follow up activities (2)

- A development environment for SCOC3 will be provided to standardize the code production tools.
- The main part of the environment integrates the tools used for the development of flight software (C compiler and RTEMS OS).
- **SCOC3 technical support definition will also be addressed in these follow up activities.**

Customer complementary needs opportunities

- SCOC3 can be sold with a ***SCOC3 simulator*** under licensing for customer requiring software development in parallel with a board.

- A ***low-cost Starter Kit*** based on SCOC3 implemented in a XILINX will be available for software and systems developments. This starter kit is funded by CNES.

- Currently developed software runs under RTEMS OS.
  Other OS's might be available depending on funding and needs:
  - eCos
  - VxWorks up to 6.5
  - Linux, ThreadX, Nucleus…

Conclusion

- **EADS ASTRIUM has designed, manufactured and tested a high performance System-on-Chip for Space Computers, which provides a high level of integration**
- **The first SCOC3 Flight Models will be available in May 2010**
- **SCOC3 Simulator available – Low-cost Starter Kit, Drivers library, RTEMS BSP, SW dev environment available soon**