NGP-N ASIC

Microelectronics Presentation Days 2010

ESA contract: Next Generation Processor - Phase 2 (18428/06/N1/US) - Started: Dec 2006
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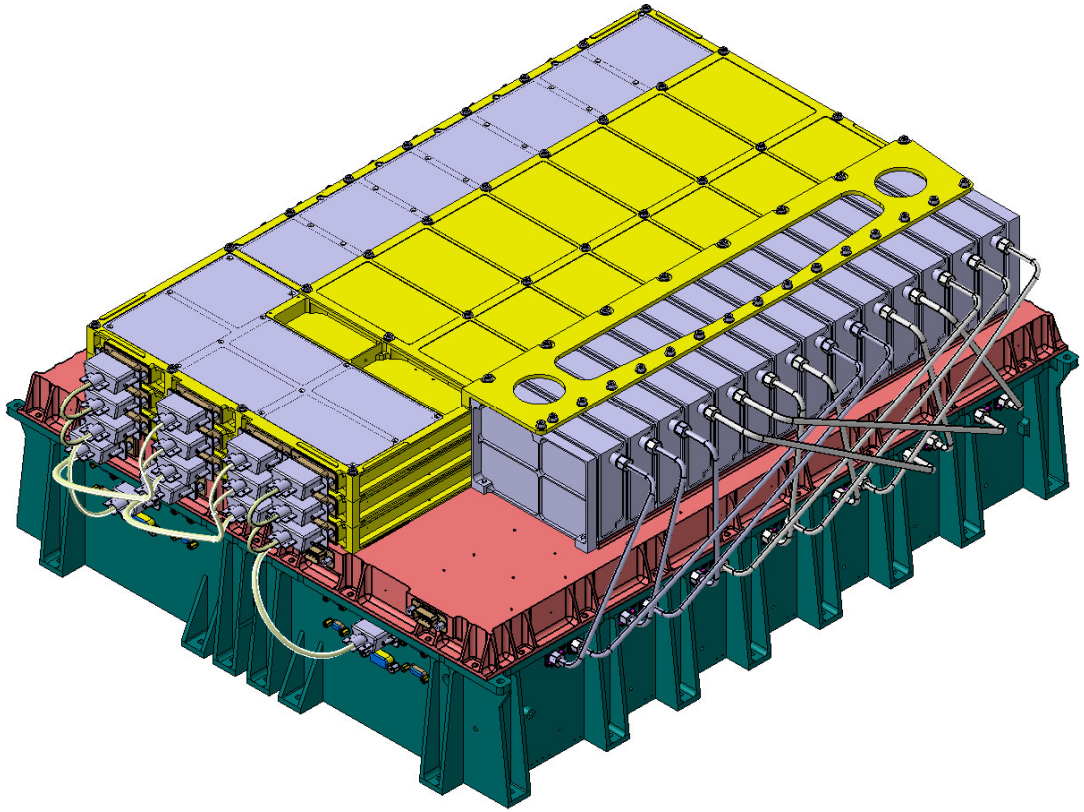
All the space you need

EADS astrium

Introduction

- Astrium Next Generation Processor (NGP) development funded under ARTES contract. Now being integrated into Alphasat XL mission.
- Generic transparent digital processor suitable for both narrowband (mobile) and broadband (fixed satellite service) missions.
- Modular processor architecture.
  - Signals from a variable number of modules can be combined to support a large number of digitally beam formed active antenna paths
  - Multiple modules controlled via Space Wire links from one central controller unit
- Integrated Processor (IP) concept consisting of:
  - Baseband digital signal processor (DSP)
  - Analogue pre- / post- processors mounted on top of the DSP
- Flexible DSP functions including
  - Fine granularity channelisation
  - Digital beam-forming and/or channel routing
  - Gain / level control on a per channel basis
- Single NGP ASIC design supports all digital processing functions

Next Generation Integrated Processor Module

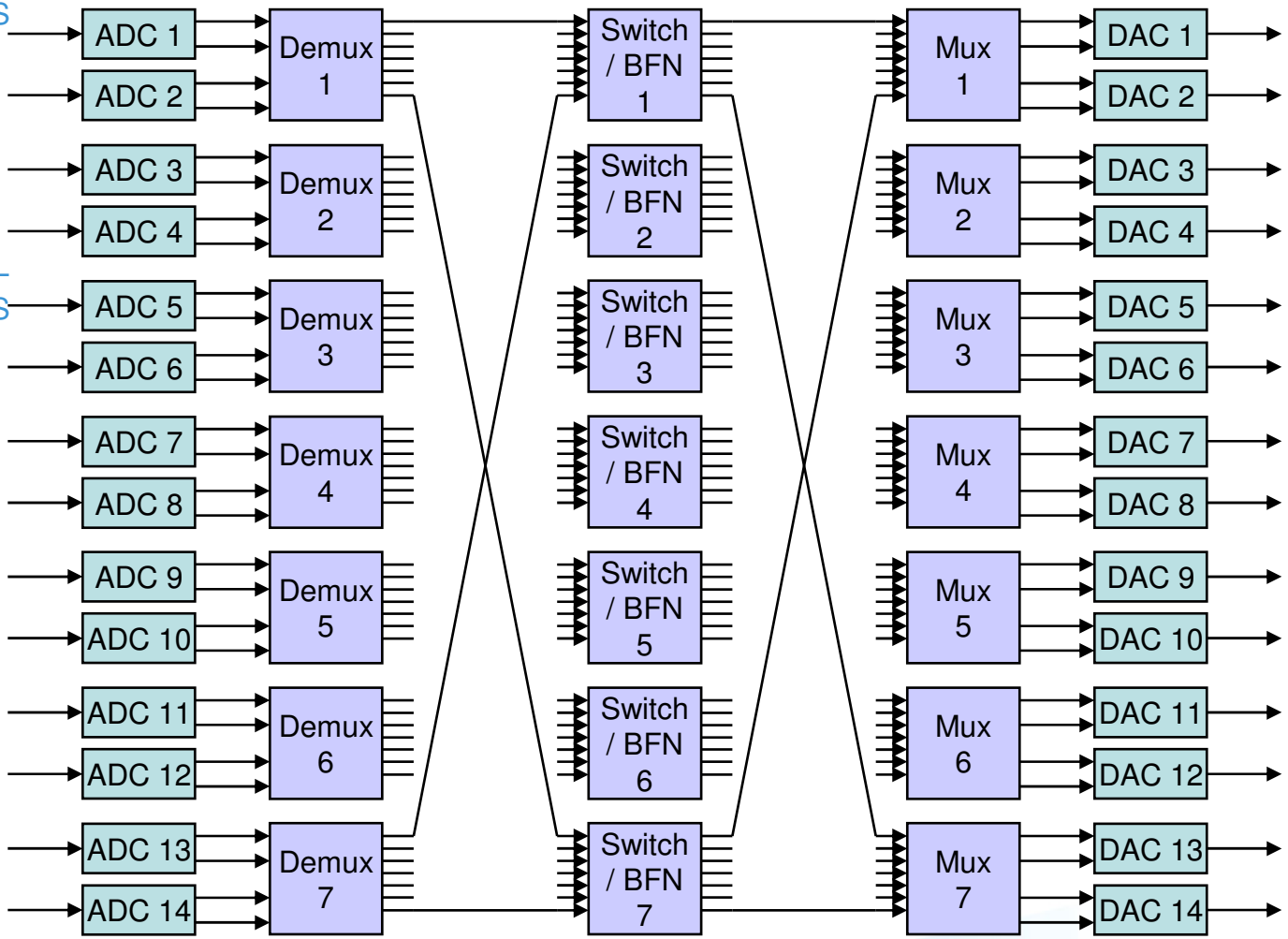


- Alphasat XL mission
  - 120 antenna elements
  - 41/48.5 MHz (FWD/RTN) processed bandwidth per element.
  - 200 KHz channelisation
- Requires:
  - Four Forward link IP modules
    - DSP + L-band Post-Processor
  - Four Return Link IP modules
    - L-band Pre-Processor + DSP
  - One central controller
  - 15 ASICs/DSP module
- Provides digital beam-forming for 120 active antenna elements over the extended L-band.

DSP Module Digital Processing Architecture

- ADC 640 MSPS
- ADC 10 bit
- Processed b/w: 250MHz

- For Alphasat XL
- ADC 384 MSPS

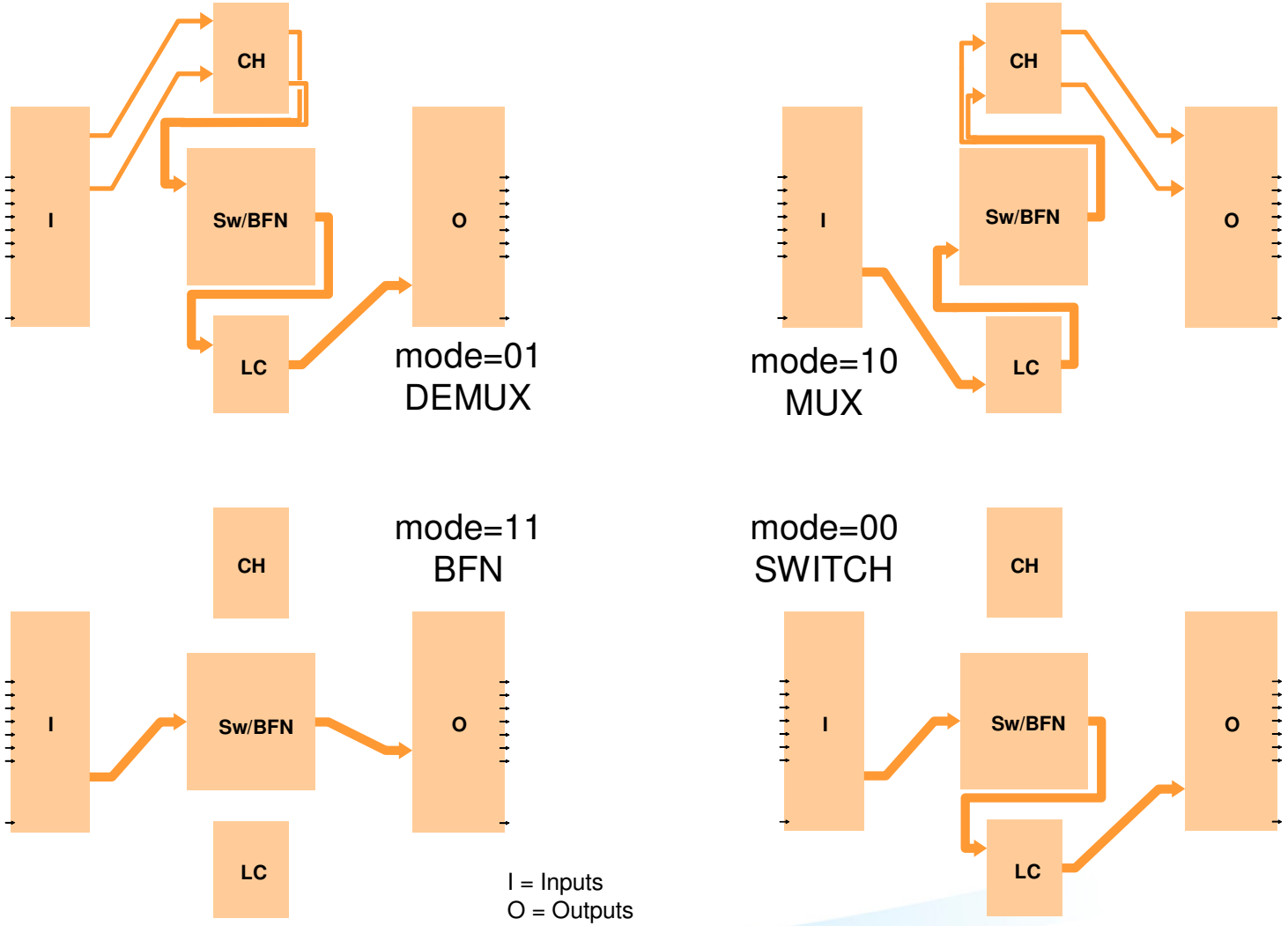


- DAC 640 MSPS
- DAC 10 bit used
- Processed b/w: 250MHz

ASIC Functional Characteristics

- Four major modes of operation
  - Demux, Switch, Beam-former and Mux
- LVDS I/O reused for ADC-ASIC, ASIC-ASIC and ASIC-DAC connections
  - Supports multiple ADC and DAC interfaces
- Data path functions include:
  - Channelisation (demux and mux)
    - Construct TDMs of separate channels
  - Switching (time and spatial switches)
  - Digital beam forming
  - Gain and automatic level control
  - Synchronisation functions (due to uncertain delays) - PI
- Controlled via a Space Wire interface
  - Each ASIC includes a 4 way SpW router to support routing for various configurations of populated ASIC and internal redundancy.
  - 0.25 Mbits of configurable coefficients per ASIC (mode dependent)
  - Encoded configuration data for SEU protection (error detection)
  - Attention request mechanism to flag errors to external controller

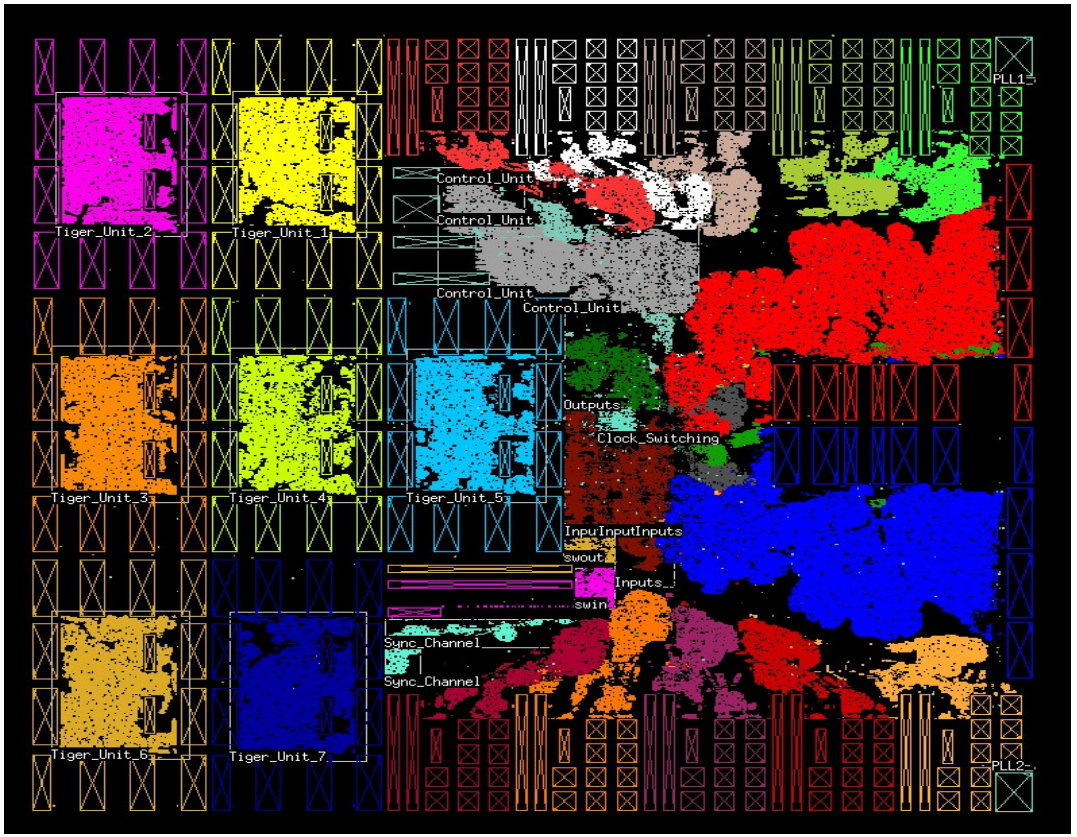
ASIC Dataflow (4 major modes)



I = Inputs
O = Outputs
CH = Channeliser
Sw/BFN = Switch / Beam-former
LC = Level Control

Layout

- Routing Congestion
  - RAM routing restrictions
- RAM (>200) placement
- Block level layout
  - Tiger logic constrained
- I/O timing
  - Multiple LVDS
  - Balanced clocks
  - Delay matching
- Timing closure
  - Multiple clock domains (>80)
  - Multiple IO modes
- Power Grid
  - RAM blocking
- Layout iterations
  - Many more than expected
- Suggestions
  - Floor planning tools
  - Physical synthesis

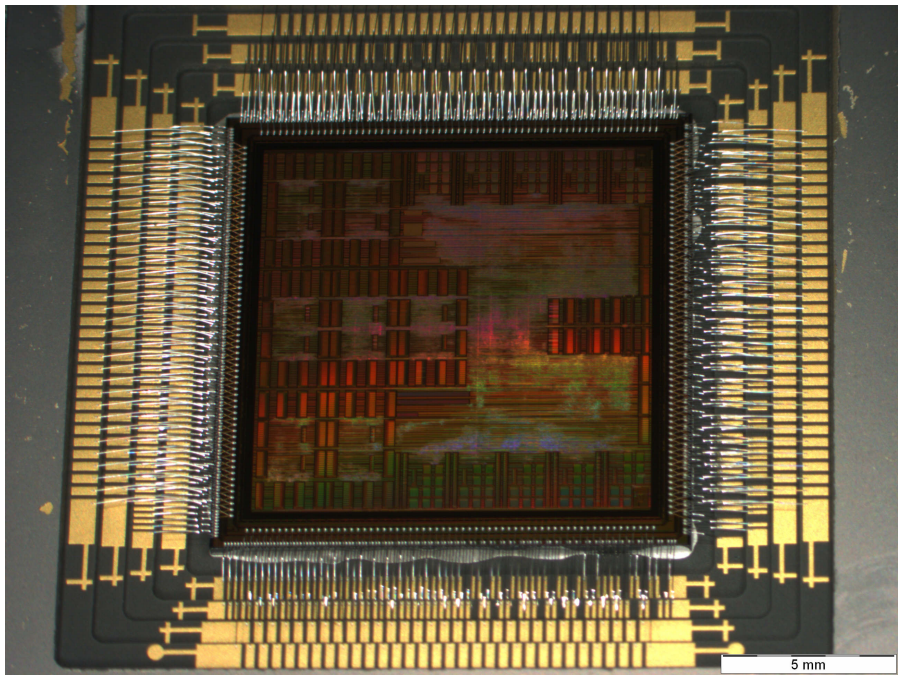


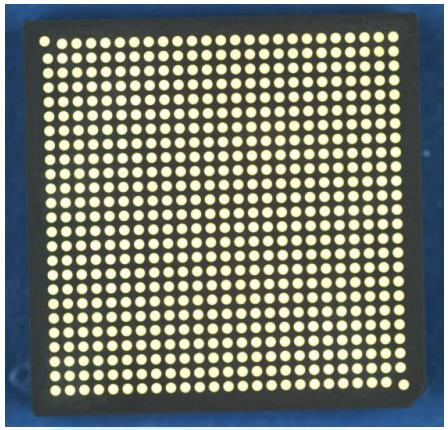
Statistics

- Gates 2.2M gates
- RAMs 3.1M Bits in 255 instances
- I/O buffers (pins) 235 (398)
- Clocking rate 320MHz max/160MHz most logic
- I/O Data Rates 160MHz – 320Mbps
- Power estimation
  - Pre-layout estimates in line with expectation
  - 640MHz, 1V8, 6 active inputs and outputs
  - DEMUX 7.9W
  - SWITCH 4.2W
  - MUX 7.5W

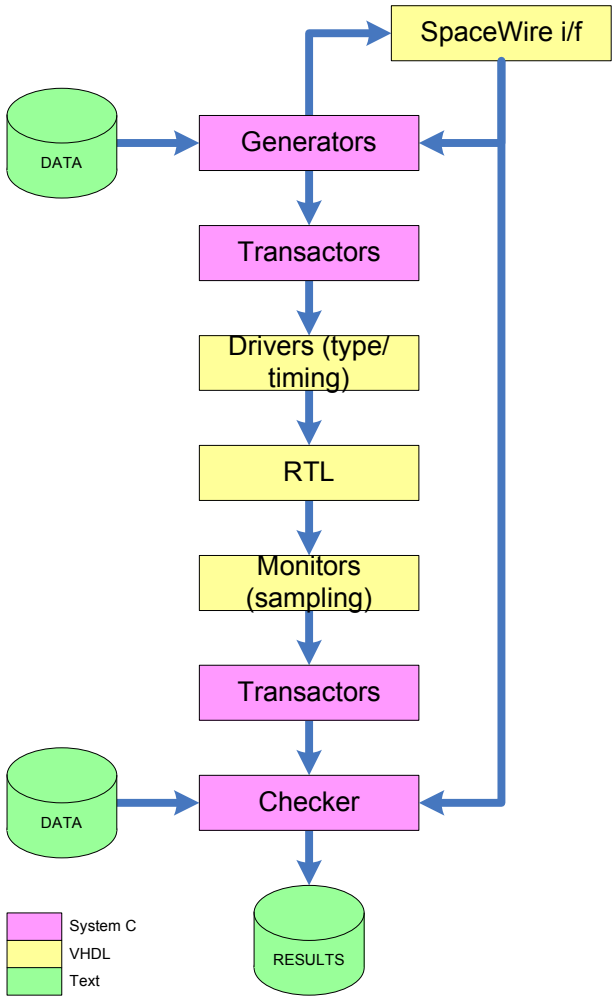
Technology

- ATMEL ATC18RHA
  - 0.18 µm
  - 85 nW/gate/MHz @100% toggle rate
  - 1.8V core supply
  - 2.5V buffer supply
  - TID of 300 kRad
- Array is ATC18RHA95_544_252
  - 796 buffer sites – dual pad ring
  - 132 mm^2 core area
- Package 625 LGA



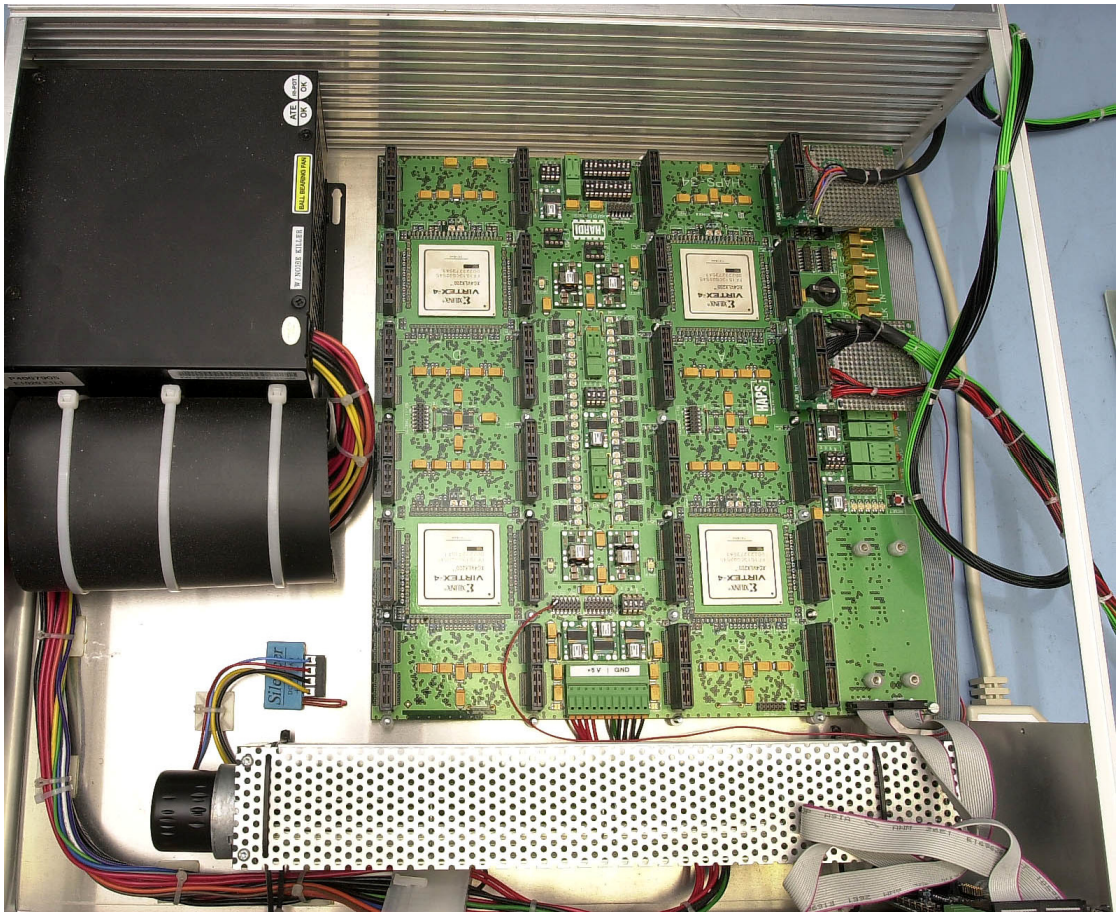


Verification Platform (Simulation)



- Very challenging verification task
  - Implementation spec >300 pages
  - SoC for each requirement
- Block level – treated as smaller chip
  - Allowed block(s) to be finished independently
- Common test bench
  - Important to maximise test bench reuse
  - Written in mixed System-C/VHDL
  - Near generic design for top-level use
  - Single reconfigurable bench for all major ASIC functional modes
  - Controlled via tcl scripts
  - Contains full Space Wire interface
  - Designed to support generation of production vectors

Verification Platform (FPGA Prototyping)



- Commercial HAPS board
- Four large Xilinx Virtex FPGAs
- Prototyping performed for:
  - Full RTL for one ASIC
  - Control functionality for 21 ASICs forming one module
- Prototyping used to verify:
  - Automatic level control function
    - Embedded test bench
  - Space Wire configuration of all ASIC coefficients (0.25 Mbits configuration data per ASIC)
- Test bed controlled via Space Wire test system & software
  - S/W developed in house - GUI
  - Coefficient control and monitor
  - Collects Attention Requests

Conclusions

- Extremely large and complex ASIC development
  - Stretching the technology in all parameters: area, speed and I/O.
- ASICs have been manufactured and tested
  - Full functionality has been verified to be right first time.
- ASIC core power dissipation has been measured
  - Found to be close to and slightly below the estimates.
- FPGA prototyping proven invaluable in the verification
  - Covering situations that would be too lengthy to simulate.
- ASICs will be flown on the Alphasat XL mission
  - Provide extended L-band mobile services for Inmarsat on the new Alphabus platform.