Overview of ESA activities on FPGA technology

Microelectronics Presentation Days

David Merodio Codinachs
European Space Agency
Microelectronics Section (TEC-EDM)
Acknowledgments

- Thanks to all colleagues who contributed from
  - TEC-ED
  - TEC-QCT
  - TEC-QEC
  - Catherine Morlet

- And all the industry, universities and institutes working on the mentioned activities
Outline

- **Introduction**
  - FPGA usage aspects
  - Activities covering the different FPGA aspects

- **European FPGAs**

- **SEE-related activities**
  - Static tools for FPGA radiation hardness assessment
  - Dynamic tools for FPGA radiation hardness: Fault Injection
  - Radiation testing

- **Quality-related activity**
  - PPBI

- **Application Reconfigurability-related activities**
  - Reconfigurable Regenerative Processor (Software Defined Radio)
  - DRPM
  - NPI

- **Conclusions**
FPGA Introduction: aspects

- In the FPGA usage there are different aspects (not exhaustive list):
  - (asp1) Capacity and performance (frequency and power consumption)
    » Related to the internal architecture and technology node used
  - (asp2) Radiation hardness
    » Addressed at different levels:
      ◆ Process
      ◆ Transistor/ Standard Cell
      ◆ Register Transfer (RTL)
      ◆ System
  - (asp3) Quality
  - (asp4) Reconfigurability

- Others:
  » ITAR (International Traffic in Arms Regulations)
    The regulations are described in Title 22 (Foreign Relations), Chapter I (Department of State), Subchapter M of the Code of Federal Regulations.
  » Cost
  » …
Rad-Hard FPGA Capacity Overview
FPGA for Space: activities summary

- **Activities related to the previous aspects:**
  - SEE mitigation and verification (related to asp2, Radiation Hardness)
    » Radiation testing
      - Actel ProASIC3 FPGAs
      - Atmel FPGAs (Atmel, under CNES contract)
      - Xilinx Virtex-II (in the past)
    » Static and dynamic tools
      - SST, STAR, RoRA, VPLACE, INFAULT, SUSANNA/JONATHAN
      - FT-UNSHADES/2, FLIPPER
  - Quality assurance (related to asp3, Quality)
    » Post Programming Burn-In (PPBI) for antifuse-based FPGAs
  - Application: (related to asp4, Reconfigurability)
    » Software Defined Radio (SDR)
    » DRPM
    » NPI: Reliability-aware design methodology for embedded systems on multi-FPGA platforms
Other activities: European FPGAs

CNES and ESA are supporting European reprogrammable space FPGA developments, based on ATMEL expertise and technology, with JAXA/HIREC/OKI support

Related to aspects (a1, a2, a3, a4)

- 40K & 280Kgates FPGA DK capabilities evaluation (for ESA IP Cores) (ESA Funding)
- 450 Kgates FPGA/SOI Validation Phase (ATMEL/OKI/HIREC) (CNES Funding)
- 280 Kgates FPGA + 4 Mbit EEPROM in one package (CNES Funding)
- Reprogrammable Computer in one package: LEON2 AT697F + 280 Kgates FPGA in one package (CNES Funding)
- FPGA 280Kgates ESCC Evaluation (ESA Funding)
- FPGA/SOI 450 Kgates development (JAXA/CNES/ATMEL/OKI/HIREC) (CNES + JAXA Funding)
- Challenge: to raise funding for >1Mgates European space reprog. FPGA. Based on Abound Logic IP and Atmel RHbD technology. Negotiations at different levels ongoing
The following website is the Atmel FPGA User’s Group:
SEE and FPGAs overview (asp2)

- **Atmel**
  - Rad-hard by design

- **Actel**
  - Antifuse:
    - No SEEs in the antifuses; DFFs rad hard at transistor level
    - Memories are not Rad-Hard
    - SETs to be considered (depending on target frequency)
  - Flash:
    - Not rad-hard; configuration Flash very resistant to SEUs
    - TID and SETs to be considered

- **Xilinx**
  - QPRo family:
    - No rad-hard; (SEUs in both configuration memory and user design; SEFIs)
    - Mitigation techniques required (consider scrubbing, TMR, …)

- **Aeroflex**
  - Antifuse, rad-hard DFFs and memories
FPGA radiation testing: RT ProASIC3

- A radiation test activity is ongoing under ESA contract; with a duration of 12 months

- Objective:
  - Get further insight in the radiation sensitivity of RT ProASIC3 FPGAs by performing
    » Heavy ion SEE tests
    » Proton SEE tests
    » Co-60 TID tests
  - Main concern of this FPGA are:
    » SET sensitiveness
    » TID sensitiveness (currently published as 15 Krad for programming functionality)

- Current status: TRR is scheduled April 16 at RADEF
Before starting with tools...

- On Sep 11\textsuperscript{th} 2009 at ESA took place the Workshop on Fault Injection & Fault Tolerance in space FPGAs. The information is available at:

  \texttt{http://www.esa.int/TEC/Microelectronics/SEMV57KIWZF_0.html}
XTMR cross-section added value

- **Data from []**
- **Device:**
  - XQR3V3000
  - Die size ~16x16 mm²

- **Results:**
  - 2 clock: XTMR not active
  - 3 clock: XTMR active

Clear added value when using XTMR ....
BUT, is it enough?

---

**Fig 6.5** Recorded cross sections for the modules FFT, FFmatrix, LUTmatrix and M18matrix plotted as a function of LET for the V2 design variant. Data are only shown for test runs with low flux.
More than XTMR required

- In spite of (X)TMR, single point failures (SPF) still exist
  - Optimization during layout leads to close-proximity implementation
    » Flipping one bit may create a short between two voter domains
    » Flipping one bit may change a constant (0 or 1) used in two domains
  - Malfunction in two domains at a time can not be voted out any more

- What else? STAR/RoRA/VPLACE; FLIPPER
**STAR/RoRA/VPLACE (II)**

🔹 **STAR: WHAT IS IT?**

- SW tool to analyze the configuration memory of Xilinx (Virtex-II and Virtex-4 devices) to **identify sensitive bits**.
- A bit (programmed or not) is sensitive if it controls resources used by the implemented circuit.

🔹 **WHAT CAN IT DO?**

- **Discovery mode**: identify all bits that if upset modify the implemented circuit -> support fault injection in meaningful parts of the configuration memory.
- **TMR mode**: identify all bits (programmed or not) that if upset overcome (X)TMR mitigation scheme -> support validation of designs.
- Correlate bits in the configuration memory with EDIF design resources-> support debug.
**STAR/RoRA/VPLACE (II)**

- **RoRA/VPLACE: WHAT IS IT?**
  - SW tool to fix domain crossing events that may escape (X)TMR Xilinx (Virtex-II and Virtex-4 devices).

- **WHAT CAN IT DO?**
  - Generate user constraint file for segregating (X)TMR domains in safe locations
  - Re-route critical nets to avoid domain crossing events
  - Seamless integration with standard synthesis/P&R flow
New results (preliminary):

- Analysis and hardening of a subset of the Reconfigurable Regenerative Processor (RRP): MTD
- MTD preliminary analysis and hardening flow
- Device: Xilinx Virtex-IV XC4VLX160

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Sensitive bits</th>
<th>Max Delay [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>MTD plain circuit</td>
<td>496,235</td>
<td>8.883</td>
</tr>
<tr>
<td>(STAR discovery mode)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MTD X-TMR</td>
<td>38,392</td>
<td>10.972</td>
</tr>
<tr>
<td>(STAR TMR failure)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MTD V-PLACE</td>
<td>17,385</td>
<td>9.886</td>
</tr>
<tr>
<td>MTD V-PLACE / RoRA</td>
<td>13,712</td>
<td>9.915</td>
</tr>
</tbody>
</table>
**SUSANNA / JONATHAN (I)**

- **WHAT IS IT?**
  - **Susanna**: SW tool to analyze the configuration memory of Atmel (AT40k and ATF280E devices) to identify sensitive bits.
  - **Jonathan**: SW tool to correlate sensitive bits to design instance.

- **WHAT CAN IT DO?**
  - **Susanna**: identify all bits that if upset modify the implemented circuit -> support fault injection.
  - **Jonathan**: Correlate bits in the configuration memory with design resources
    -> detection most sensitive module of design
    -> support debug
Several benchmark circuits of the ITC’’99 set:
- Not all the programming bits for a used resource are potentially critical
- A not programmed bit can induce an error in the circuit
- Placement and routing strategies affect the reliability of the design

The estimation is pessimistic

Critical bits are afterwards validated using fault injection
FLIPPER (I)

◆ WHAT IS IT?
  ➔ FLIPPER started in 2004
  ➔ injects bit-flips in XILINX configuration memory by partial re-configuration
  ➔ HW platform + SW application running on PC
  ➔ DUT is XQR2V6000 hosted on a piggy-back board; Update to Virtex-4 planned.
  ➔ Functional test vectors + expected output values are imported by the SW application from an external HDL simulator

◆ WHAT CAN IT DO?
  ➔ Identify design sensitive configuration bits with respect to the applied set of test vectors – systematic injections
  ➔ Mimics SEU irradiation tests (bit-flip accumulation) – random injections
  ➔ Evaluates the impact of critical bits for a given workload – specific injections
**FLIPPER (II)**

- **FLIPPER : comparing mitigation efficiency and predictions vs rad tests**
  - FLIPPER fault injection analyses to predict cumulative failure probability
  - Benchmark design with 2 protection variants (V1, V2)
    - V1: applying XTMR directly to unprotected design
    - V2: XTMR with a voter for every flip-flop
  - Beam time @PSI (CH) 180 MeVproton
    - average flux: $6.28 \cdot 107\text{cm}^{-2}\text{s}^{-1}$ CBU at most during test vector application—CBUrate: $\sim 82\text{s}^{-1}$
    - stimuli: $\sim 28,000\text{ vectors}\@10\text{ MHz}$
    - total exposure time: $\sim 8\text{hours}$
    - Fluence: $\sim 2.19 \cdot 10^{12}\text{p}/\text{cm}^{-2}$
    - TID: $< 140\text{ krad}$
**FLIPPER (III)**

- **Some results from FLIPPER (from [TNS-00709-2009])**
  
  For most of the designs, the systematic use of voters for all flip-flops (V2) improves the robustness against accumulated SEU compared to the default XTMR solution (V1), where only feedback paths are voted.

  However it is not true for all design modules, for the FFT, V1 is even more robust than V2.

  This is due to the fact that the XTMR-ed version of the FFT module already includes a voter for each flip-flop; V2, thus, only adds superfluous muxes that, as expected, increase SEU sensitivity without improving protection.
**FT-UNSHADES 2: fast update**

- **Expected Results:**
  - Evolution of the former FT-UNSHADES system
  - High speed fault injection tool
  - Flexible evaluation of digital designs (hierarchical)
  - Zero effort for the preparation process
  - High injection rate combined with detailed analysis in the same tool
  - Remote access for IP preserve
Quality: PPBI

- **Post Programming Burn In**
  - ESA has started an activity to facilitate NRE costs on the PPBI that Actel is providing via SERMA

- **Details on the current offer available**
  - Actel can be contacted during MPD for more details and comments

- **PPBI Dedicated meeting took place at ESTEC on 2\textsuperscript{nd} March 2010**
  - Agencies, Industry, Test Houses and Actel were present
  - Information available upon request
Reconfigurability: SDR (I)

- **Reconfigurable Regenerative Processor - Software Defined Radio (SDR):**
  
  » Processor Signal Processing Chain:

![Diagram of the processor signal processing chain]

- **Reconfigurability levels (possible classification):**

  ➔ Full reconfiguration:
  
  » Full reconfiguration of the processor with new algorithms

  ➔ **Partial reconfiguration with new/upgrade algorithms:**
  
  » Only a portion of the design in the FPGA gets reconfigured

  ➔ **Parameters modification:**
  
  » Affects only the parameters (same as with SW)

  ➔ **Add-on algorithms:**
  
  » Adding one or more algorithms to the current chain.
Reconfigurability: SDR (II)

- **Current status:**
  - Activity to be finished in 2Q10
  - TRR already successful and final test execution is ongoing
  - CCN foreseen in order to include radiation mitigation techniques in the full demonstrator.

**RRP:** Reconfigurable Regenerative Processor
Reconfigurability: GMDR (I)

- FPGA Based Generic Module and Dynamic Reconfigurator:
  
  **Activity Objectives:**
  
  - Design, develop a payload data processing module demonstrator utilizing reprogrammable FPGAs as core data processing unit.
  - Allow for a range of data processing algorithms to be implemented to cover a wide range of applications.
  - Fault tolerant design
  - In-flight reconfigurable core of FPGAs
  - Focus on the SW Development Environment kit to exploit the unit’s capabilities.
  - Run Performance Benchmarks based on CCSDS Image compression standards

- **Activity Started Q1 09; 2 ongoing contracts.**
- **Duration 24 Months**
**Reconfigurability: GMDR (II)**

- FPGA Based Generic Module and Dynamic Reconfigurator:

- General instrument I/F
- System Controller
- Avionics Bus I/F
  - * SpW (RMAP)
  - * MIL-STD-1553
  - * GPIO

- Cluster of Reprogrammable FPGA’s
- Configuration Memory
- CAN I/F towards low data rate instruments
- SpW I/F towards payload

Legend:
- Transducer
- SpW Interface
- CAN bus
- MIL-Std-1553 bus
- Discrete I/O
- Reconfigurable Core
Reconfigurability: GMDR (III)

- **2 Contracts:**
  - TwT and University of Paderborn
    - Architecture based on the Raptor X64
    - Dynamic Reconfiguration follows a layered approach
    - Politecnico di Torino will join the team for the hardening aspects
      (STAR/RoRA/VPLACE in reconfigurable solutions)
  - Astrium UK and IDA Braunschweig
    - Architecture based on SpW router and NoC approach using SOCWire inside the FPGAs
    - SystemC models for platform cosimulation

- **Current status:**
  - PDR for both contracts
Networking/Partnering Initiative (NPI)

- General NPI info: [http://www.esa.int/esaMI/Technology/SEM4KVWPXPF_0.html](http://www.esa.int/esaMI/Technology/SEM4KVWPXPF_0.html)
- NPI Contract between ESA and Politecnico di Milano - 1 Jan 2009 to 31 Dec 2011
- PhD Candidate: Chiara Sandionigi
- Advisor: Prof. Cristiana Bolchini/ ESA T.O.: David Merodio Codinachs, Luca Fossati

Objective

- Define a methodology to design a reliable embedded system on a multi-FPGA platform, exploiting the devices reconfiguration capabilities to manage the occurrence of hardware faults

Issues

- Apply fault detection and mitigation techniques on the system
- Distribute the reliable system on the multi-FPGA platform
- Define an overall fault mitigation strategy
- Design a reliable reconfiguration controller and the related protocol
Reliability-aware design methodology for embedded systems on multi-FPGA platforms

Hybrid approach based onto passive redundancy and active fault mitigation

Passive redundancy
- Application of spatial redundancy techniques
- Fault detection: Duplication With Comparison
- Fault tolerance: Triple Modular Redundancy

Active fault mitigation
- Reconfiguration based on the fault type
- Transient fault (soft errors): configuration rewriting
- Permanent fault (aging): functionality relocation
- Replicated Reconfiguration Controller solution
Conclusions

- **ESA involved in the development of European FPGAs**

- **ESA involved in SEE-related activities**
  - Static tools for FPGA radiation hardness assessment
    - SST, STAR, RoRA, VPLACE, INFAULT, SUSANNA/JONATHAN
  - Dynamic tools for FPGA radiation hardness: Fault Injection
    - FT-UNSHADES/2, FLIPPER
  - Radiation testing

- **ESA involved in Quality-related activities**
  - PPBI

- **ESA involved in Application Reconfigurability-related activities**
  - Reconfigurable Regenerative Processor (Software Defined Radio)
  - DRPM
  - NPI
Thank you

Questions?
Mitigation of SEU in User Logic

- **Standard synchronous RTL design**

- **TMR and single voters for flip-flops** for hard-wired logic (ASIC)

- **Functional TMR (FTMR)** [4] for SRAM (reprogrammable) FPGA
Selection of a Mitigation Strategy

- **SEE mitigation has area and performance overhead**
- **Trade-off between cost and fault tolerance**
  - Same hardening scheme for the complete design is easiest to implement
  - Selective hardening of critical parts is often the only acceptable solution
  - Life time requirement of applications can be very different

<table>
<thead>
<tr>
<th>Data Criticality</th>
<th>Low</th>
<th>High</th>
</tr>
</thead>
<tbody>
<tr>
<td>Error Persistence</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Operating Window</th>
<th>Low Mitigation</th>
<th>Scrubbing</th>
<th>XTMR</th>
<th>Redundant devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minutes</td>
<td>No Mitigation</td>
<td>Scrubbing XTMR</td>
<td>XTMR</td>
<td>Redundant devices</td>
</tr>
<tr>
<td>Days</td>
<td>Scrubbing</td>
<td>XTMR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Months</td>
<td>Scrubbing</td>
<td>XTMR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous</td>
<td>Scrubbing</td>
<td>XTMR</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>