

Microelectronics Presentation Days  
March 2010

AT697F & SpaceWire RTC for Space



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for Guy Mantelet

**Atmel ASIC BU  
Aerospace Product Line**

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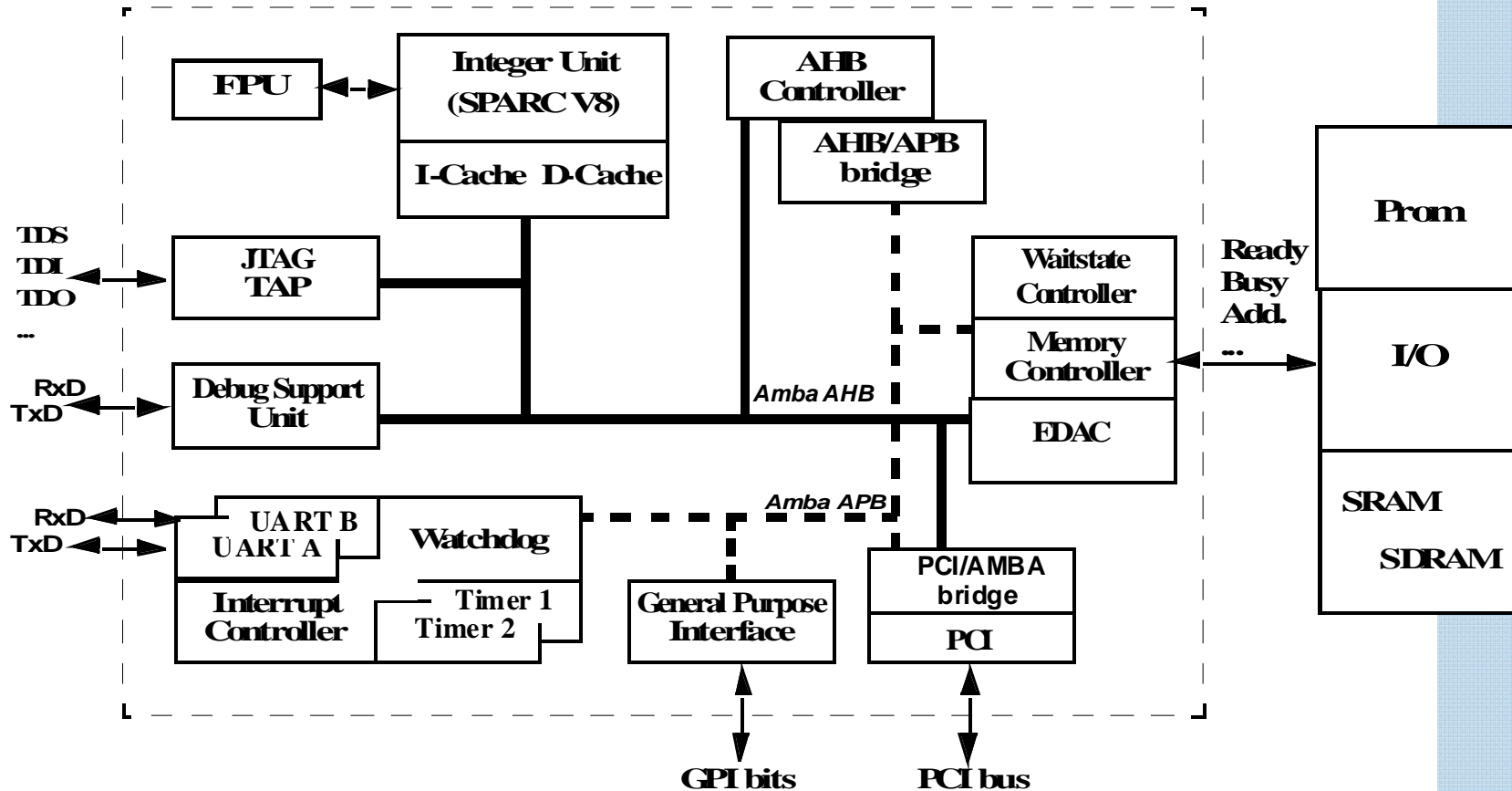
### AT697 Sparc V8 32-bit Architecture

- **SPARC V8 LEON2-FT with Integer and Floating Point Unit**
- **On chip Amba Bus**
- **Embedded Instruction and Data caches**
  - **16Kbytes multi-sets Data cache**
  - **32Kbytes multi-sets Instruction Cache**
- **Memories Interface for PROM, SRAM and SDRAM**
- **PCI 2.2 interface (33 MHz)**
- **Two Timers, two 8-bit Uarts and interrupt Controller**
- **User friendly Debug Support Unit**
  - **Trace buffer 512 lines of 16 bytes**

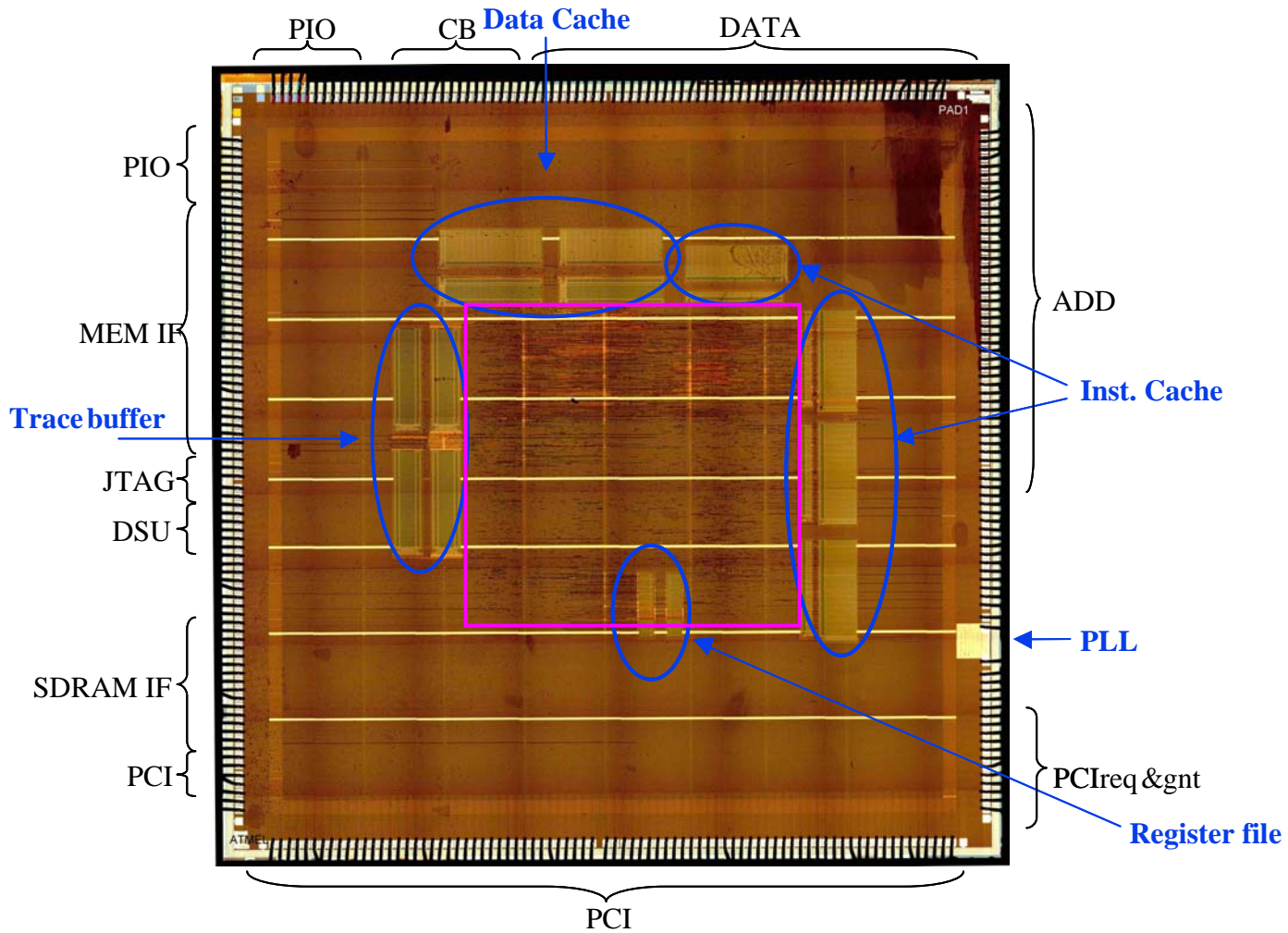
### AT697 basics

- **ATC18RHA CMOS 0.18 micron; 1.8 V core; 3.3V I/Os**
- **Fault tolerance by design**
  - **Triple Modular Redundancy with skew**
    - SEU and SET protection
  - **EDAC on register file and external memories**
  - **Parity on the caches**
- **Available package**
  - **MCGA 349 last delivery Q2\_2011**
  - **LGA 349**
  - **MQFPF 256**

## AT697 block diagram



## AT697 Die View





## AT697E performance

### ■ Performance at 100MHz

- 86 MIPS (Dhrystone 2.1)
- 23 MFLOPs (Whetstone)
- SDRAM interface speed impacted by the bus load
  - On AT697-EVAB (2 SRAM and 1 SDRAM banks) : 65 MHz maximum

### ■ Power consumption

- 7 mW / MHz
- At 100 MHz and for high activity : core at 0.5 W, I/O at 0.2 W

**150 MIPS/W**



# AT697E radiation performance

## ■ Total Ionizing Dose

- Parts fully functional at 200 krad (Si)
- 3.3V I/O standby current increases after 100 krad (Si), and recovers after high temperature annealing
- These results allow to use these AT697E parts for space mission requiring a maximum of 60 krad (Si)

## ■ Single Event Effects

- No Single Event Latchup (SEL) at 95 MeV/mg/cm<sup>2</sup> – max voltage – 125°C for a fluence of 1 E7 particles/cm<sup>2</sup>
- Very good Single Event Upset/Transient (SEU/SET) protection

### AT697F rationales

- **Prototype devices: AT697E and Flight devices: AT697F**
- **ATC18RHA library**
  - To allow successful total dose test up to 300 krad (Si)
  - To ensure appropriate process reliability monitoring (through SEC test vehicle)
- **Bug removal**
  - All known bugs has been corrected (see AT697E errata sheet)
- **Removal of existing functions**
  - 16-bit mode PROM/RAM interface (no EDAC support)
  - PCI single transaction mode
- **Addition of new functions**
  - Addition of Two Memory Block Protection Units (TSC695F compatible)
- **Pin out compatible with AT697E**



### AT697F improvements

- **Feedbacks from customers during AT697E validation**
- **Improvements**
  - **Asynchronous assertion of BRDYN**
  - **Use of the BRDYN for PROM area**
  - **Extending the timers to 32-bits**
  - **Addition of four external interrupts**
  - **AHB trace buffer halt**
  - **New 8-bit memory EDAC scheme**
  - **Write to 8-bit PROM with EDAC enabled**
  - **PCI device configuration boot pin made readable**
  - **PCI configuration registers made AHB readable in satellite mode**
  - **Higher capacitive load capability.**
  - **Higher ESD protection 2000V (250V for AT697E)**
  - **Total dose : tested up to 300Krad(si) successfully**
- **SDRAM interface speed up to 90MHz**

## AT697F status

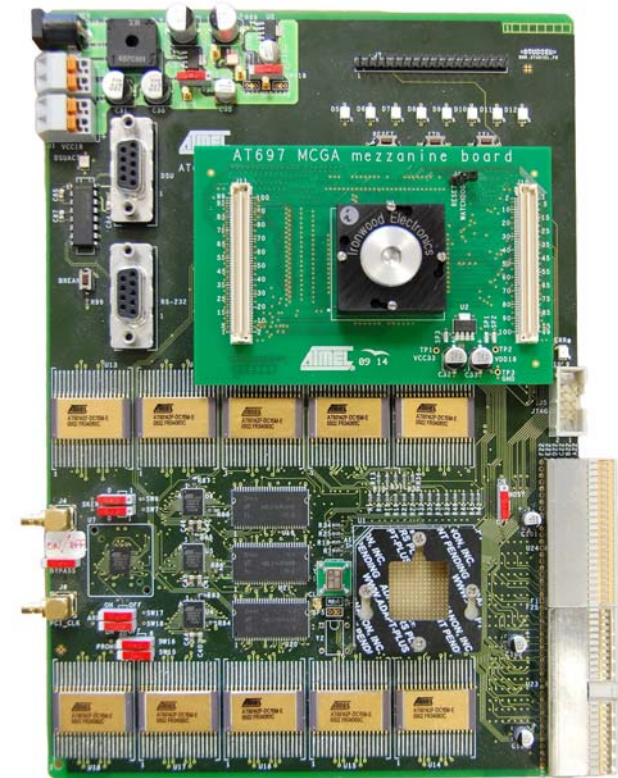
- **Preliminary Datasheet available. Final June 2010**
- **ESCC evaluation started. Final report end Q3/2010**
- **Order entry opened**
  - **Engineering Models already shipping**
  - **Availability**
    - SMD number: variant      **5962-072240**
    - EM      **order+6w**
    - QML-Q      **order+12w**
    - QML-V      **order +24w**
- **Radiation characterisation**
  - **TID report done**
  - **Heavy ions: July 2010**





# ATMEL AT697 Compact PCI Evaluation board

- Compact PCI plug-in format
  - 6U format, 32 bit, 33MHz interface
  - Configurable for System and Peripheral slot operation
  - Two mezzanine board MCGA & MQFPF
- Processor
  - Atmel AT697E/F , Rad-Hard 32 bit Sparc V8 Embedded Processor
- On-board memory
  - SRAM - 4Mbyte
    - 2 AT60142 SRAM banks
  - FLASH - 2Mbyte
  - SDRAM - 64Mbyte
- Interfaces
  - Memory/Peripheral expansion connectors
  - Debug Support Unit interface
  - PIO expansion
  - On-board power regulation allows operation from PCI slot, or stand-alone with +5V supply.



## Lesson learnt

### ■ Design

- **TMR**
  - No automatic design tools, manual script
- **Skew**
  - Triple skewed Clock
  - Tools must be squeezed!
  - 10% increase in power consumption (and area)
- **Reset**
  - AT697F keeps Flip-Flop data under reset
  - Simulation at gate level did not converge

### ■ Test

- **TDF**
  - Accurate measurement of set-up and hold with tester loads
  - Simulation with tester loads done successfully

### ■ See also DAC 2009 presentation by R.Weigand

### AT7913E Sparc V8

- Sparc V8 Leon2 FT with Floating Point Unit
- AT7913E RTC (Remote Terminal Controller)
  - Two CAN interface
  - FIFO interface (parity check)
  - ADC/DAC interface
  - 2 UART interfaces
  - 2 bidirectional SPW link 200Mbit/s on chip LVDS
  - 64kB x 32 on chip memory with EDAC
  - ...
- CMOS Technology: ATC18RHA (0,18  $\mu\text{m}$ )
- LGA 349
- MQFPF 352 feasibility on going
- Power consumption: ~0.7W@50MHz
- 1.8V core, 3.3V I/O

# AT7913E Sparc V8 Status

- **SMD spec and Datasheet available**
- **User's Manual for June**
- **Order entry opened, first samples delivered**
- **Availabilty**
  - **EM**                      **end May 2010**
  - **QML-Q**                **order + 12w**
  - **QML-V**                **order + 24w**
- **Evaluation Kit in development at AURELIA/CAEN and STAR DUNDEE**
- **Contract “almost” closed with RUAG**
- **Support set-up with cooperation of RUAG**



Questions?

Thank You