DARE180 Maintenance & DARE90 Development

Microelectronics Presentation Days
30 March 2010
ESA/ESTEC Noordwijk – NL

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Outline

- **WP1: DARE180 Library maintenance**

  \+ CCN: DARE180 CIS Port

- WP2.1: DARE90 Test vehicle design
- WP2.2: DARE90 Test vehicle manufacturing
- WP2.3: DARE90 Test structure characterization and irradiation
- WP2.4: DARE90 Test results analysis and library definition

DARE180 Library Maintenance

- Objective:
  - Provide a ready-to-use DARE180 library including all the views for the complete design flow
  - Provide the necessary documentation including a data book
- Tasks:
  - Script data book generation
  - Check consistency of the library
  - Simulate failing SRAMs of DIE_HARD test chip

DARE180 – Virtuoso Database

- Schematic Update:
  - CORE, IO, IOa, PLL, LVDS, (SRAM)
  - Conversion script from old to new database for schematics and symbols
- Layout Update:
  - Conversion script based on GDSII layer remapping
  - PG tracks set to 1um
  - top metal 20kA
  - SAB layer (DRC)
  - MMSYMBOL layer added (LVS)
  - new bondpad (oxide studs)
  - minimum area rules (DRC)
  - ...
- New names: DARE180_* (previously RadHardUMC18_*)
  - DARE180_CORE, DARE180_IO, ..

DARE180 – Database Verification

- DRC:
  - Automated verification scripts for complete library
- LVS:
  - Include extraction for ELT
  - Automated verification scripts for complete library
- LPE:
  - Based on LVS verification scripts
  - Extraction of parasitic capacitors and resistors
  - Reduction of complex RC circuits

DARE180 – Characterization

- SignalStorm -> ELC
  - CORE and IO
  - Fully scripted approach
  - HIT cells are included in the flow
  - Automated generation of databook (html)
  - Verilog, Vital, lib/db
- Ocean (spectre)
  - LVDS and PLL
  - A lot of scripting to generate the views
  - Verilog, Vital, lib/db, html

DARE180 – SRAM Generator

- C++ code
  - Unix -> Linux
  - Minor changes
- Simulation
  - To solve problem in medium and big size SRAMs
  - High capacity spice simulator used (Ultrasim)
  - Based on schematic -> all OK
  - Based on layout with parasitic C extraction -> all OK
  - Based on layout with full RC networks -> timing problem in medium sized and big SRAMs

    - Good news: We know the problem...and also how to fix it!
    - Bad news: The solution is yet to be implemented!

DARE180 – Library Additions

- Analog IO pads for enabling a mixed-signal design flow
  - 2 possible analog domains: 1.8V, 3.3V
  - a specific breaker cell was included
- Specific views for enabling a Cadence SoC Encounter P&R flow
  - LEF files, abstract views, etc.
  - These were extensively debugged in an external design.

Beyond DARE180 …

- The DARE180 IO libraries are compatible with the Logic and the MM-RF processing options (thick top metal)
- Large Bond Pad IO library
  - 110 x 110 um2 (standard IO = 70 x 70 um2)
  - Available for IO, IOa, LVDS and PLL
- Cmos Imaging Sensor Technology
  - Reduced metal stack (4M)
  - Only LBP version available for IO cells
  - Fully characterized with CIS transistor models
  - ‘Not just another port’
    - ESD (multiple power domains, big die, limited metal layers)
    - Additional functionality for LVDS: PD input
    - 4 additional HIT cells with M1 reprogrammable Set/Reset
  - PLL not ported

DARE180, DARE180_LBP and DARE180_CIS Libraries

IO at 3.3 and 2.5 V

		Logic/MM-RF	CIS
Core 1.8V	combinatorial	50	50
	normal' FF's	20	20
	HIT FF's	20	20
	HIT FF with M1 progr. Reset	no	4
	TIEx	2	2
IO	Digital IO 70x70	40	no
	Digital IO 110x110	40	40
IO	Analog IO 70x70	5	no
	Analog IO 110x110	5	6
IO	LVDS 70x70	3	no
	LVDS 110x110	3	3
IO	PLL 70x70	1	no
	PLL 110x110	1	no
SRAM Compiler (6Tor cell)		yes	no

All FF's have scan equivalents

+ fillers, corners, extra ESD

In a nutshell…

- The DARE180 library supports design of ASICS for spacecraft
  - Uses commercially available technology without tweaking the process
  - Using the library is free of charge for European space industry
  - Customer can do front-end design (to netlist)
- Physical implementation services provided by imec
- Manufacturing, Packaging, Quality screening & Radiation test up to FM is supported

- Flexible solution
  - DARE180 allows for mixed signal designs
    - Analog IO
    - Can add specific analog blocks: designed by you, a design house or imec
  - Cells can be added to the library

The DARE180 standard cell library family

- Developed in several ESA projects
- DARE = Design Against Radiation Effects (=RHbD)
- Commercial Technology: UMC L180 CMOS

- TID hardness is far beyond requirement level for geostationary orbit
    - Tested to 1 MRad
- No SEL, SEFI, SEH seen so far
- Low SEU sensitivity, compatible with geostationary orbit mission
    - 'normal' flip-flops & RAMs
    - HIT-based flip-flops are very insensitive to SEU

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DARE180 vs a commercial .18 library

- Maximum gate density = 25Kgates/mm2
- DARE180 cells are 2 - 4 times bigger than cells with same functionality from a commercial library
- DARE180 vs commercial cell power = 2.2x
  - Total power = Internal & Switching power
- No speed penalty
- Views available for a classical ASIC design flow
  - Using the HIT flip-flops no triplication is necessary

- Designs with a lot of RAM become very big
- SEU Hardening of RAM using EDAC circuit

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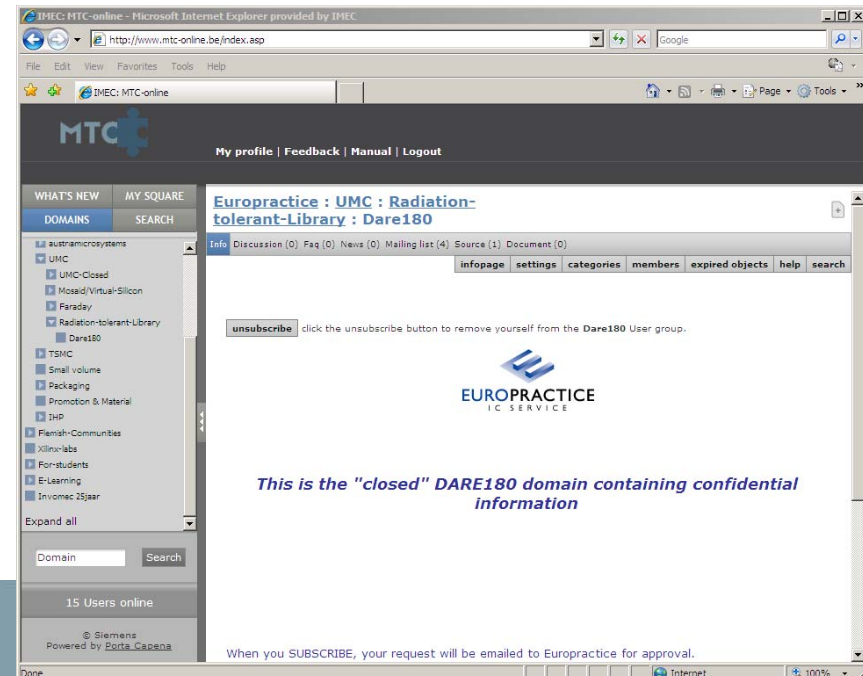
How to get access

- Get in touch with Steven.Redant@imec.be
  - By mail, or by asking access to the library files on the web
- Sign NDA (per project)
- Get access to the download area on the web
  - www.europractice-online -> UMC -> Radiation-Tolerant-Library
- Download the (Front End) views
  - Synthesis & Simulation



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DARE90 – layout for TID hardness

- TID hardness requires circular gates (ELT shapes) for NMOS devices

- UMC's 90nm Design Rule Manual forbids the use of polysilicon corners on diffusion
  - 90 degrees nor 45 degrees
  - In DARE180 45-degree corners were still allowed

- We sent a test structure (with 36 ELT devices – NMOS and PMOS) to UMC for investigation
  - **Good news**: UMC gave clearance to process this type of layout, "at our own risk"

DARE90 – which device flavor to choose? (1)

	$t_{OX,inv}$ (nm)	$\lvert V_{T,sat} \rvert$ (mV)	$\lvert I_{ON} \rvert$ (uA/um)	$\lvert I_{OFF} \rvert$ (nA/um)
NMOS				
SP – low V_T – 1.0V / 1.2V	2.25	155 / 137	760 / 993	80 / 100
SP – reg. V_T – 1.0V / 1.2V		240 / 227	655 / 907	5.0 / 5.0
SP – high V_T – 1.0V / 1.2V		370 / 362	480 / 710	0.3 / 0.4
LL – low V_T – 1.2V	2.95	386	546	0.2
LL – reg. V_T – 1.2V		453	480	0.03
LL – high V_T – 1.2V		540	385	0.006
PMOS				
SP – low V_T – 1.0V / 1.2V	2.45	105 / 90	320 / 448	80 / 110
SP – reg. V_T – 1.0V / 1.2V		177 / 167	280 / 394	10 / 12
SP – high V_T – 1.0V / 1.2V		300 / 287	195 / 297	0.4 / 0.6
LL – low V_T – 1.2V	3.10	287	250	0.8
LL – reg. V_T – 1.2V		409	185	0.03
LL – high V_T – 1.2V		455	155	0.01

DARE90 – which device flavor to choose? (2)

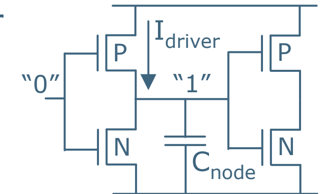
- What are we aiming for?
  - first of all: functional circuits!
  - then: low power, high speed, minimal area, low leakage,…?
- Low leakage (LL option) may be desirable for space applications
  - I_{OFF} (= subthreshold leakage) is reduced by 2 orders of magnitude w.r.t. SP…
    - … but drivestrength (speed) is also reduced
  - LL devices run at 1.2V operating voltage only

DARE90 – which device flavor to choose? (3)

- Is there an impact on SET sensitivity? We don't know yet.

assumption: sensitivity ~ $1/(I_{driver}*C_{node})$ = FOM

- C_{node} can be interpreted as the C_{OX} per unit area ($=C'_{OX}$) seen by the driver
- I_{driver} is the I_{DS} of the device keeping the node at its logic level



example for PMOS driver:

What happens to SET sensitivity when replacing all SP devices by equally sized LL devices?

$t_{OX}*1.26 \rightarrow C'_{OX}/1.26$; $I_{driver}/1.93$ → $FOM_{LL} = 2.43*FOM_{SP}$

conclusions:

- LL is more SET-sensitive than SP when the device area is unchanged. Speed decreases.
- Restoring the speed by increasing the PMOS W/L increases the area.
- Maintaining the PMOS W/L and keeping it SP yields a better FOM: $FOM_{LL} = 1.26*FOM_{SP}$ (but PMOS I_{OFF} detereorates)
- The case of an NMOS-ELT driver is always much better because of its higher drivestrength: $FOM_{Ndriver} \approx FOM_{Pdriver}/9$ (see next slide)

- What about the V_T option?
  - I_{OFF} ~ $1/V_T$: higher V_T means lower leakage current
  - speed ~ $1/V_T$: higher V_T means lower drivestrength

DARE90 – NMOS/PMOS drivestrength balancing (1)

- Nowadays commercial library vendors do not apply this for regular DSM standard cells
  - Goal = minimal area
  - Balanced buffers/inverters are provided separately for clock trees

- But: minimal NMOS ELT shapes have a significantly higher W/L ratio compared to minimal 'rectangular' transistors
  - *geometrically*: $W_{ELT,min} \approx$ **9**$*W_{rect,min}$!!
  - *electrically*: difference in carrier mobility ($\mu_N/\mu_P \approx$ **3**) !
  - In total there's a serious drivestrength disproportion between NMOS-ELT and a minimal rectangular PMOS

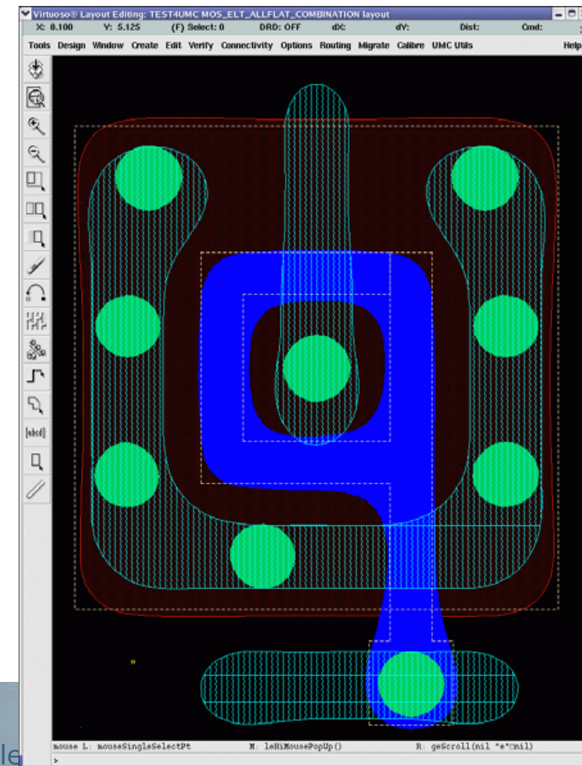
DARE90 – NMOS/PMOS drivestrength balancing (2)

- Several scenarios:
  1. Live with it: make minimal rectangular PMOS devices
     - Good for cell area
     - Bad for cell delay & short-circuit power
  2. Construct PMOS devices as minimal ELT shapes
     - Drivestrength mismatch is now limited to the inherent difference in carrier mobility ($\mu_N/\mu_P \approx 3$)
     - Larger cell area
     - Smaller cell delay, less short-circuit power
  3. Build multi-V_T cells? Or even mixed LL-SP?
  4. ESA/industry requirements?

- Choice depends on the aim
  - Low power, high speed, minimal area, low leakage,…?

DARE90 – device modeling

- BSIM4 (v4.3.0) is used in the 90nm PDK
  - unlike BSIM3 (v3) in DARE180
- an ELT aspect ratio model can be found in literature
  - Anelli, Giraldo (CERN), used in DARE180
  - How valid is this for 90nm?
- UMC provided us with another picture:
  - This is a LITHO-simulation on our test structure
  - Overall the processed gate length is larger than the drawn gate length (dotted line), especially in the corners
- We quantified this by adjusting the standard ELT model
  - this preliminary eqn. is only valid for the 36 samples of our test structure!

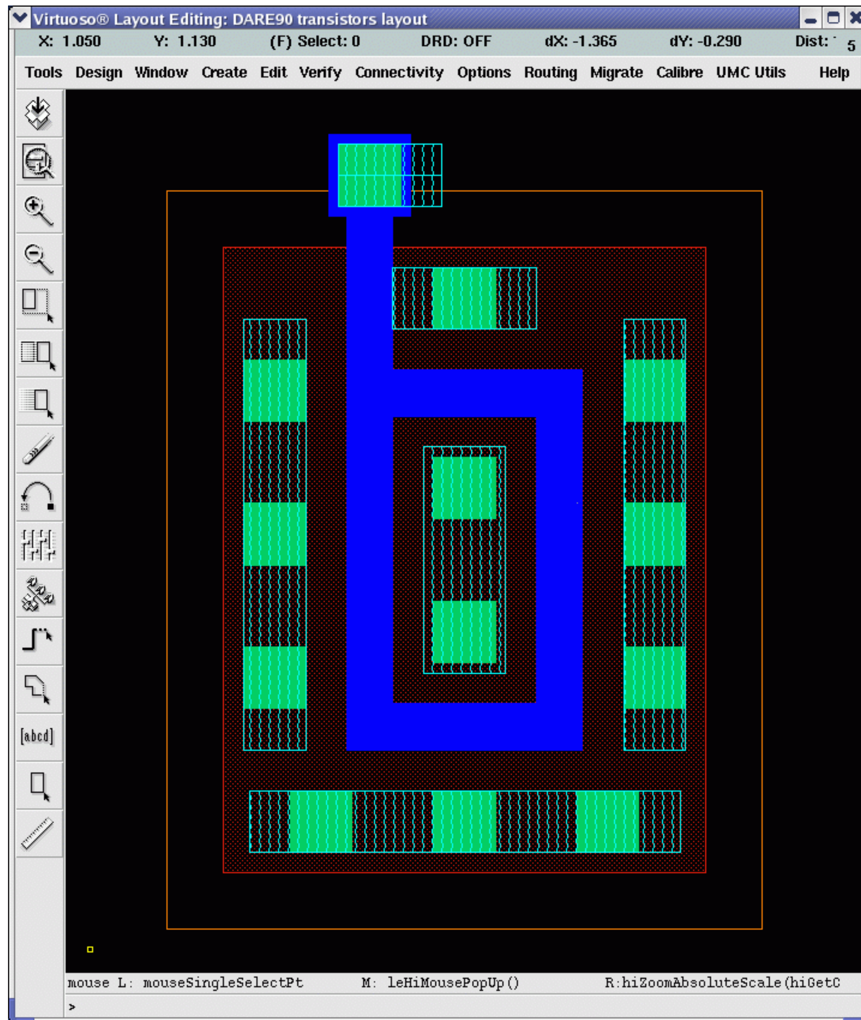


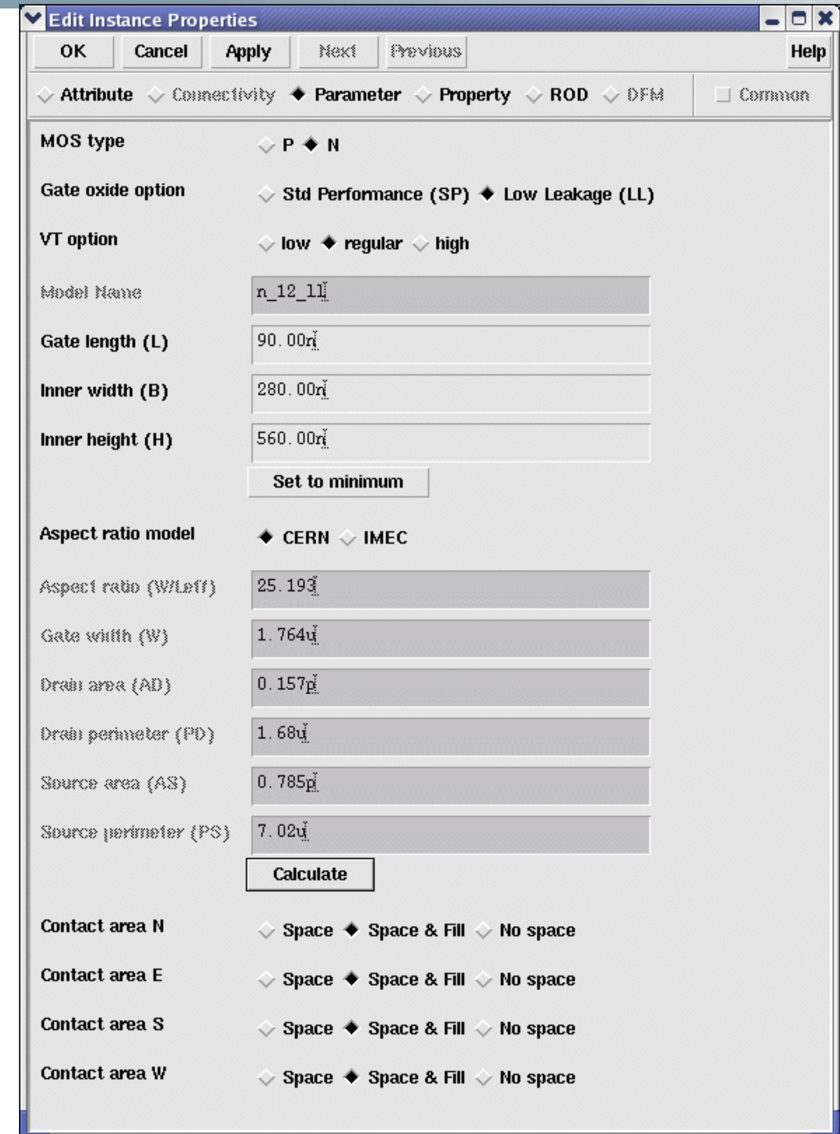
DARE90 – standard cells

- a “multi-flavor” ELT Pcell was developed – see next slide
  - adjustable parameters:
    - height (H), width (B) and gate length (L)
    - LL or SP marker layers
    - Low/regular/high V_T marker layers
  - Both aspect ratio models were integrated (CERN, IMEC)

- Based on previous decisions (device flavor, NMOS/PMOS compensation, etc.):
  - Initial simulations must still be run to define D1, D2, etc.
  - The most complex cell must be designed & laid out to come to the basic standard cell frame
    - reference = HIT cell

DARE90 – ELT Pcell





DARE90 – I/O ring - cells

Name	Kind
inpad	CMOS input
outpad	CMOS output
vddpad	Core Power
gndpad	Core Ground
v3iopad	I/O Power
v0iopad	I/O Ground
Corner	Corner cell
FILLER118_DARE	I/O Fillers(necessary because bondpad pitch exceeds width of an IO cell)

DARE90 – I/O ring - ESD

- 3.3V IO
- ESD rules for 90nm ≈ 180nm
- Minor changes expected
- ESD expert input
  - DARE180 ESD = portable for I/O cells with thick oxide
  - Gate length of GGPMOS and GGNMOS may go from 0.44 to 0.25 um.
- Implementation without ESD device directly between 1.2V and 3.3V

DARE90 - Combinatorial Core Cells for DIE_HARDER

Name	Kind
Combinatorial cells at 1V (limited core library cells)	
INVD1	Inverter, drive 1
NOR3	3-input NOR, drive1
NAND2	2-input NAND, drive 1
BUFD1	Buffer, drive 1
EXOR2	EXOR, drive 1
NOR2	2-input NOR, drive 1
BUFBD1	Balanced Buffer, drive 1
BUFBD4	Balanced Buffer, drive 4
Combinatorial cells at 3.3V (not part of core library)	
INVD0V3	Inverter, drive 0 using 3.3V transistors
NAND2V3	2-input NAND gate, drive 0 using 3.3V transistors
NOR2V3	2-input NOR gate, drive 0 using 3.3V transistors

DARE90- Memory Core cells for DIE_HARDER

Memory cells (limited core library cells)	
XDFF	HIT D-flip Flop, with Guard Bands, with Enclosed transistors
XDFF_NG	HIT D-flipflop, No Guard Bands, with Enclosed Transistors
XDFF_NE	HIT D-flipflop, with Guard Bands, no Enclosed Transistors
XDFFC(=DFFX1)	Non-hardened D-flipflop
XDFFRL	HIT asynchronously resettable D-flipflop
XDFFSL	HIT asynchronously settable D-flipflop
XDFFSLRL	HIT asynchronously settable & resettable D-flipflop
XLATCHD1	HIT latch, Drive 1
XLATCHD2	HIT latch, Drive 2
XLATCHC(=DLAHX1)	Non-hardened latch

DARE90 – Teststructures

Structure	#Supply domains	TEST
Ring Oscillators 1.2V +3.3V	1	TID
ShiftReg Phys. Countermeasures	4	TID
SET data + clock + reset	1	SET/SEL
ShiftReg SEU	1	SEU/SEL
Functional Comb + Seq	1	Functional
Functional IO	2	Functional
Total	10	

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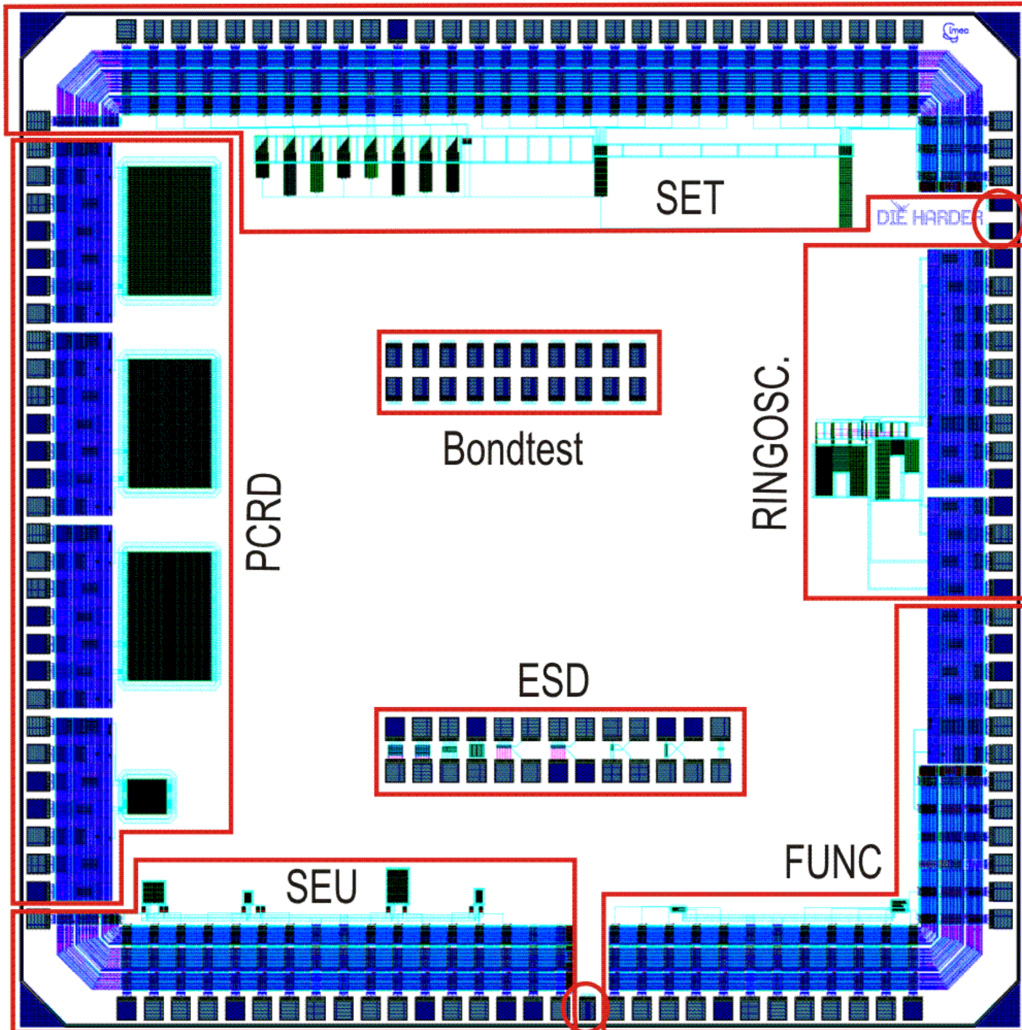
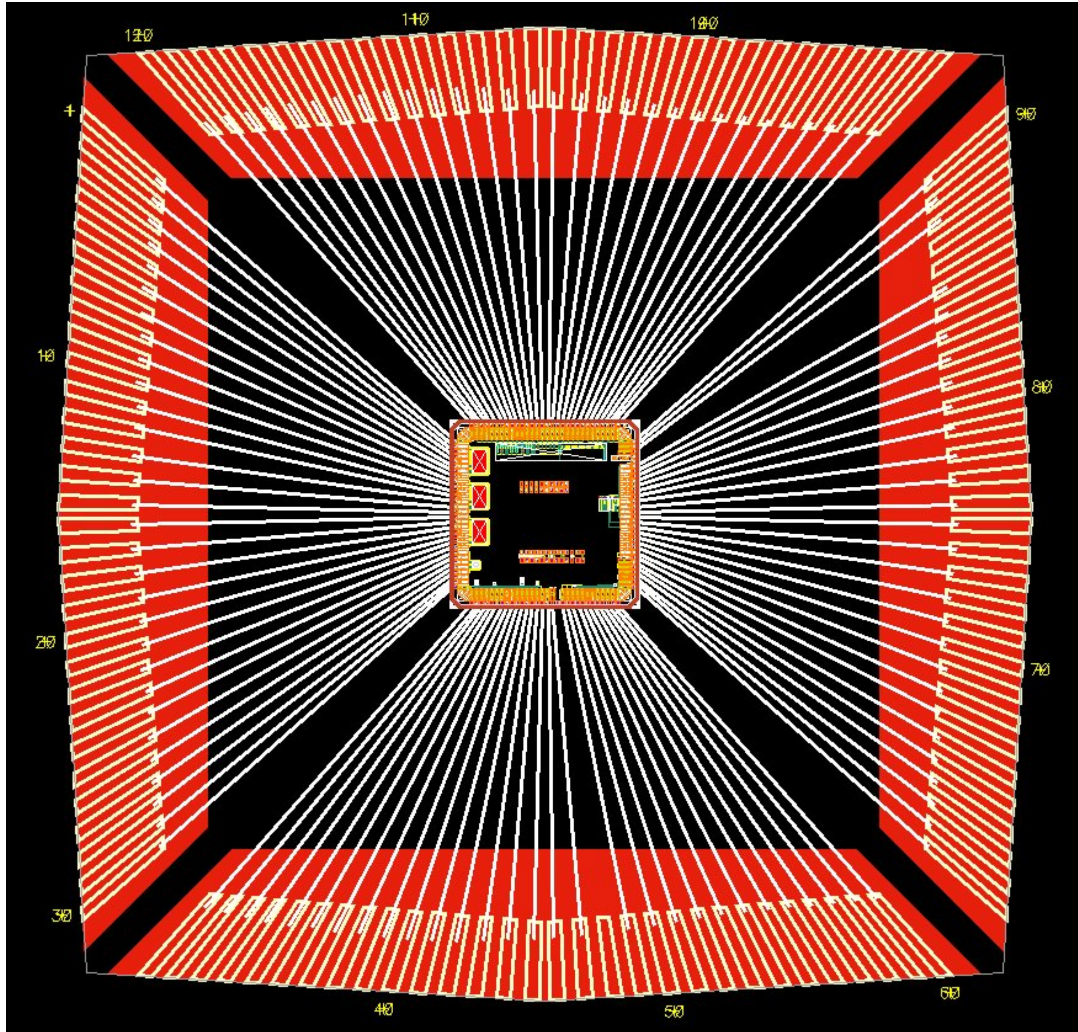
DARE90 – DIE_HARDER Floorplan



- Pad-limited design
- Total size of the chip: 3330 x3330 sq.µm
- 10 Supply domains
- I/O voltage: 3.3V
- Core voltage: 1.2V

DARE90 – Package – Bonding diagram



- Ceramic QFP120 Package

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DARE90 DIE_HARDER test setup

- Teradyne J750
- HATINA

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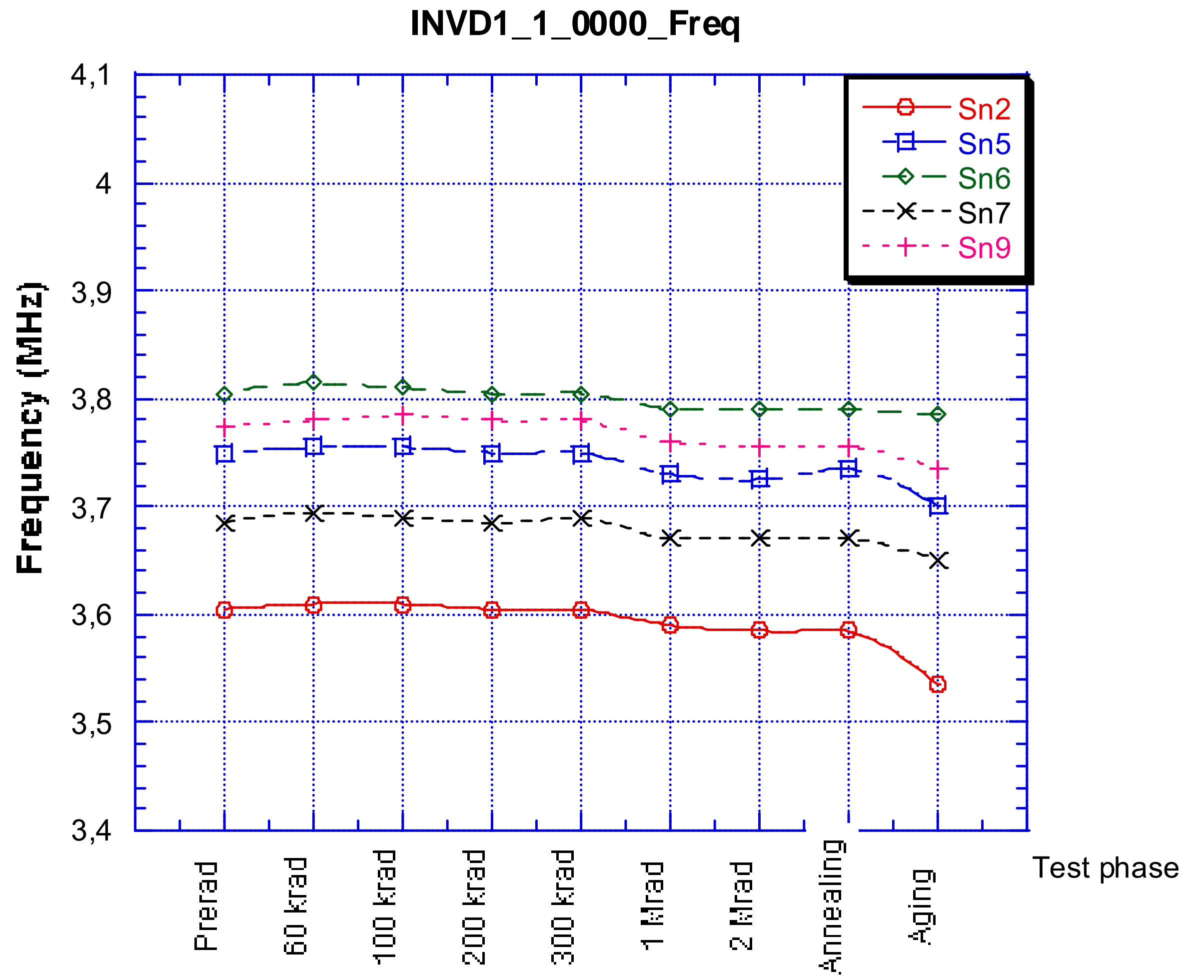
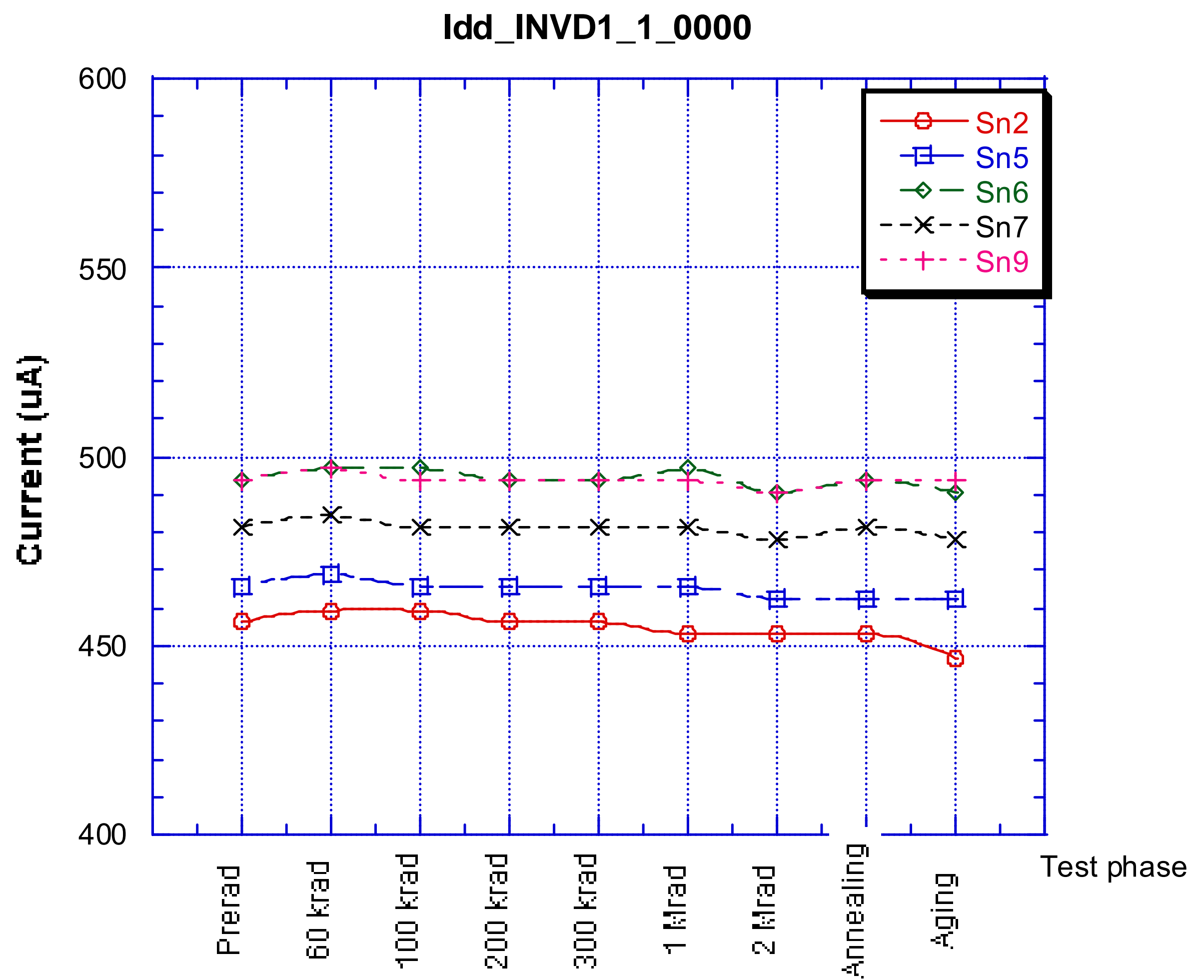
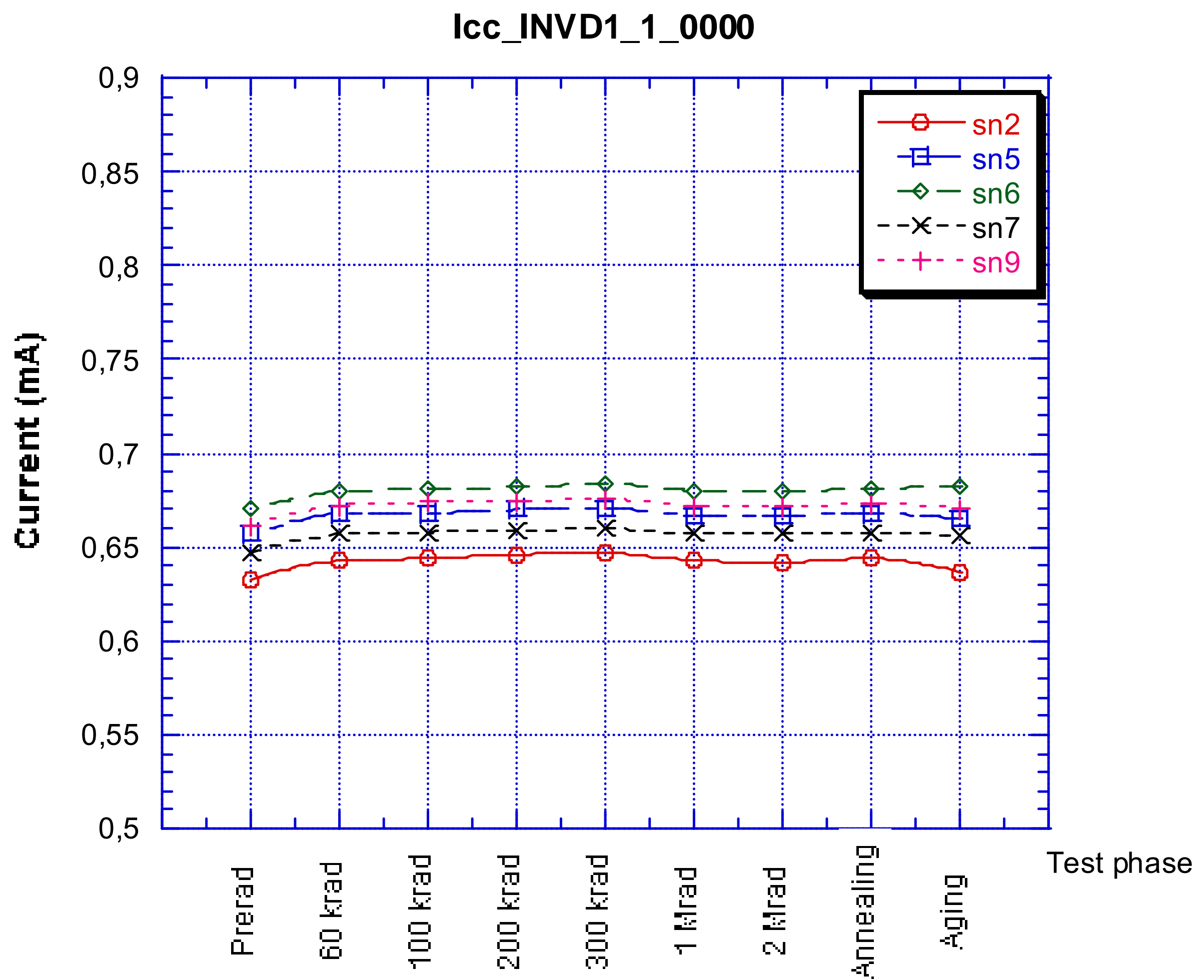
DARE90 Ring Oscillator TID: Frequency



DARE90 Ring Oscillator TID: Idd (1.2V)



DARE90 Ring Oscillator TID: Icc (3.3V)



Conclusions

- DARE180
  - The updated library is available as V4.1
  - The SRAM problem is identified and scheduled to be fixed
  - The library development is scripted from GDSII to LEF
- DARE180_CIS
  - Not a straight forward porting
  - Valuable feedback on our characterization flow
- DARE90
  - Analysis of irradiation tests (TID, SEU, SET, SEL)
  - Definition of complete library
  - Reuse of DARE180 scripting environment

Years of Making
Technology Fly