LEON3 Fault-Tolerant Design Against Radiation Effects - ESCC Evaluation

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Microelectronics Presentation Days 2010

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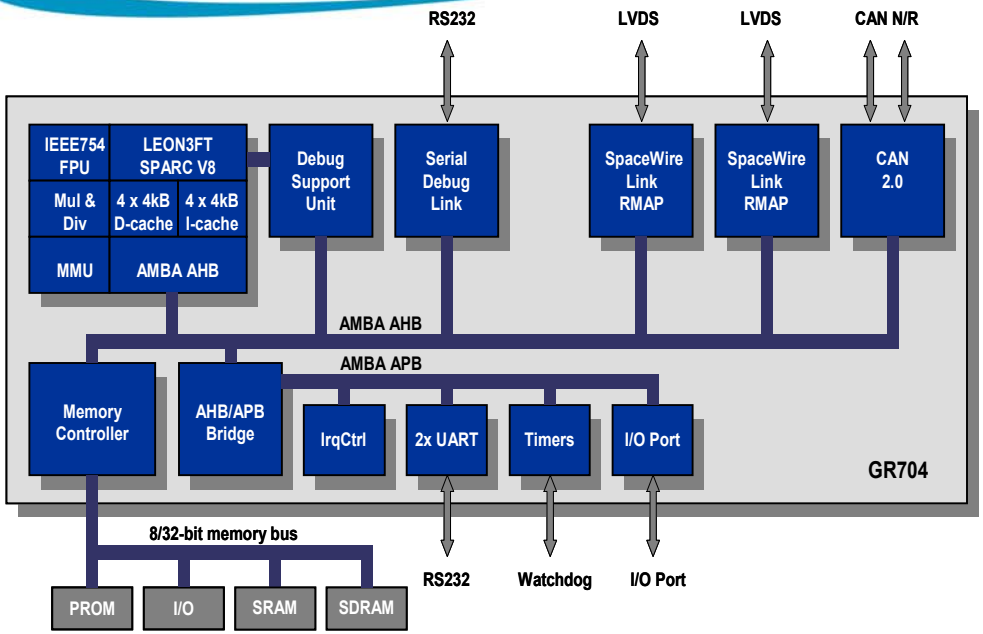
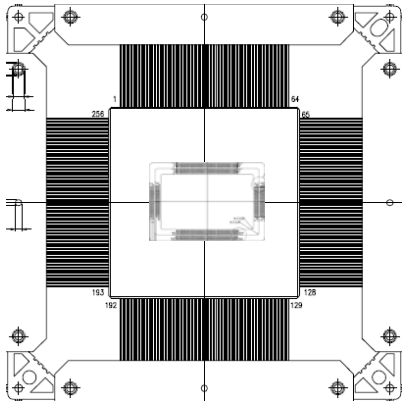
Project overview

- **Evaluation of the feasibility to develop and produce an ASIC having a proved capability for space use in a fabless approach, using a commercially available technology (UMC 0.18 µm CMOS), the Design Against Radiation Effects (DARE) library and a dedicated production and evaluation flow complying with the ESCC standards**
- **The 2 main outputs of the project will be :**
  - An evaluation plan summarizing the results of all the tests
  - An ASIC procurement & Qualification flow defining the tests to perform for guaranteeing highest space quality and reliability requirements for future DARE chips.
- **Design selected is the Aeroflex-Gaisler LEON3-FT**
- **Responsibilities:**
  - Thales Alenia Space ETCA (B) - Prime
    - Project management
    - Validation and evaluation testing
  - Aeroflex Gaisler (SE)
    - LEON3-FT processor design
  - IMEC (B)
    - Layout generation and DARE library
    - Interface with ASIC wafer fab via MPW EUROPRACTICE run



- LEON3-FT core with MMU & 2x16 KB caches
- 2 SPACEWIRE links + CAN-BUS interface
- Memory Controller with EDAC supporting SDRAM-PROM-SRAM memories
- 16 GPIO + UARTs
- Max core frequency : 120 Mhz
- Max SpaceWire rate : 250 MBPS
- Max power consumption : 3 W

- DARE library (1.8V / 3.3V) – UMC 0.18 CMOS technology
- Full Custom CQFP256 with tie bar. Leads pitch 0.5
- Die dimension : 10 x 5 mm
- 430k equivalent gates



- **Functional tests performed in application-representative conditions on GAISLER GR-PCI-XC2V LEON PCI development board**

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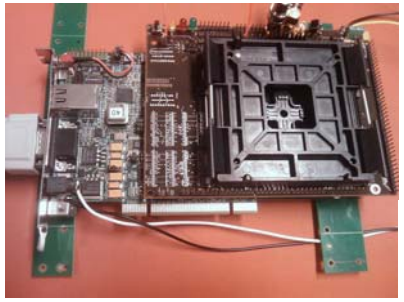
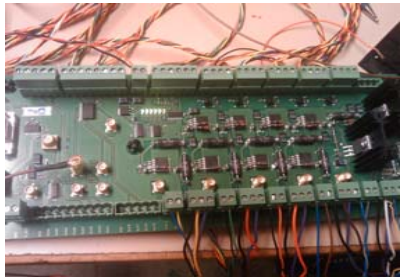
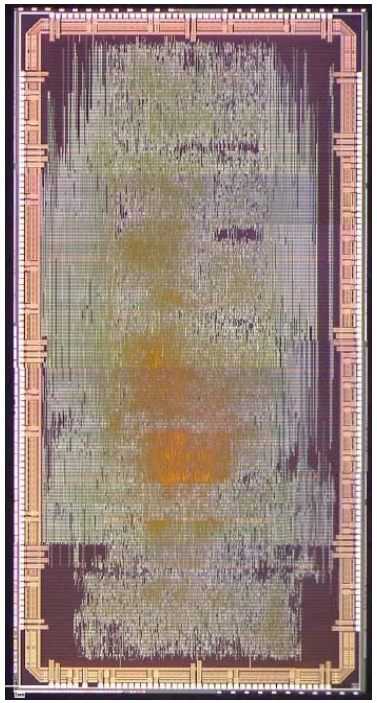


- **Schlumberger tester at test house facilities (SERMA) for production tests.**

- **Dedicated ETCA test boards for evaluation and validation tests**



- **Design / Layout / Manufacturing** √
- **ADR / PDR / CDR successful** √
- **Design validation**
  - Assembly & screening tests √
  - TID tests √
  - Heavy ions tests
- **Evaluation tests**
  - ESD HBM test √
  - Package construction analysis √
  - Functionality verification over varying parameters (T°, Voltage,…)
  - Mechanical & thermal package tests
  - Die construction analysis
  - Thermal & power step stress tests
  - Life-test > 2000h & burn-in
- **Project end : September 2010**



Results

Production yield

- **149 parts produced and packaged into CQFP 256**
  - 7 parts rejected during assembly after visual inspection
  - 4 parts used for package constructions analysis & assembly trial

- **138 parts electrically tested at 3 temperature (-55°C / +25°C / 125 °C)**
  - IO continuity tests.
  - Supply currents measurement (Iccsb, Iccop)
  - Static and dynamic parameters measurement (Vol/Voh/Vil/Vih,tplh,tphl)
  - Scan and functional tests
  - 124 passed the tests but after cache disabling (cache problem detected during electrical testing)
  - 14 failed the test

√ **Excellent production yield (Manufacturing + Assembly + Production tests)**

⇒ +/- 85%

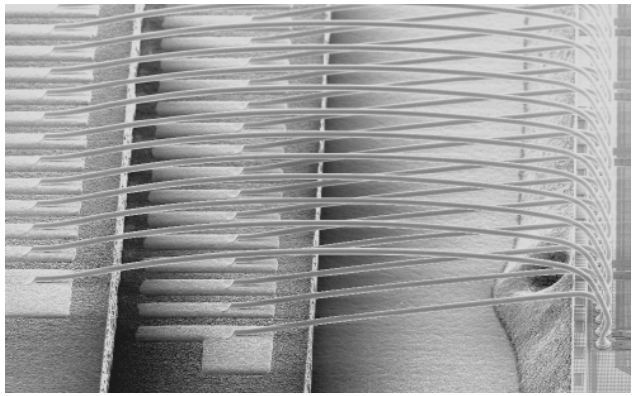
- **Risk on functionality of larger RAMs known at project start**
  - Large RAMs for caches on LEONDARE did not work correctly. Smaller ones did.
  - Simulations of full RAMs showed problem. Solution identified.
  - Problem will be corrected in upcoming compiler version.
  - Workaround by not enabling the caches by software

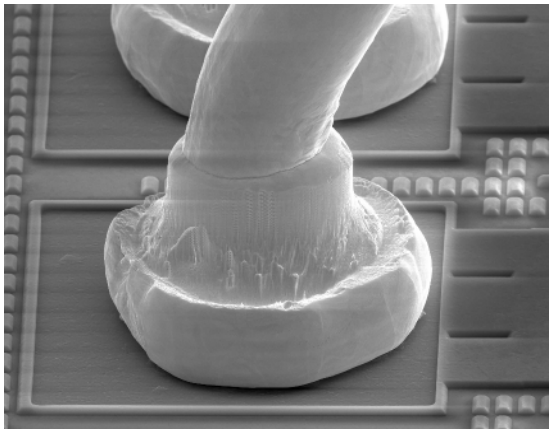
- **Power consumption estimate complied with measurements after LVDS buffer consumption was taken into account.**

Package construction analysis

- **Following ESCC2269000**

- **Performed on 3 parts, ball bonding 25 µm diameter gold wires.**

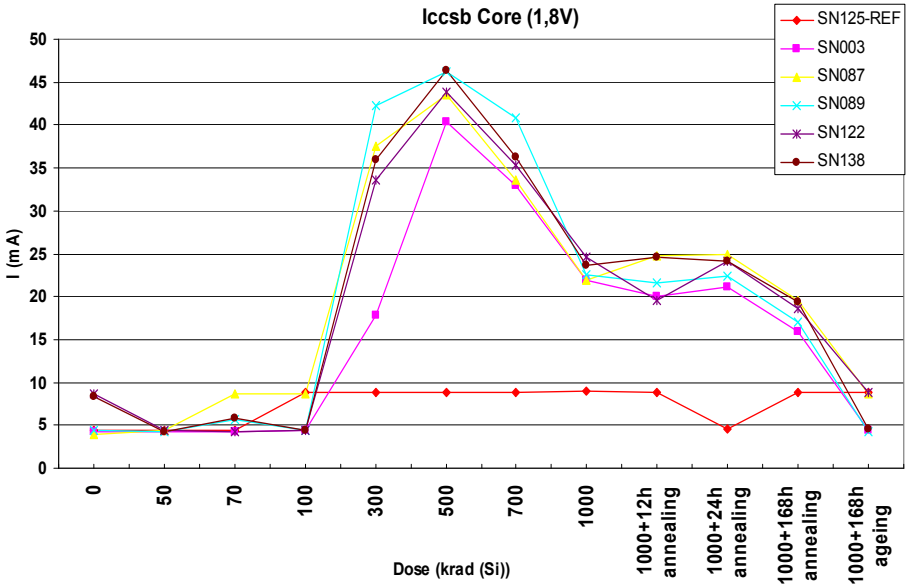


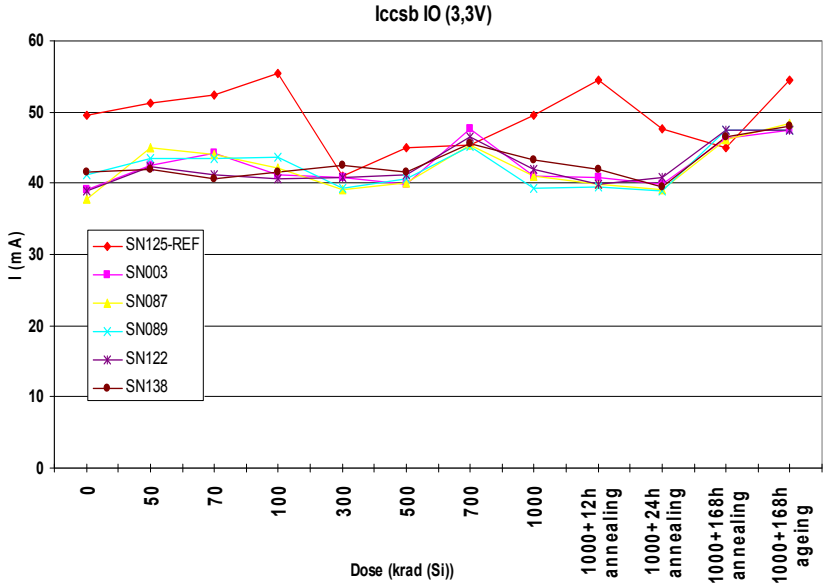


- **Results :**
  - No assembly defect was revealed
  - Internal connection were good
  - Wire pull & die shear test were correct

TID test (1/2)

- **Following ESCC22900**
- **Icc stand-by of the core :**
  - Stable until 100 krad(Si)
  - Increase until 500 krad (Si)
  - To decrease until 1 Mrad (Si)
  - Fully recovery & functional after accelerated ageing at 100 °C

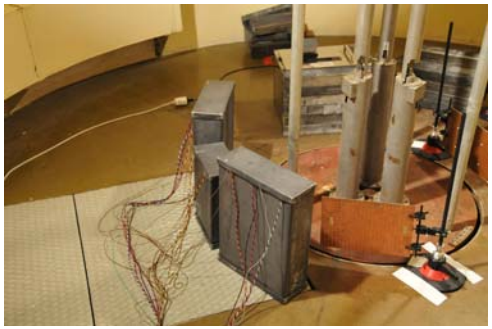


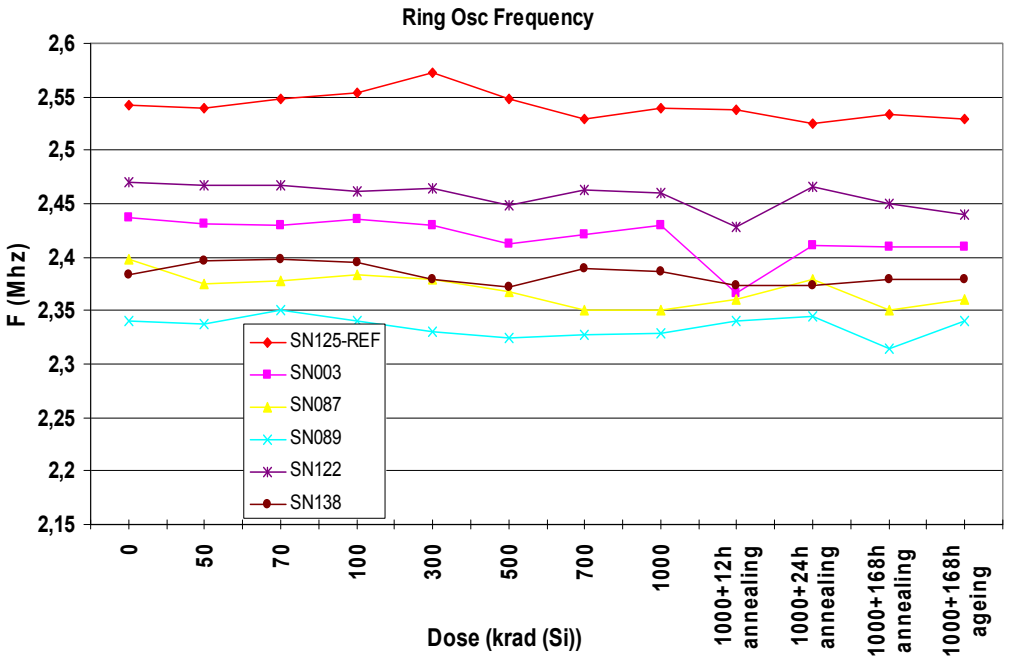


- **Icc stand-by of the IO :**
  - Dominated by the LVDS buffers consumptions
  - No significant evolution during the irradiation

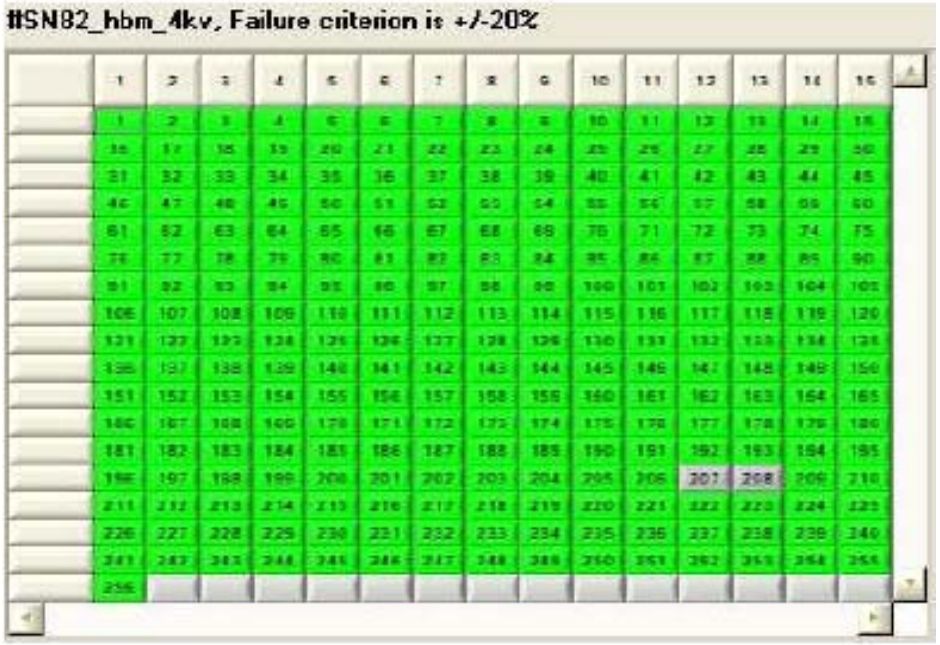
TID test (2/2)

- **Timing drift :**
  - Measure of an embedded ring oscillator
  - No significant variations during and after irradiation





- Following ESCC23800 (MIL-STD883H Method 3015)
- DARE IO ESD protection embedded
- Human Body Model passed at 1 KV 2KV & 4 KV
- Post electrical tests passed after 1 KV 2KV & 4 KV



Dev SN82: HBM Test Result at 4kV

⇒ **ESD Class 3A (>4kV) device !**

Pre-Results

- **Thermal step-stress test combined with a power step-stress test:**
  - First step at 150 °C and power max

- **First heavy ion test on December 2009:**
  - SEU hardening results seem good (LET th > 55Mev.mg/cm^2)
  - Connector problem during the test campaign invalid the results
  - New test in May 2010

Conclusion

- The first results shows that DARE library using the commercial UMC 0.18 technology keeps one's promises as expected.

- The LEONDARE project confirms the possibility to take advantage of commercial technologies for the design of rad-hard ASICs.

Thales Alenia Space in Belgium

www.thalesaleniaspace.com