Multi-DSP/Micro-Processor Architecture (MDPA)

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Content

- Motivation
- MDPA ASIC Features
- Blockdiagram
- Physical Layout
- ASIC status
- Application: Payload Controller using MDPA ASIC
- Application: Mass Memory Controller using MDPA ASIC
- Available Software Tools
- Outlook

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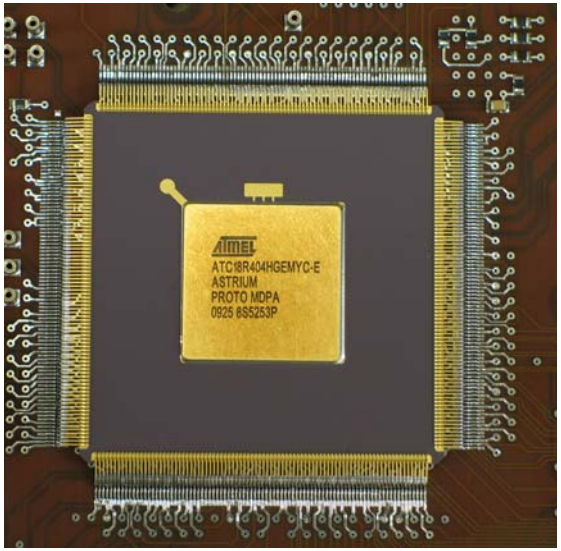
Motivation

- Implementation of a System-on-Chip (SOC) based on LEON2FT to serve upcoming Telecom and EO Missions
- General Requirements
  - High Control Processing Performance
  - Scalable to multiprocessor system via SpaceWire with routing capability
  - Spacecraft interface via Milbus or SpaceWire
  - Payload interface via MilBus, SpaceWire or CAN bus
- Specific Telecom Requirements
  - DVB-S regeneration function for high speed TM/TC interface with Network Control Center (600Kbps each direction)
  - Radiation hardened to operate 15 years in GEO orbit without uncorrectable error

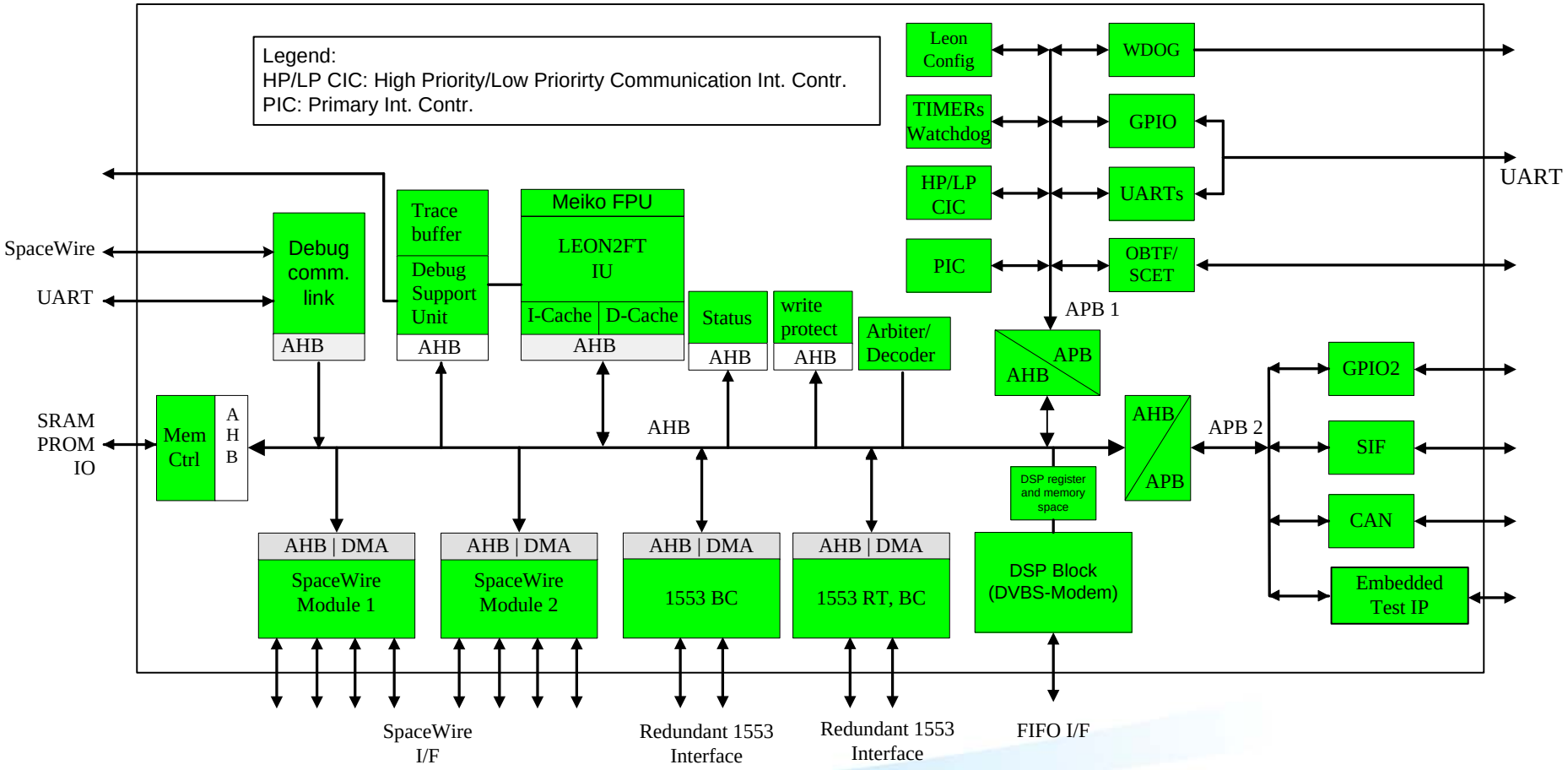
➔ MDPA (MultiDSP/microProcessor Architecture)

MultiDSP/µProcessor Architecture (MDPA) ASIC

- LEON2FT based System-on-Chip (SOC) operating at up to 80MHz; factor 5 of ERC32 performance (Hartstone benchmark)
- First SOC with SpaceWire router (path addressing) on-chip with 8 SpaceWire links operating at up to 200Mbps
- Further on-Chip features:
  - IEEE- 754 Floating Point Unit (Meiko)
  - 2 MilBus 1553 Controllers (Astrium SAS IP)
  - 1 CAN bus 2.0 Controller (ESA IP)
  - 2 UARTs
  - Modem based on DVB-S standard protocol (Astrium Ltd IP)
  - RMAP client compatible SpaceWire link
  - Debug Support Unit and Service interface
  - Watchdog, Timing functions
- Technology: Atmel ATC18RHA
- Package: CQFP352
- Testing according to QML-Q and QML-V



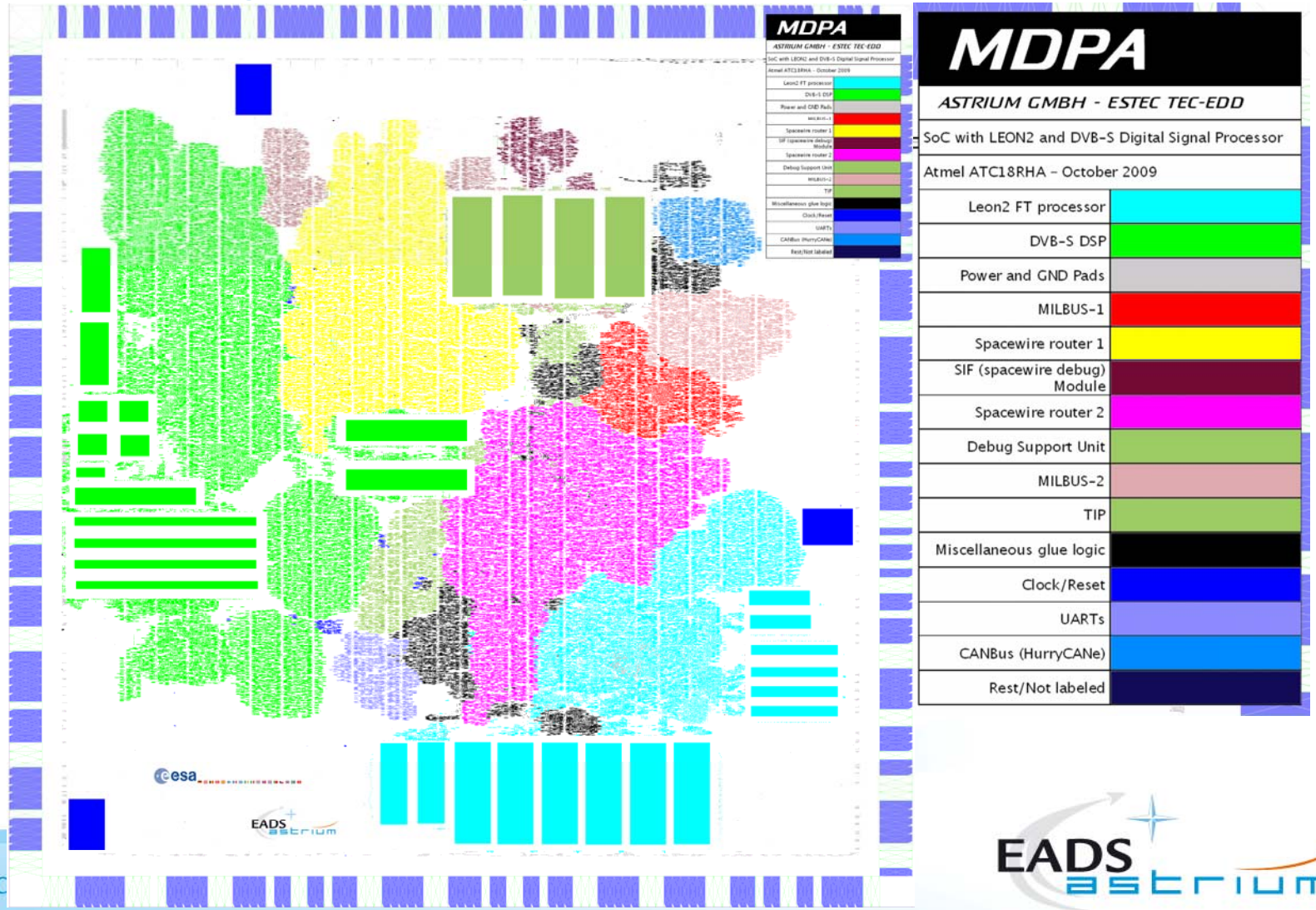
MDPA SoC Blockdiagram



MDPA SoC Elements

- Basic Elements of MDPA SoC
  - LEON2-FT Processor
  - Hardwired DVB-S algorithms
  - General Purpose Clock
  - UARTs with FIFO
  - SpaceWire I/Fs (with limited RMAP support)
  - Service Interface (SIF)
  - Two MIL-STD-1553B Interfaces (RT and BC)
  - CANbus
  - Time distribution services
    - Real Time Clock (RTC)
    - Spacecraft Elapsed Time (SCET)
    - Cycle Time (CT)
- Additional Processing Features
  - Floating Point Unit (FPU)
  - Watchdog
  - Non maskable interrupt (NMI)
  - Reset detection register
  - Software reset
  - GPIO extension
  - SRAM bank swap
  - SRAM Chip Selects
  - Debug Support via SpW and UART interface

MDPA SoC Physical Layout

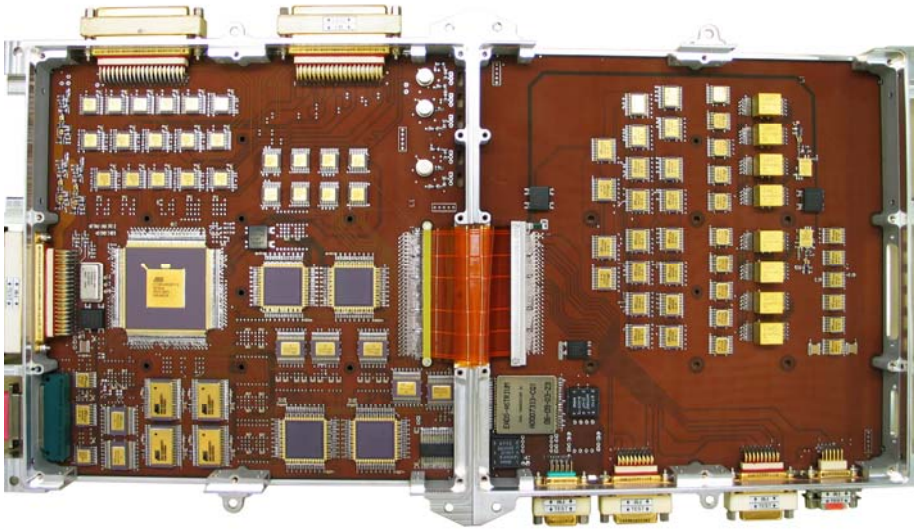


ASIC status

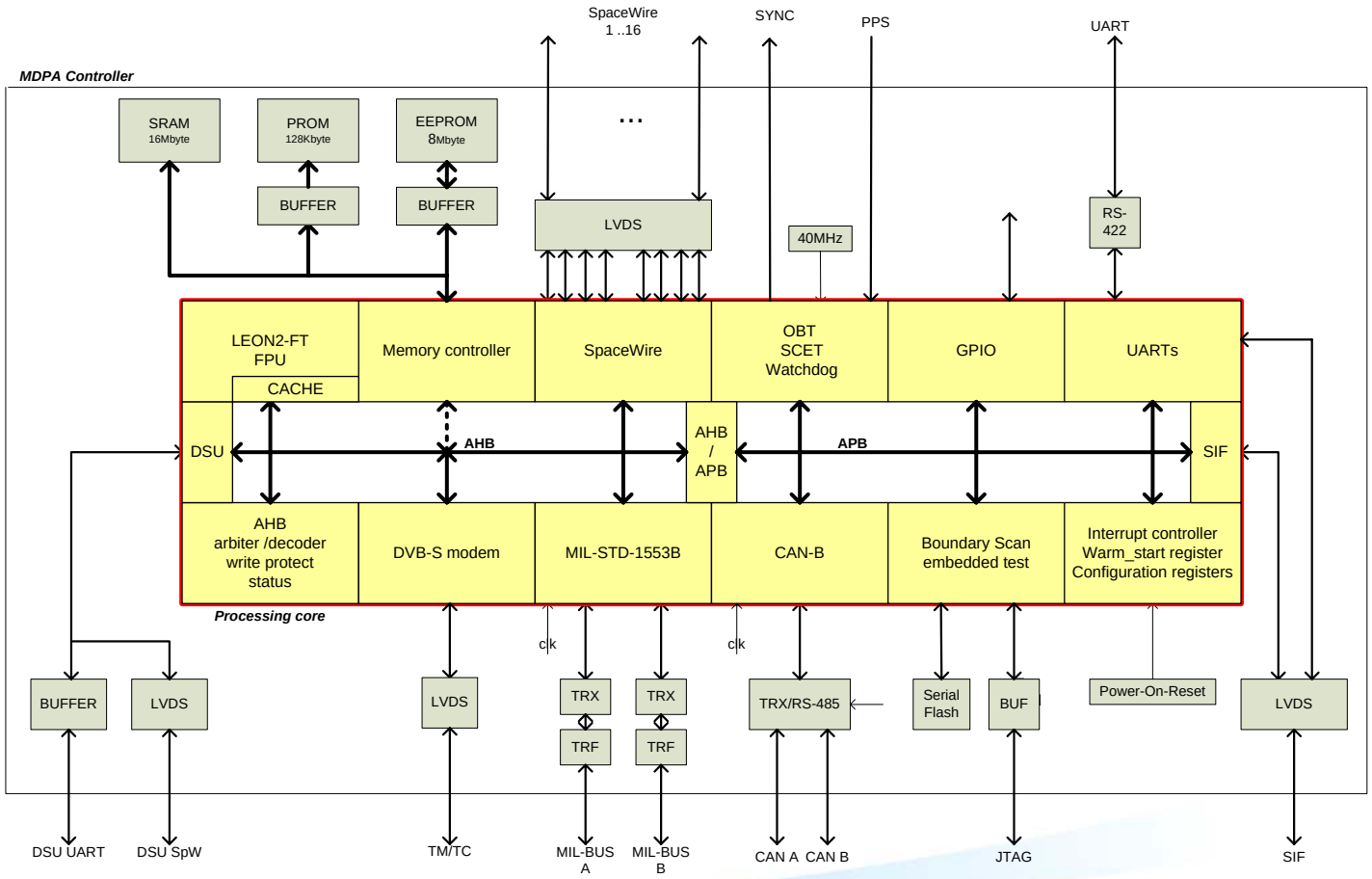
- Validation Prototypes available since July 2009
- Industrial Prototypes available since September 2009
- Industrial Prototypes have been tested by Atmel over military temperature range at speed (80MHz)
- Industrial Prototypes have been implemented on controller module board and have been fully functional tested up to 80MHz
- QML-V parts have been packaged and are currently under test at Atmel
- Availability of QML-V Flight parts: end of April

AlphaSAT Payload Controller with MDPA

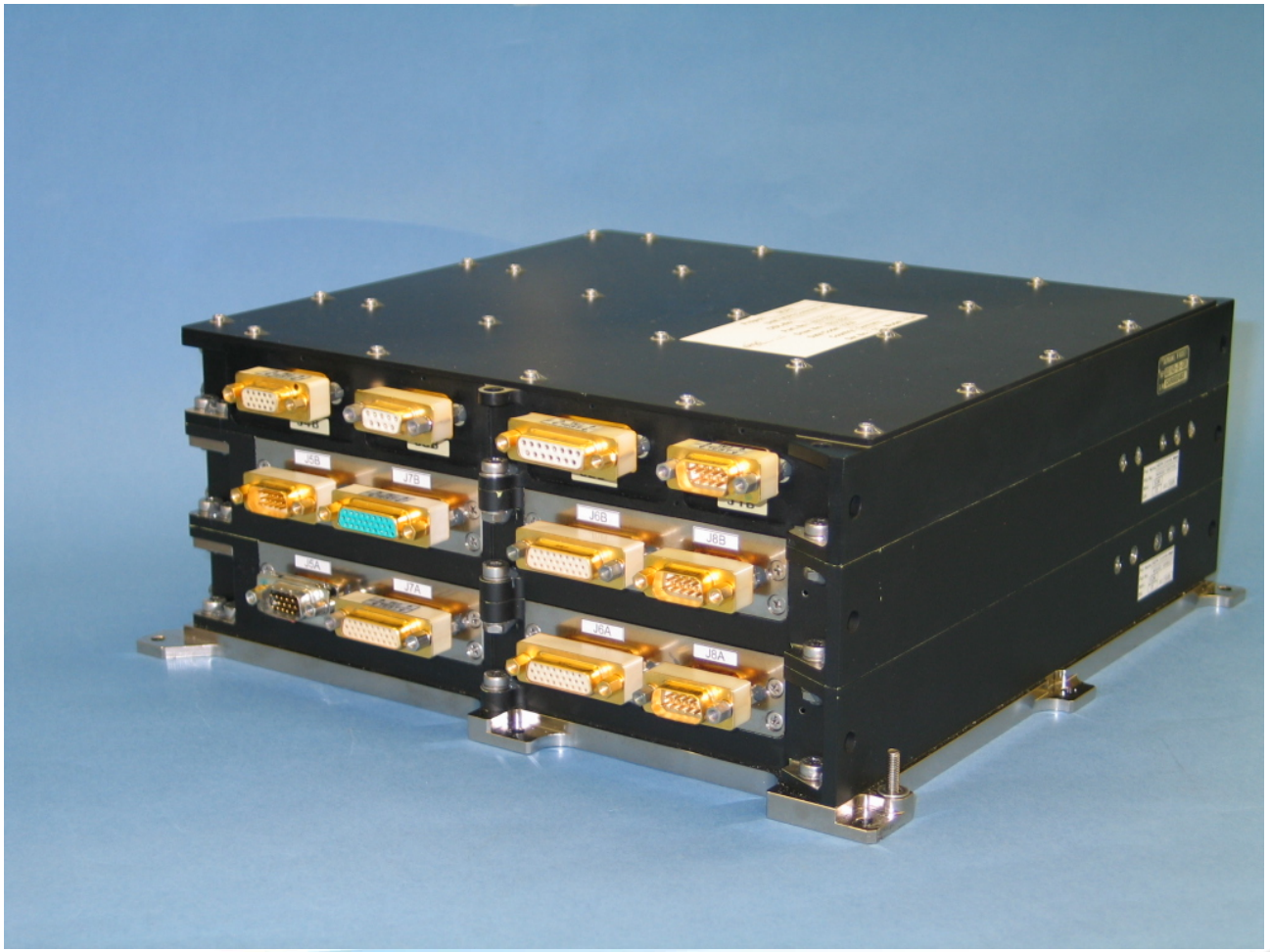
- MDPA receives mobile communication requests and configures on-board switch subsystem accordingly
- Network Control Channel is regenerated by on-chip modem
- On-Board Switch connected via 8 SpaceWire links using RMAP protocol
- Spacecraft I/F: MilBus 1553 RT
- 16 Mbyte SRAM working memory, 2x 4Mbyte EEPROM, 64KByte PROM capacity
- 15 years GEO orbit operation



AlphaSAT Payload Controller Blockdiagram

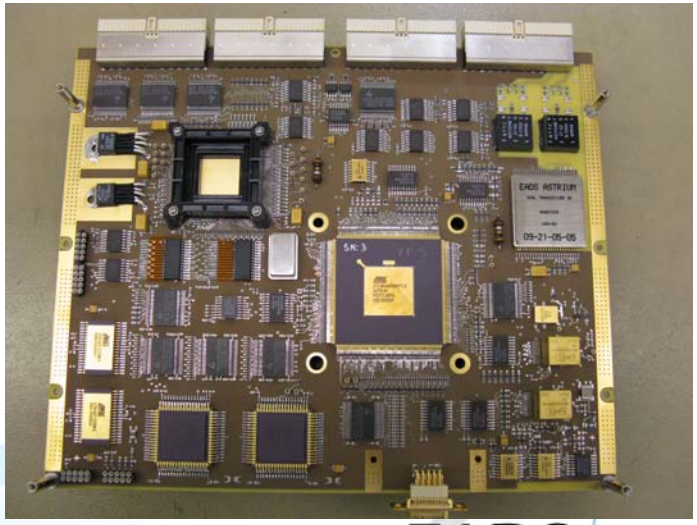


AlphaSAT Payload Controller EQM Unit



Next Generation Mass Memory Supervisor using MDPA

- MDPA based controller and file system manager for next generation flash, SDRAM or DDR-RAM based mass memories
- Supports MilBus, CAN, UART or SpaceWire external interfaces
- Internal 16bit wide parallel memory module interface
- Main advantages over ERC32:
  - Higher performance by factor 5
  - Highly integrated , lower power (3.5W for board @40MHz)
  - More sophisticated test interface (direct register/memory access via DSU; watchpoints, Breakpoints, single step etc)



Available Software Tools

- Boot strap
- Low level Software routines according to ECSS-E40
- Debug Support Unit Monitor (e.g. from Aeroflex Gaisler)
- Service Interface box (USB interface) with host tools for software download, monitoring, task level debugging and task timing tool
- MDPA simulator

Conclusion and Outlook

- First implementation of LEON2FT with SpaceWire and routing functionality
- MDPA ASIC full operational with 80MHz of processing speed
- Versatile payload equipment controller can be realised due to
  - High number of interfaces and functions on chip
  - High CPU performance at low power due to high integrated semiconductor technology (0.18micron)
  - Robustness of the design due to various error protection methods
  - State-of-the-art assembly methods (Quad flat pack)
- The MDPA chip can be made available to interested parties on case by case basis