FFTC – Fast Fourier Transform Co-processor

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Outline

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Introduction

- An existing design for Fast Fourier Transformation is converted to an ASIC, including glue logic and EDAC. The design will be proven on a dedicated testboard (FTAB)

- The FFTC ASIC is based on Eonic’s PowerFFT
  - PowerFFT is proprietary of Eonic
  - PowerFFT is a commercial product
  - PowerFFT IP is licensed by ESA from Eonic for space applications
Target Applications

- SAR Image Processing
- Radar Altimeter Processing
- Fourier Transform spectrometer data processing
- Data compression (e.g. wavelet)
FFTC Architecture

- FFTC contains 4 radix 2 processors working as butterfly engines
- FFTC provides MAC (Multiply/Accumulate) functionality
- FFTC includes internal RAM for a 1024 point FFT (using internal RAM, external RAM can be used)
- 1024 points complex FFT in less than 10 microseconds @ 100 MHz
- FFTC is manufactured in a space qualified ASIC technology
- FTAB includes address generators
- FTAB includes a sequencer and control logic
FFTCA Architecture

- Crossbar Switch
- Input Converter
- MAC Core
- FFT Core
- Output Converter
- FFTC Control

4 additional memory ports

Switch

4 configurations:

- PCFG = "00"
- PCFG = "01"
- PCFG = "10"
- PCFG = "11"
FFTCArchitecture
**FFTC Architecture**

- **FFT Core:**
  - Vector length 16, 32, ... to 1024 points

- **MAC Core:**
  - Vector multiplication of two vectors
  - Vector addition of two vectors
  - Gain / offset operation
  - Conjugate one vector and add to second vector
  - Square law detection of a vector
 FFTC Architecture

- **Control**
  - Data converters, processing core, cross-bar switch etc. are set through FFT control instructions
  - Device is programmed using high level instructions
  - Very Long Instruction Word (VLIW): one instruction sufficient for FFT up to 1024 points
  - Cycled operations possible

- **Memory Ports**
  - External memory banks provided for longer FFTs or multi-dimensional data sets
  - Are controlled and synchronised by external memory controller
  - Can be used as data buffers
ASIC Facts

FFTC ASIC is realized in ATC18RHA technology from ATMEL in the frame of a SMPW run

- Core supply voltage: 1.8 V
- I/O supply voltage: 3.3V
- gate count: 1.85 Mio
- Clock frequency: 100 MHz (data interfaces)
  128 MHz (internal)
- Package: tbd
  (SPPGA for validation protos)
- Memory ports: 4
Packaging Option: SPPGA

- SPPGA as short pin grid array is not made of alloy column but is a real pin of copper or Kovar

  - To fix the pin to the bottom of the CLGA, NTK has to modify the 2 last levels of their package: they enlarge the diameter of the pad (black line of the drawing) and they add an over coat glass layer to block the pad (see the overlap between the black and grey area)

  - The pin is also soldered to the pad but with a “high temperature alloy AgCu” than cannot be removed when soldered without damaging the soldering area
FFTC Demonstration System

- **FTAB - FFTC Accelerator Board**
  - Serves as a demonstrator for the FFTC device
  - Can be used as a building block for high performance on-board signal processing units
  - Can be connected to a SpaceWire network, allowing scaling of processing performance for application requirements

- **FFTC demonstration system is based on**
  - FFTC Accelerator Board
  - Host (test) computer (PC)
  - SpaceWire PCI interface board

- **FFTC Validation including**
  - Application of data vectors used in the verification as golden pattern
  - Fast data processing/generation, using LFSR data generation in FTAB (to overcome data rate limitations implied by SpW-link)
FFTCAccelerator Board (FTAB)

- Buffer Memory 1
- Buffer Memory 2
- Buffer Memory 3
- Buffer Memory 4

FTAB Controller and Address Generator

SpaceWire Links

CMD

Status/Control

Address/Control

P0

P5

57+6

57+6

57+6

57+6
FTAB controller block diagram

- **Router Matrix**
  - Port 0 data
  - Port 5 data

- **Sequence Controller**
  - Control & Status Register

- **FTAB Configuration**

- **Ports**
  - Port 0 controller
  - Port 1 SDRAM controller
  - Port 2 SDRAM controller
  - Port 3 SDRAM controller
  - Port 4 SDRAM controller

- **Additional Components**
  - SpaceWire cell
  - Controller / interpreter
  - FFTC controller

- **Data Flow**
  - Data transfer between components

- **External Connections**
  - p0 (63:0)
  - p5 (63:0)
  - CMD

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FFTTC Accelerator Board (FTAB)
FTAB Support software

- Host computer controls the FTAB via SpaceWire
- Communication between Host and FTAB via SpaceWire
- Perform FFTC and FTAB configuration
- Send commands for FFTC via SpaceWire
- Data transfer to and from FFTC via SpaceWire
- Communication is based on RMAP
Status

- (Re-) Start of the FFTC project: March 2007 ✓
- Requirement Review: July 2007 ✓
- Feasibility Study Review: August 2008 ✓
- Logic Review: March 2009 ✓
- Design Review: November 2009 ✓
- MPW: Spring 2010 ✗
- Validation Prototypes: Summer 2010 ✗
- Industrialization Prototypes: Summer 2011 ✗
- Project end: Summer 2011 ✗