Modernised GNSS Receiver and Design Methodology

March 12, 2007

Overview

- Motivation
- Design targets
- HW architecture
  - Receiver
  - ASIC
- Design methodology
  - Design and simulation
  - Real Time Emulation
  - Software module validation

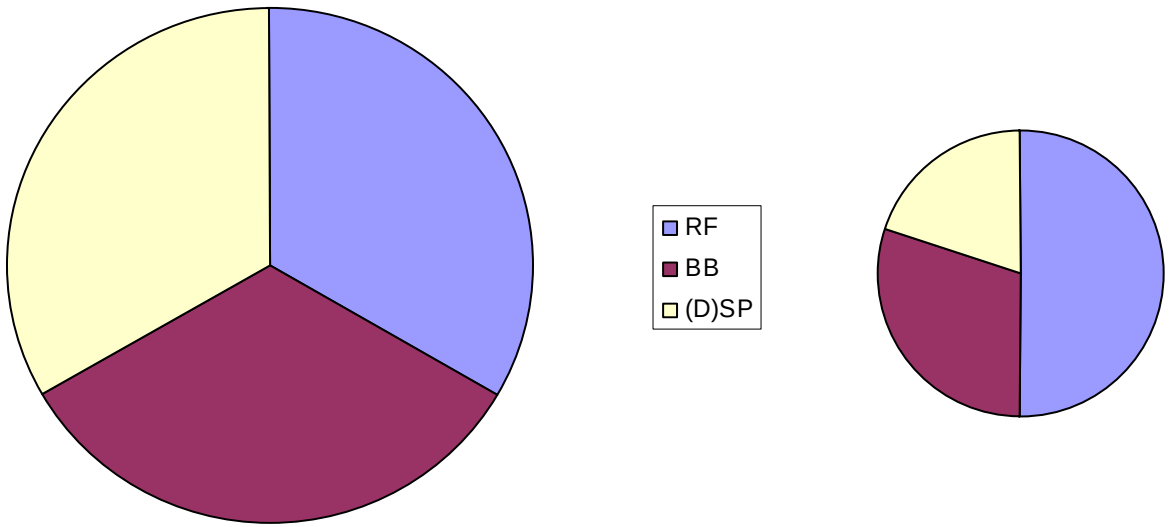
Motivation

Motivation

- Facts
  - New signals (beyond classical L1/L2 GPS and EGNOS)
  - Increased interest in Glonass
  - New applications
- Applications for high end receivers
  - > 100 channels tracked
  - Survey, timing receivers, machine control .....
  - Multiple antenna´s, RTK, attitude,....
- State of the art
  - Fast acquisition
  - Low power consumption

Motivation

- Power reduction in 3 domains



- Situation 2001 → Situation 2007
- Gain through technology and integration level

Motivation

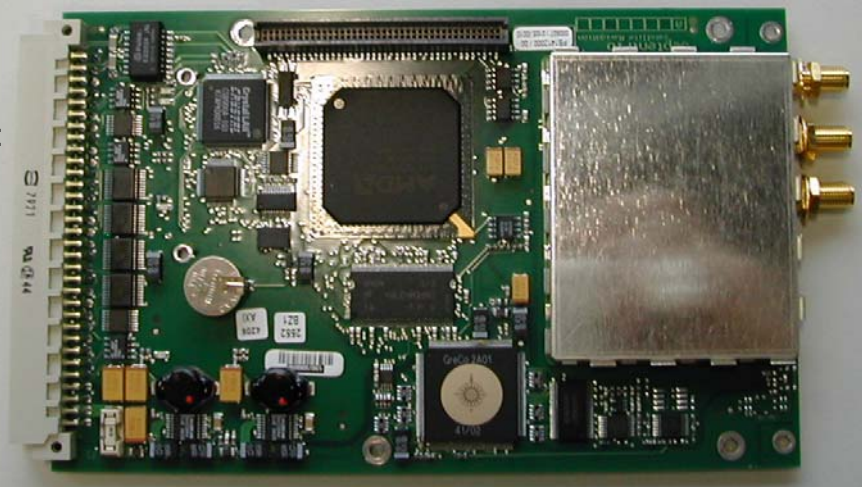
Example:

2005 design:

1.2 Watt

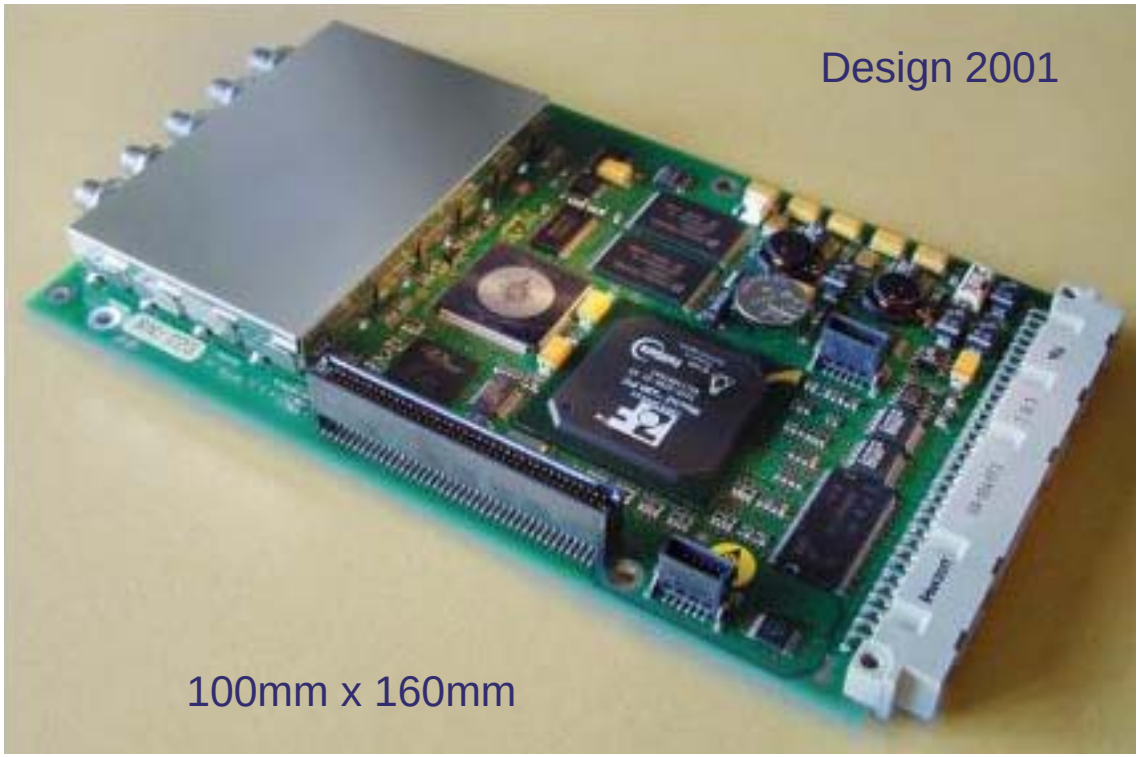
2001 design:

7 Watt



Motivation

- Size reduction



Design 2006

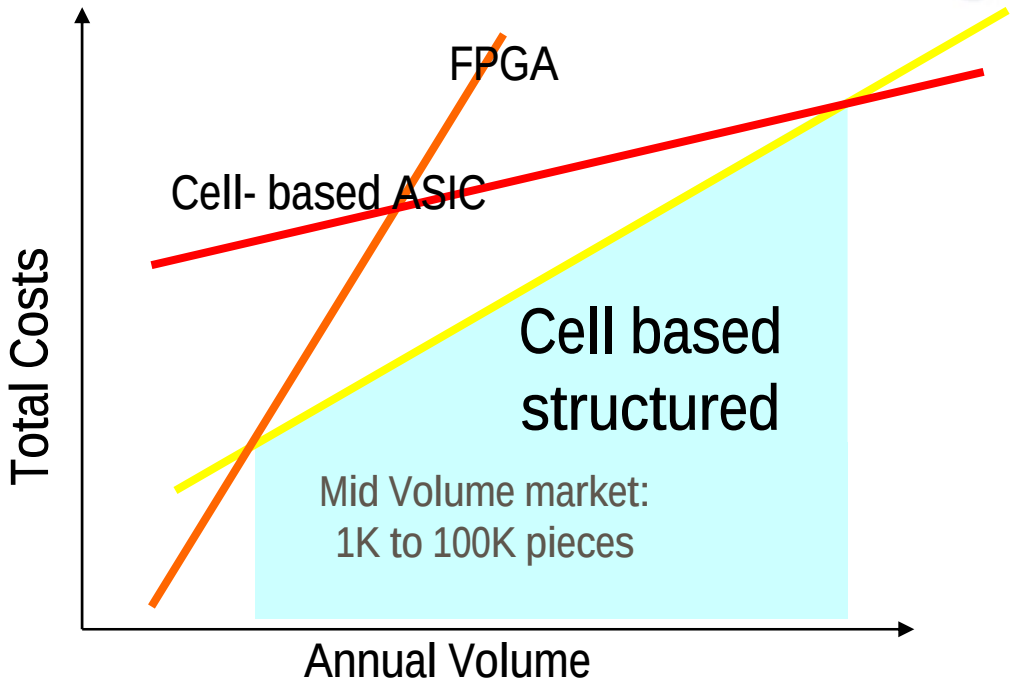
56.5mm x 76.4mm

Design targets

- Professional receivers
  - High availability (“All-in-view” tracking)
  - Mm level accuracy and high update rate
  - Integrity
- Practical in use
  - Fast (re)acquistion
    - Rovers
  - Accurate timing
- Engineering concerns
  - Scalability
  - Programmability
  - Technology independence and portability
  - Testability
  - ROHS

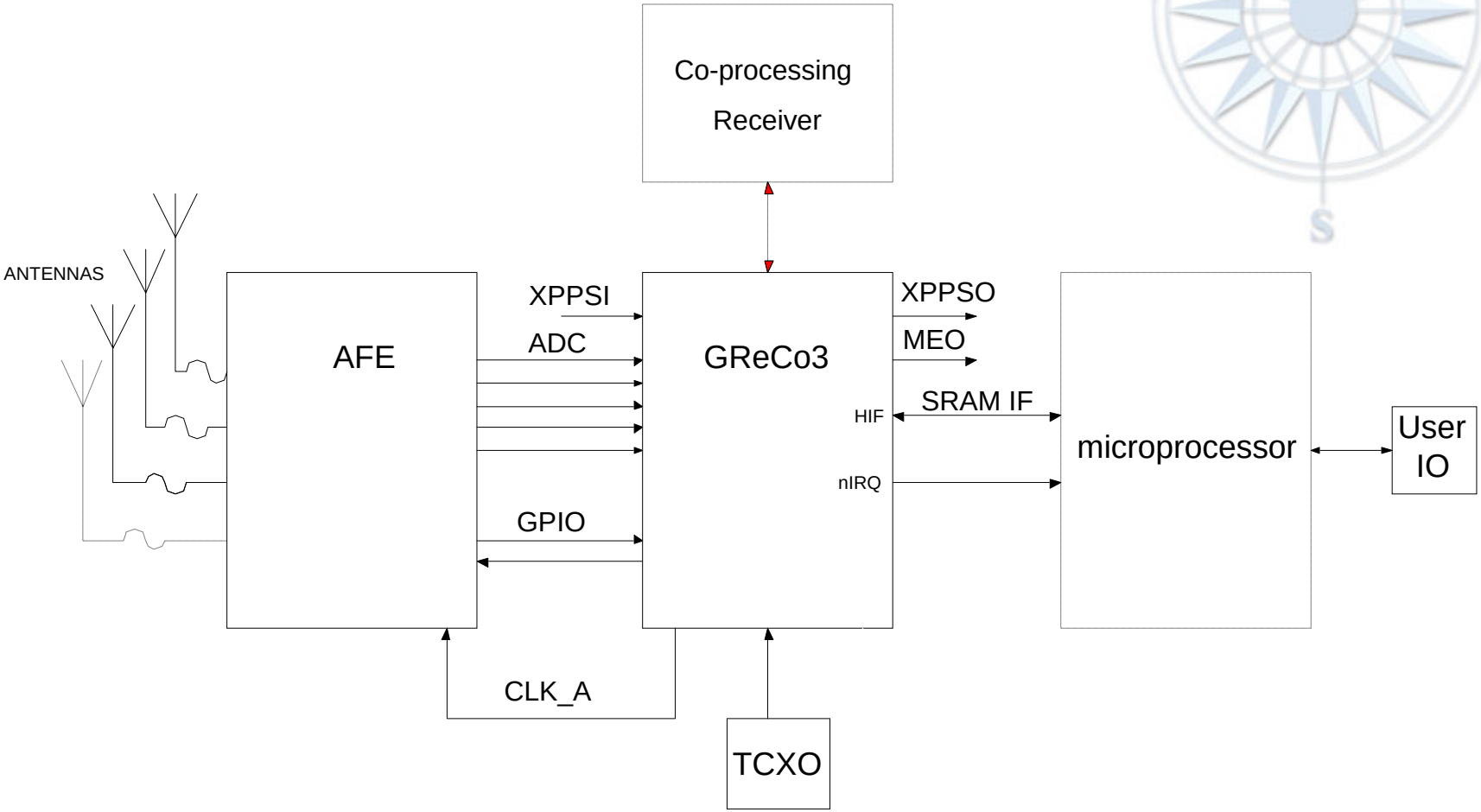
Design targets

- Efficient Design and Technology
  - Size and Cost : FPGA vs ASIC



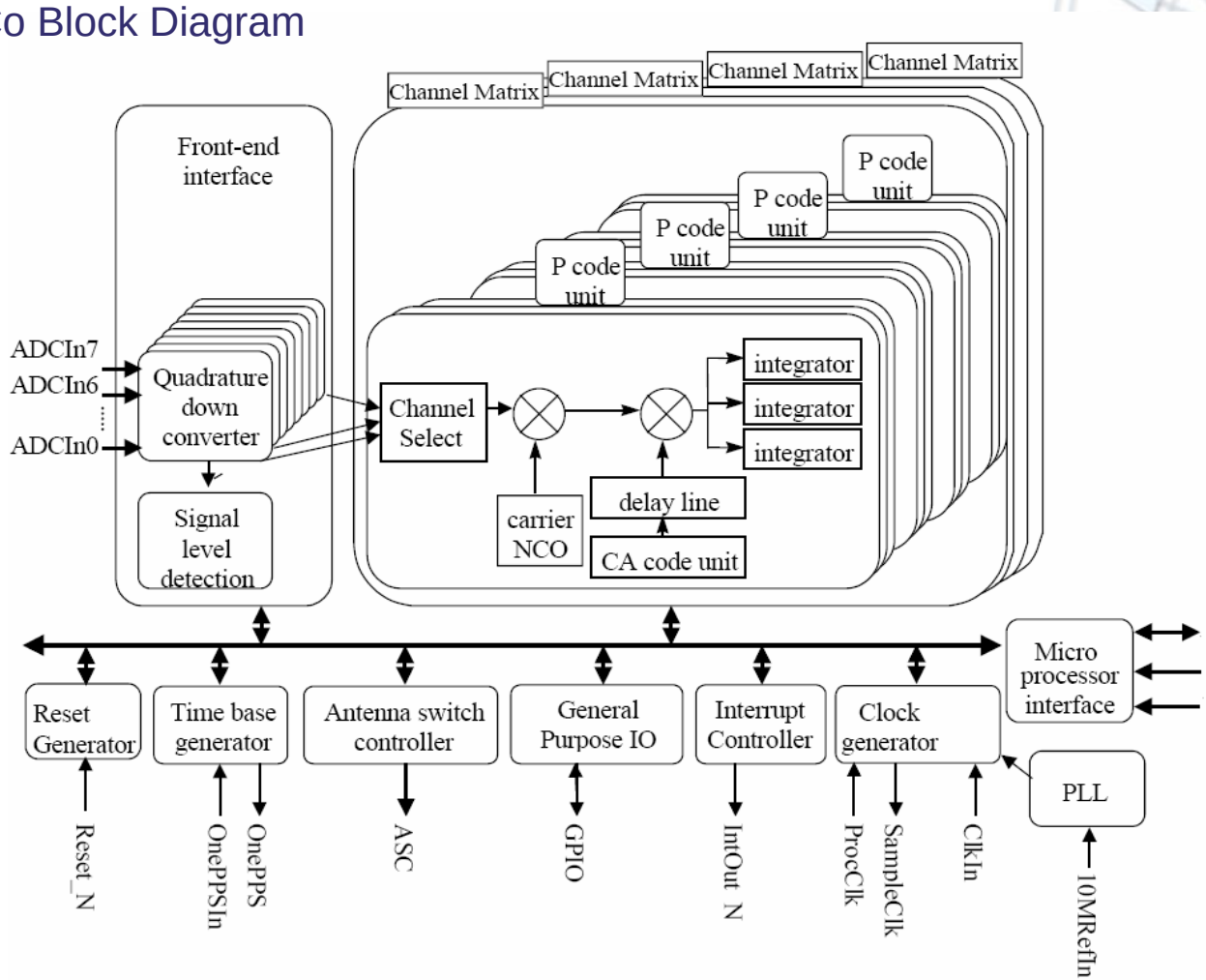
HW architecture

Receiver architecture



Evolution, not revolution

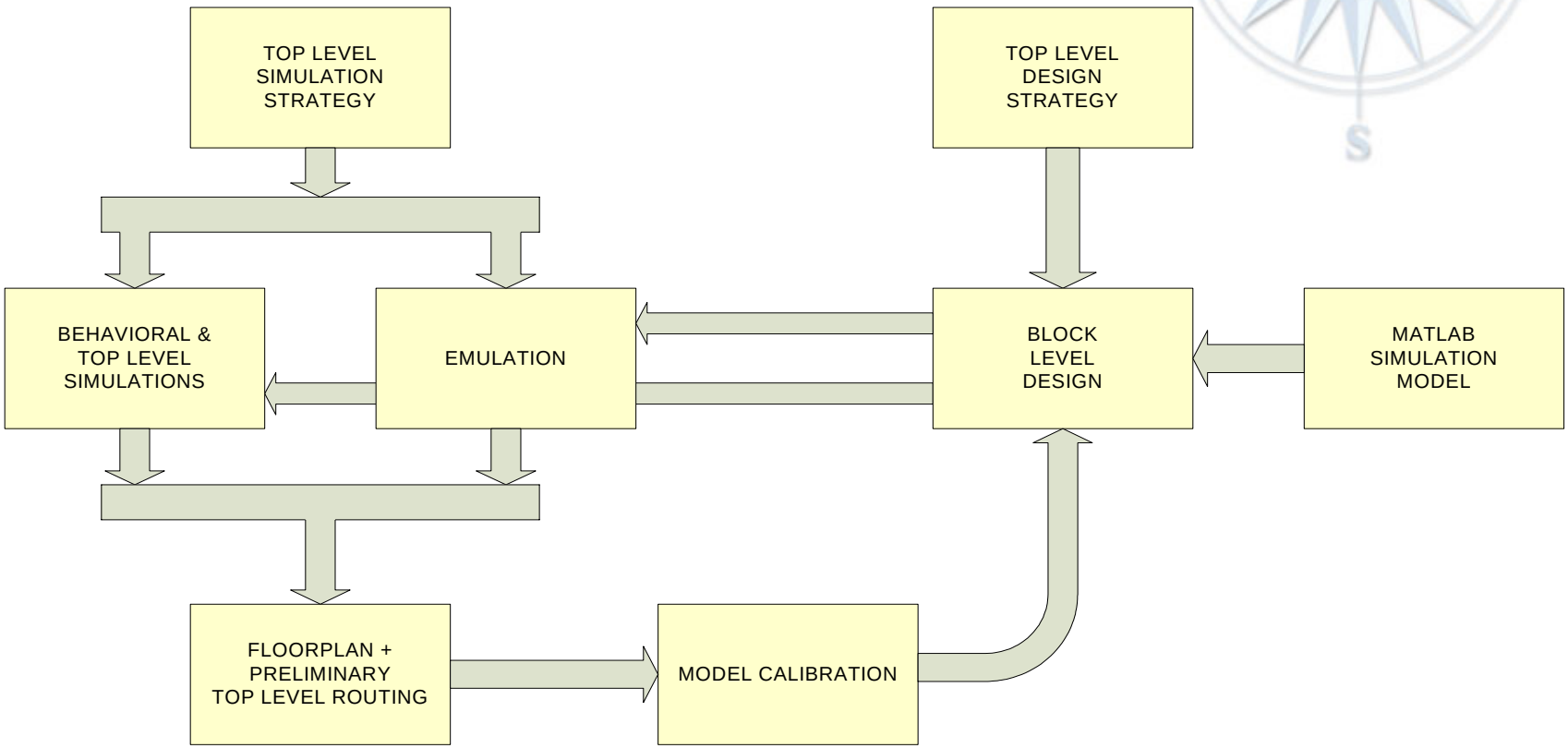
- GReCo Block Diagram



GReCo3 Functionality

- GReCo3 supports
  - GPS modernisation and new signals (L2C, galileo codes, memory codes,...)
  - Multi constellation/Antenna support (5 FrontEnd inputs)
  - Large number of universal channels
  - Fast Acquisition Unit
  - HW co-processing units
  - Multipath mitigation support
  - Interference detection functionality
  - Improved NCO resolution
  - More observables
  - Clock steering functionality
  - Watchdog and support functions
- Synergy: baseband operation with Galileo1 RF ASIC possible

GReCo3 Design Methodology



GReCo3 Design Methodology

- "Platform independent" design allows
  - easy FPGA prototyping
    - Increases first-time-right ASIC port
    - Allows early SW co-design
  - Project interchangebility
    - Sharing IP modules over projects on different platforms
  - Matlab simulation models
    - Higher visibility on dynamic range DSP units
    - in-depth emulation of various HW units

GReCo3 Design Methodology

- GNSS specific design issues
  - Long codes, large number of space vehicles
  - Signal structure
    - Generating test vectors is time-consuming
    - Complexity to create real-world scenario
      - Cross-correlation, multipath,...
  - Side effects
    - Code/carrier phase measurement hard to simulate
  - Early performance evaluation
    - Conformance with theory
    - bandwidth – performance trade-off

GReCo3 Design Methodology

- Non GNSS specific design issues
  - Asynchronous MP interface
    - Clock difference GNSS and microprocessor
    - 16/32 bit interface, little/big endian
      - Maximum compatibilty
  - Benefits of hardware co-processing units
    - Trade-off
      - Less host processor load
      - More IO cycles to transfer data from/to ASIC

GReCo3 Design Methodology

	complexity	vhdl testbench coverage	emulation
Channel type 1	medium	93% coverage not 100% due to : large number of SV codes lots of modulations flexibility/compatibility	focus on : testing all SV codes testing different modulations long-term data-logging (counter drifting)
Channel type 2	high	97% coverage not 100% due to : very long codes	focus on : tracking implementation verification of all SVs through long-term data logging verify interface with tracker CA-channel
MPIF	high	99%	focus on : long-term verification hardware delay independency remove vhdl processor-model dependency
FAU	high	96% coverage not 100% due to : large number of possible codes limit dynamical range not reached very flexible settings	focus on : verify large number of codes verify large subset of settings verify cooperation with tracker channel
RFE	low	98% coverage not 100% due to : interference detection logic	emulation to be done

Conclusion

- Emulation brings benefits
  - Efficiency
    - More cases can be investigated
    - Realtime emulation up to 10.000x faster than simulation
  - SW re-usable
    - Engineering sample testing
    - End product
- Not entirely free of risks
  - HW parameters are not tested
  - Not a replacement, but a complement for RTL simulation