NPT-C 0.13um ASIC

Digital Processor Technology Enhancements
ESA Contract: 16948-NL-JSC

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Processor Product Group

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Introduction

The NPT-C, designed using the STM HCMOS9 technology, is the latest ASIC to be completed in the EADS Astrium Processor Product Group.

Acknowledgements
Objectives
ASIC Architecture
Radiation Test Structure
Increased Design Integration
Radiation Test
Progress and Summary

UK EXPORT CONTROL SYSTEM EQUIPMENT & COMPONENTS RATING: 3A001a1a, 3A001a2, 3A001a3, 3A001a10, 3A001a11, 4A001a.
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Acknowledgements

- Astrium
  - Specification, Design and Verification
  - Synthesis and Static Timing Analysis
  - Test vector generation
  - Radiation test

- Dolphin Integration - Vendor interface
  - Placement and routing
  - Test vector translation
  - Manufacture and test coordination

- STM
  - Radiation hard buffer
  - Layout guidance
  - Manufacture
  - ATE facilities

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Objectives

- Gain design experience through development of large scale ASIC which supports complete functionality of an Inmarsat 4 MCM.
  - This ASIC is equivalent to a (10 chip) multi chip module used on the Inmarsat4 satellite and includes four radiation test chains.

- Gain an insight into design flow issues associated with multi-million gate ASIC designs.
  - 64 bit versions of tools used now allows much larger designs to be processed.
  - Investment in new machines with more memory alleviated issues.

- Facilitate the analysis of the radiation hardness of both the technology and various design configurations.
  - While the radiation tests have yet to be performed, the objectives is to compare the SEE performances of the four test chains and gauge the effectiveness of the majority voting schemes used.

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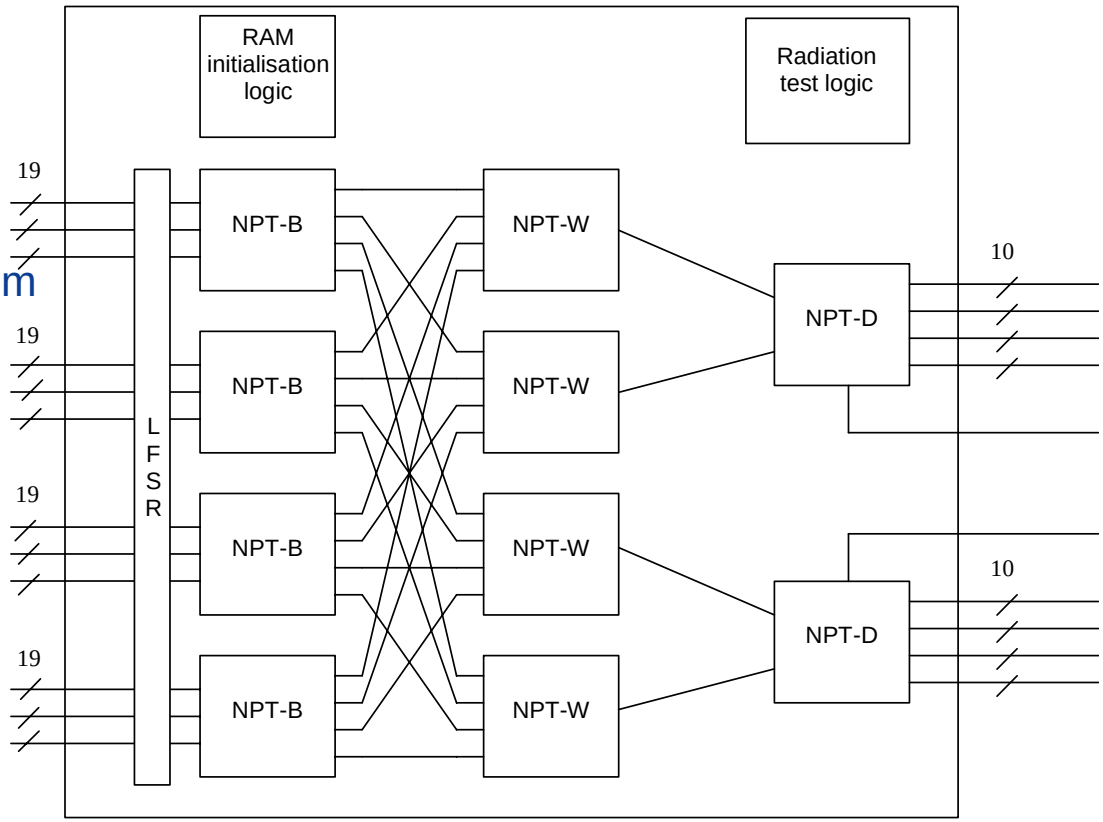
ASIC Architecture

- NPT-C Functionality comprises
  - 4 NPT-B, 2 NPT-D and 4 NPT-W (functionally equivalent to Inmarsat 4 MCM-C)
  - RAM Initialisation
  - Radiation Test block
  - LFSR
- Chosen Technology
  - STM HCMOS9 0.13um



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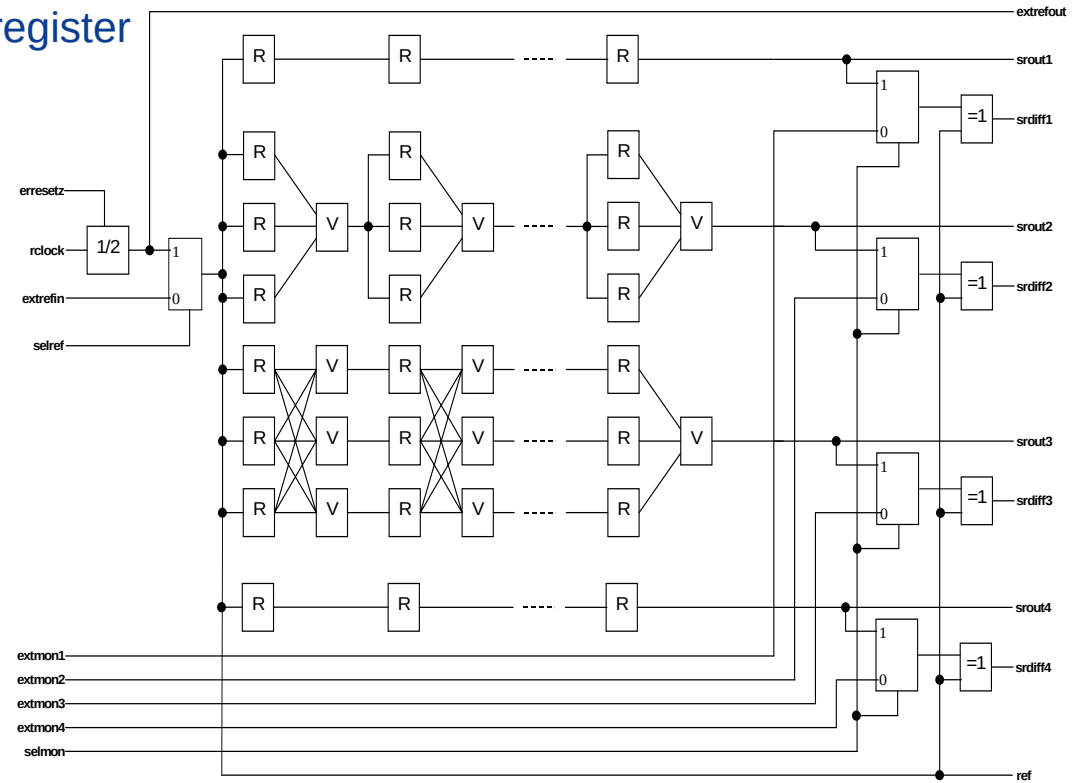
Radiation Test Structure (1)

- The radiation test block forms the majority of the NPT-C in terms of size, it contains
  - Shift register 1 : standard registers chained together
  - Shift register 2 : TMV register configurations chained together
  - Shift register 3 : TMV register and voter configurations chained together
  - Shift register 4 : radiation hard registers chained together
  - 64000 stages/shift register



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Radiation Test Structure (2)

- Radiation Hard Asynchronous Control Trees
  - Chips containing standard clock trees had been tested with heavy ions by STM
    - It was found that multiple upsets had been induced in the clock trees.
      - Addressed by the development of a radiation hard buffer.
  - NPT-C baseline had been to use a radiation tolerant tree.
    - An ion impact may induce multiple upsets in this radiation tolerant tree.
    - The susceptibility of this tree was unknown.
    - The NPT-C radiation test objective is to measure the effectiveness of TMV techniques, and this may be undermined if upsets are induced in the asynchronous control trees.
    - Correlating measurements against the actual event may be difficult.
  - Decision taken to use the radiation hard buffer in 3 of the 4 test chains.
    - It is hoped that the radiation test results will confirm that SET disturbances in the asynchronous control trees do not propagate.

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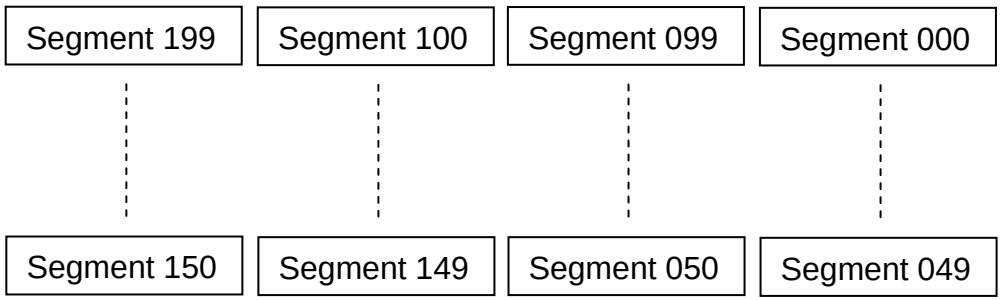
Radiation Test Structure (3)

- The placement of each segment type was done manually with segment placement then being repeated within each shift register.



  - Manual placement was required because the auto placement method would not account for the radiation guidelines (no rules for radiation placement).
- While manual placement has been possible for the NPT-C, automatic means would have been preferred.
  - If radiation guidelines are to be implemented, they should be automatically handled by placement tools and this is considered vital for future ASICs.
  - Indeed, extensive manual placement of non-repeated structures to meet radiation placement rules is considered daunting (if not infeasible) for large designs.
- Auto placement rules that account for radiation placement should be developed.

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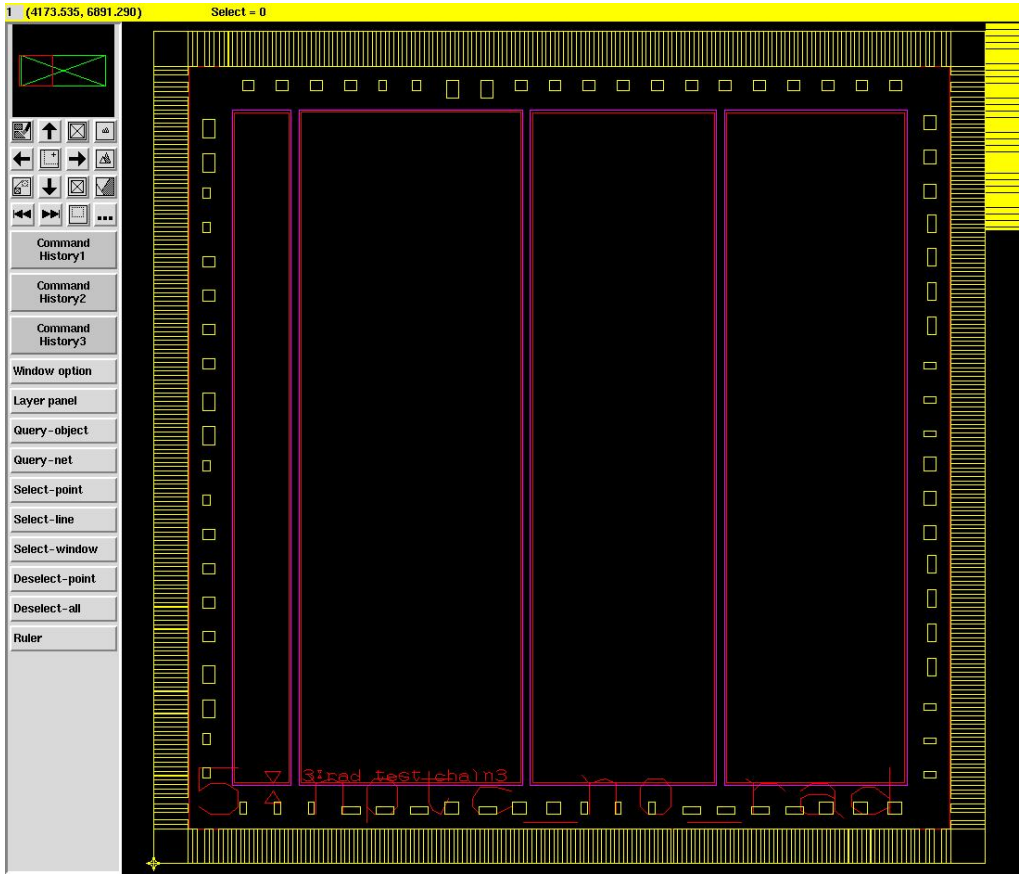
Radiation Test Structure (5)

- **Note size of Radiation Test Block vs. MCM functionality.**



Shift register	Area mm^2
Std d-type, no TMV, RT control	3.67372 (0.57482 x 6.39108)
Std d-type, triple register, single voter, RT/RH control	11.10250 (1.6728 x 6.63708)
Std d-type, triple register & voter, RT/RH control	13.08354 (1.97128 x 6.63708)
RH 12T d-type, no TMV, RT/RH control	11.52963 (1.80402 x 6.39108)

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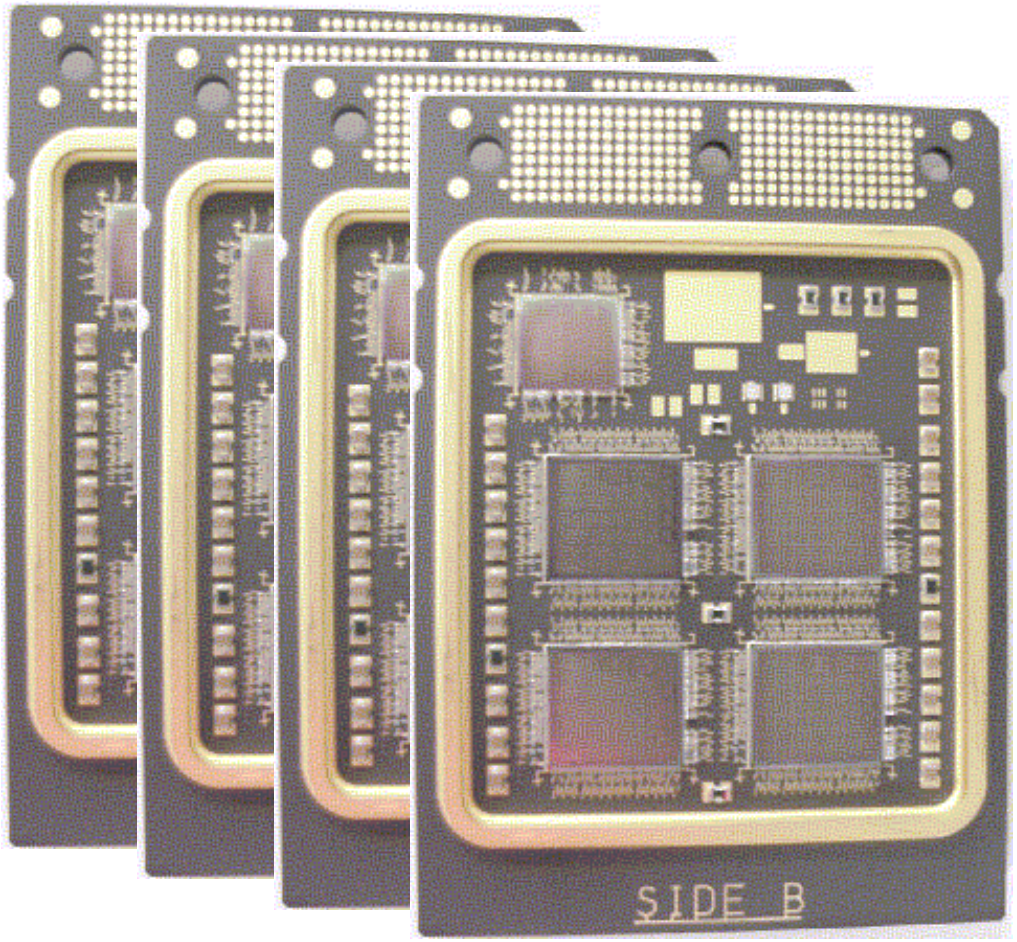
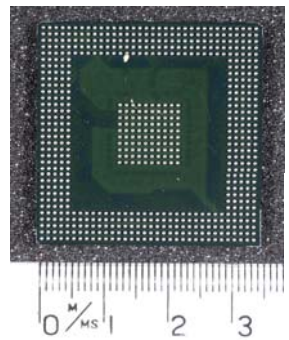
Increased Design Integration

- **MCM functionality corresponds to approximately 25% of NPT-C core area.**





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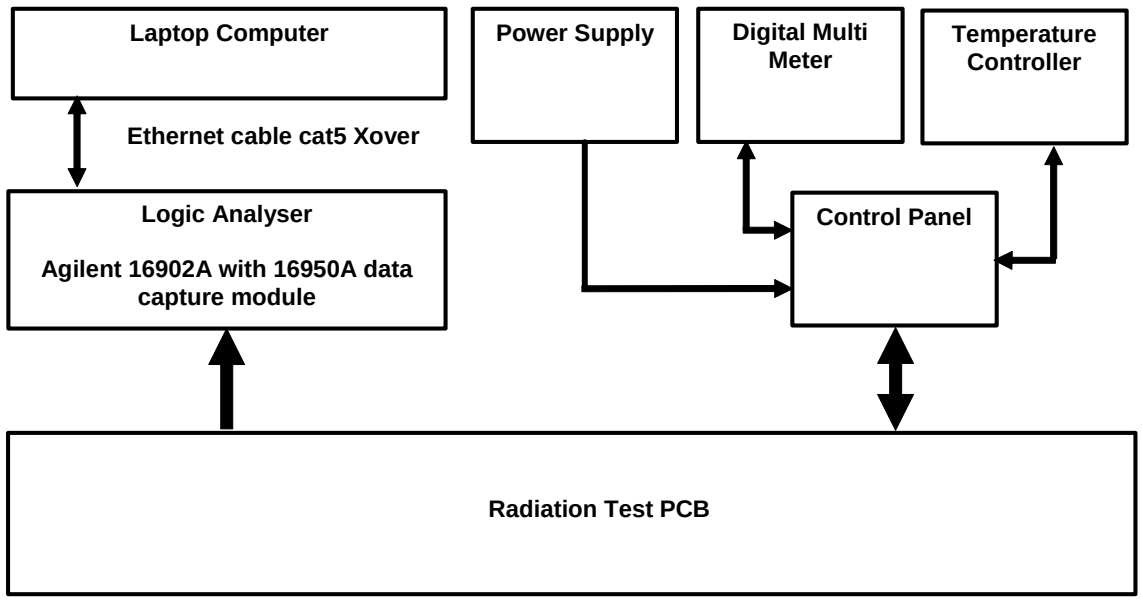
Radiation Test (1)

- **Radiation Test**
  - Radiation test plan and procedure has been written.
  - Develop necessary test PCBs as required for the test programme.
    - FPGA and PCB design and manufacture is underway.
  - De-pot or de-lid ASIC samples as necessary.
  - Perform radiation test on the ASIC samples.
  - Produce radiation test report.

- **Radiation Test Concept**



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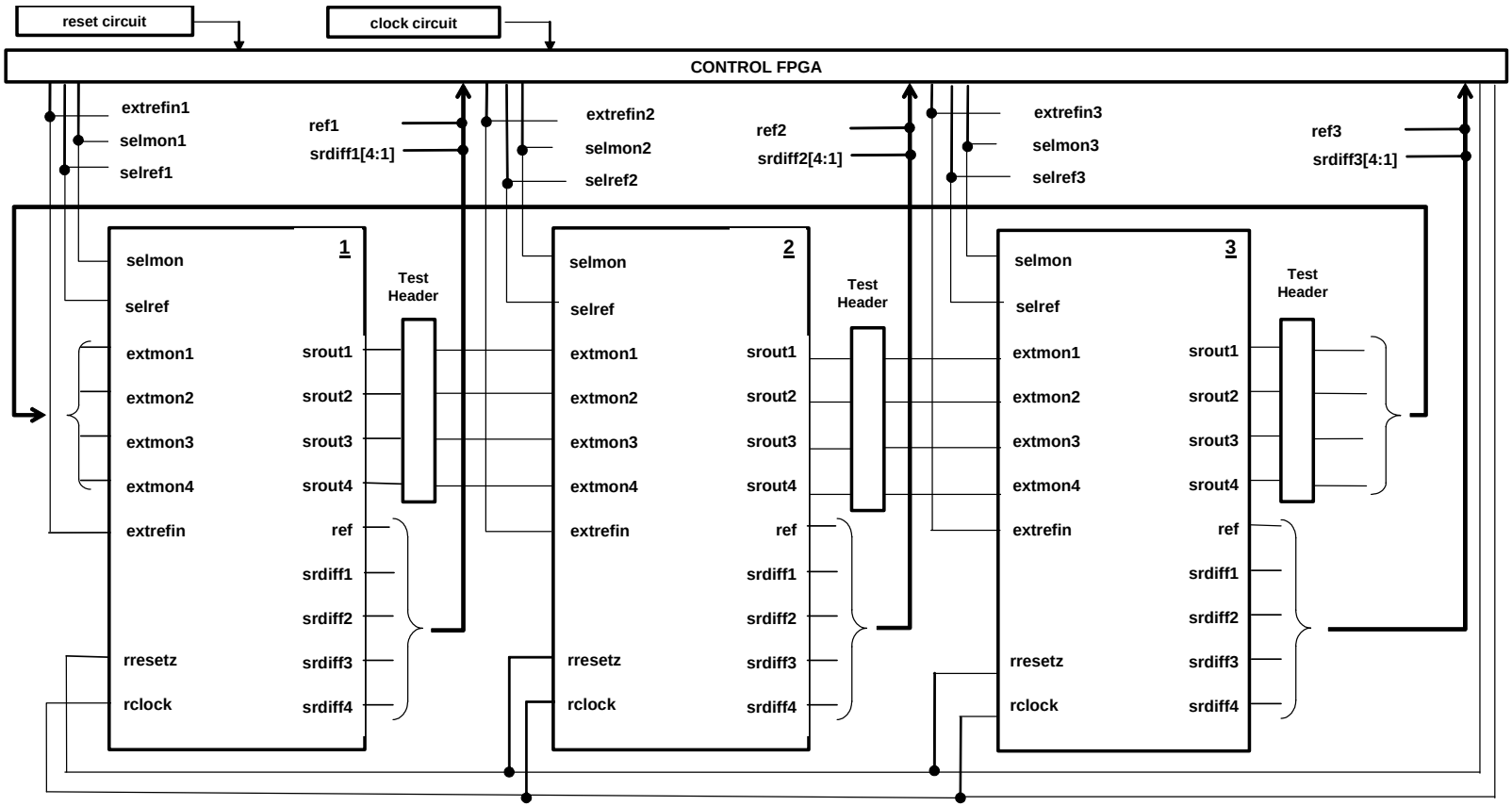
Radiation Test (2)

- **Radiation Test Architecture**



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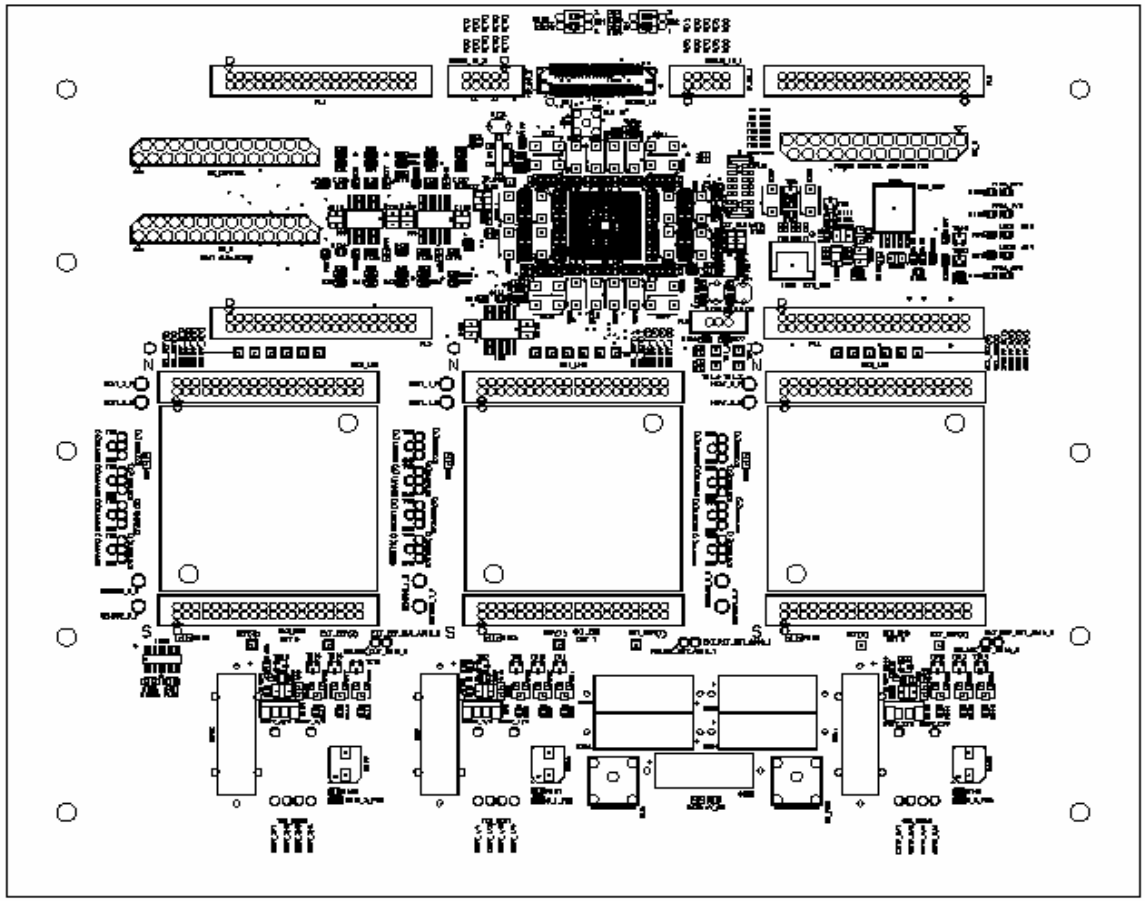
Radiation Test (3)

- **Motherboard**
  - 3 ASIC daughter boards
  - Adjustable ASIC power supply
  - Intelligent FPGA
  - Data compaction



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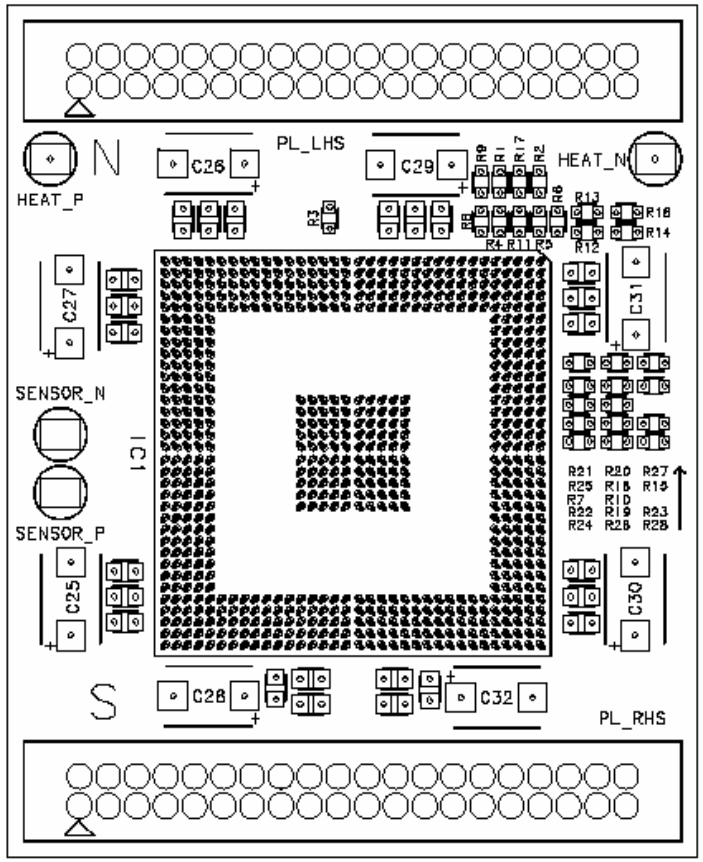
Radiation Test (4)

- **Daughterboard**
  - Heater
  - Temperature sensor
  - Thermally coupled to motherboard



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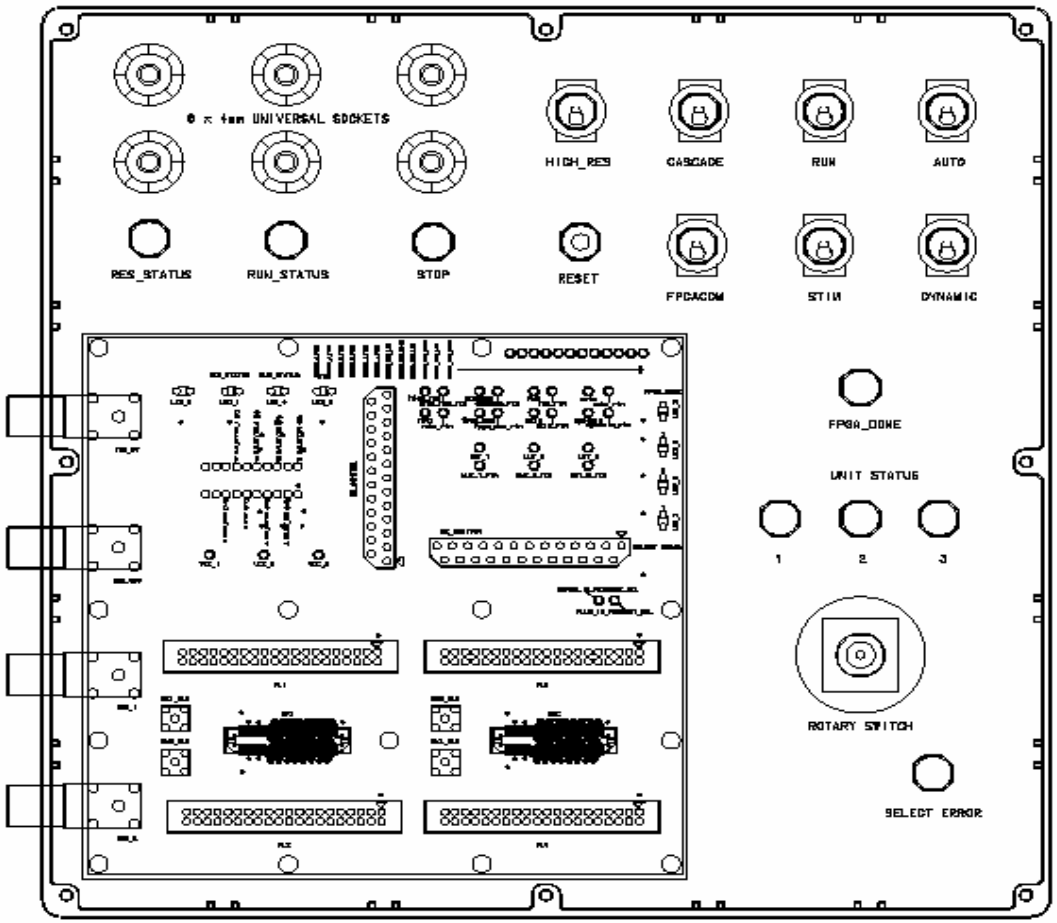
Radiation Test (5)

- **Control Box**
  - ASIC stimulus
  - Start test
  - Select ASIC
  - Select compaction
  - Select voltage
  - Measure ASIC current and voltage



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Progress and Summary

- The ASICs have been delivered.
- The Radiation Test Plan has been issued.
- The control FPGA design has been coded and synthesised.
- The design and specification of the test system is complete.
- The PCB manufacture/assembly/commissioning has been started.
- The test equipment has been received.
- Radiation test is planned for May/June 2007.
- Radiation test report.