FLIPPER

SEU Fault Injection in Xilinx FPGAs

ESA/ESTEC Contract n. 8559/NL/LvH/gm

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Outline

- Overview
- Basic principle and main features
- Case study
- Preliminary results
- Conclusions

FLIPPER what is it?

FLIPPER is a flexible XC2VP20-based board conceived as a powerful hardware platform for the following main application

- SEU emulation by fault injection in Virtex II devices (patent pending)

FLIPPER can be used in more general ways

- radiation ground testing
- test equipment
- digital I/O board
- general purpose Virtex2 board
- …

Why FLIPPER?

- SEUs are of utmost concern for Xilinx devices as functionalities are sensitive to unintended change in configuration memory
- Fault Injection tools able to adequately address "reacheable" radiation sensitive parts, are useful
- Our objective is providing one tool able to:
  - inject SEUs into the configuration memory
  - manage a high number of I/O pins
  - exercise a DUT device performing on board comparison of test results

FLIPPER basic principle

- SEU injection by *active partial reconfiguration*
- SEU injection by configuration adopted in an earlier prototype for Virtex I*
- Close approach, yet with different purposes, used by FT UNSHADES
- Reported approach by the literature in the FI field (e.g. R. Leveugle)

** Alderighi et al., Proocedings of the 18th IEEE Int'l On-line Testing Symposium, 2003*

Alderighi et al., Proocedings of the 9th IEEE Int'l Conference on Defect and Fault Tolerance in VLSI Systems, 2003

FLIPPER what's for

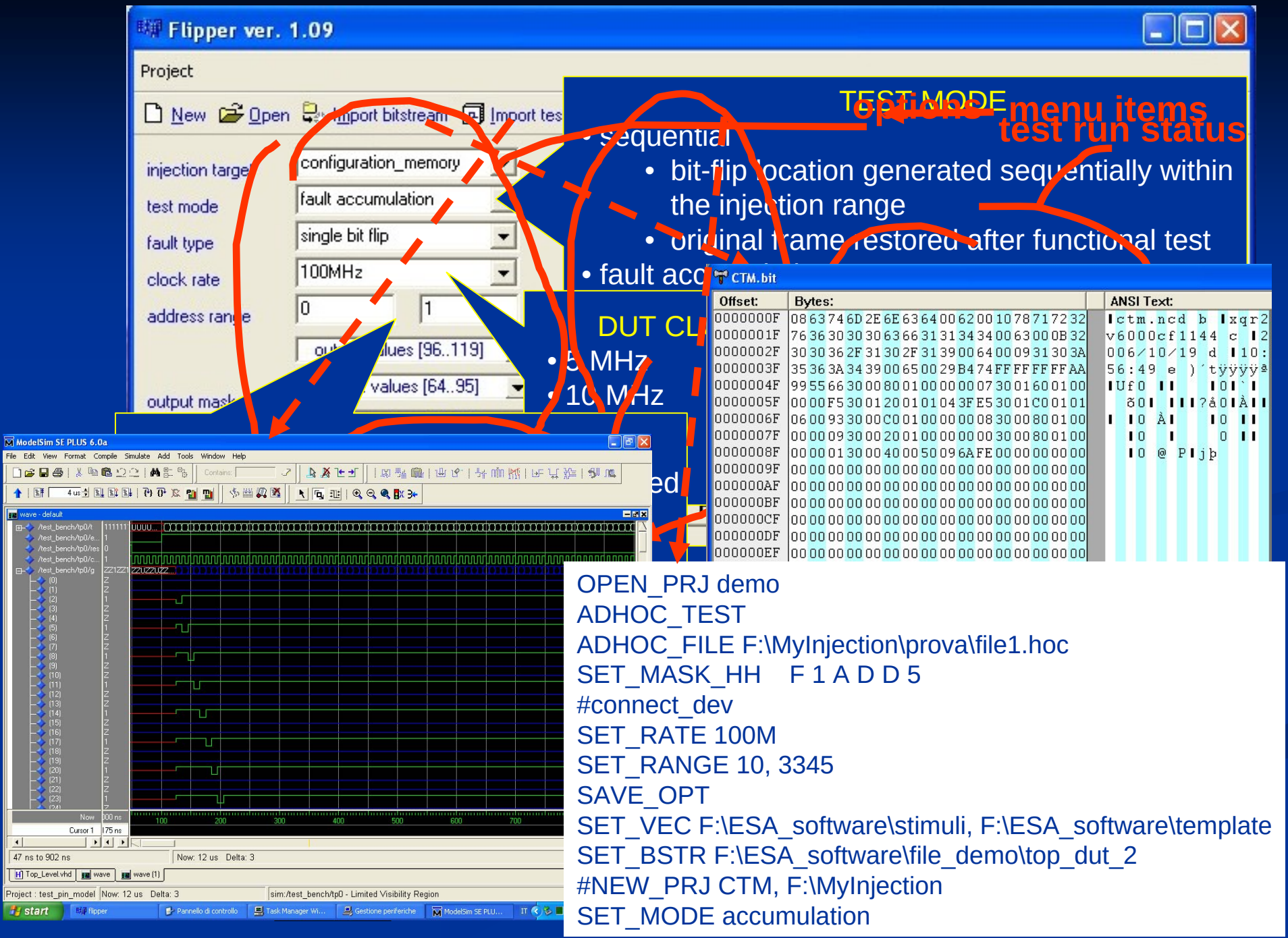
- Analyze SEU effects in designs implemented in Xilinx FPGAs
- Study SEU effects in Xilinx FPGA reconfiguration logic
  - by means of a write operation into configuration logic registers
- Evaluate/compare mitigated designs in one/selected device(s)

FLIPPER features

- SEU emulator comprising hardware, firmware & software
- Fault injection based on frame modification and active partial re-configuration
  - Verified through JTAG & Impact verify
- Single bit and multiple bit upsets
- Test vectors and gold vectors imported from ModelSim simulation
- Test vectors up to 150 bit wide and gold vectors up to 120 bit wide
- ≈ 26000 test vectors @10MHz → ≈ 11 injection/s with max. I/O port width

FLIPPER features (cont'd)

- After each injection the DUT is exercised for the whole set of test vectors
- Test/gold vectors comparison performed on board. In case of mismatch, a fault packet is sent to the PC containing:
  - # of the current injected fault
  - # of the current test vector
  - Ex-OR between the current DUT outputs and the expected (gold) values
- DUT FPGA's pin wired together in triplets on the DUT board to implement XTMR-ed designs
- XQR2V6000 used as DUT for ESA contract
- Test execution either via GUI interface or in batch mode
- Injection mode and options selectable via software

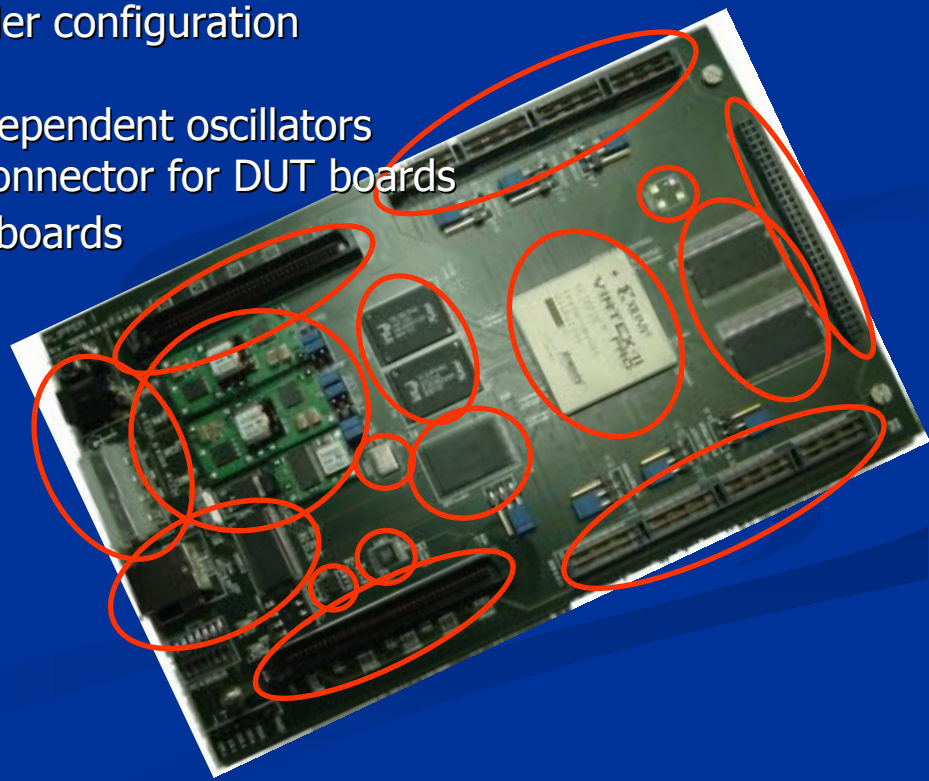



```
OPEN_PRJ demo
ADHOC_TEST
ADHOC_FILE F:\MyInjection\prova\file1.hoc
SET_MASK_HH    F 1 A D D 5
#connect_dev
SET_RATE 100M
SET_RANGE 10, 3345
SAVE_OPT
SET_VEC F:\ESA_software\stimuli, F:\ESA_software\template
SET_BSTR F:\ESA_software\file_demo\top_dut_2
#NEW_PRJ CTM, F:\MyInjection
SET_MODE accumulation
```

Technical features

Main board:

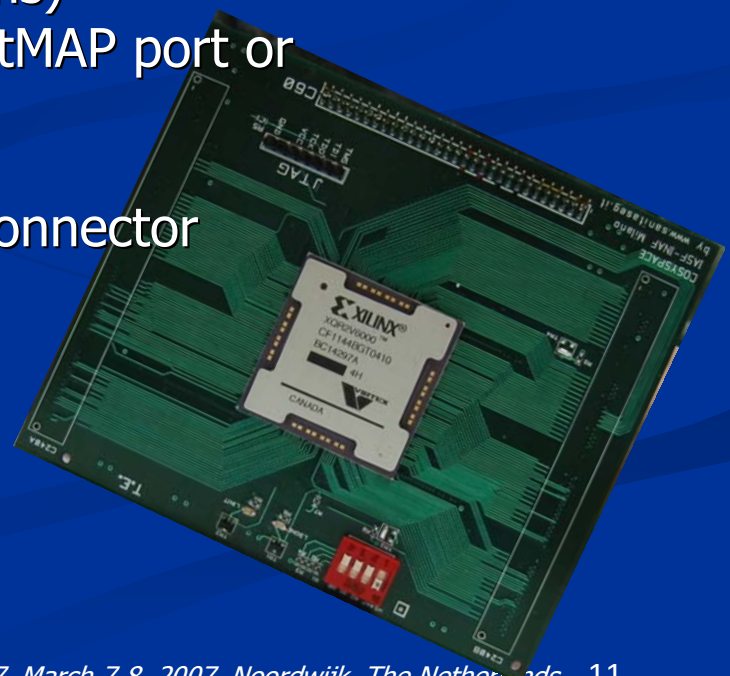
- Xilinx XC2VP20-5 FF896
- USB 2.0 port with dedicated microcontroller
- Up to 128 MByte SDRAM or 256 MByte DDR memory
- 16 MByte Flash
- ISP Flash for FPGA configuration (JTAG configuration also allowed)
- 32 KByte I^2C E^2PROM for the microcontroller configuration
- Temperature control chip
- Two customizable frequencies through independent oscillators
- Two 240 pin connectors plus one 60 pin connector for DUT boards
- P160 connectors for standard expansion boards
- Single power supply (5V/10A)
- On-board voltage regulators for
  - 1.5V/15A
  - 2.5V/15A
  - 3.3V/6A
  - 1.8V/1.5A
- Power LEDs
- FPGA configuration LEDs
- Size: 22 cm x 12 cm



Technical features (cont'd)

Piggy-back DUT board:

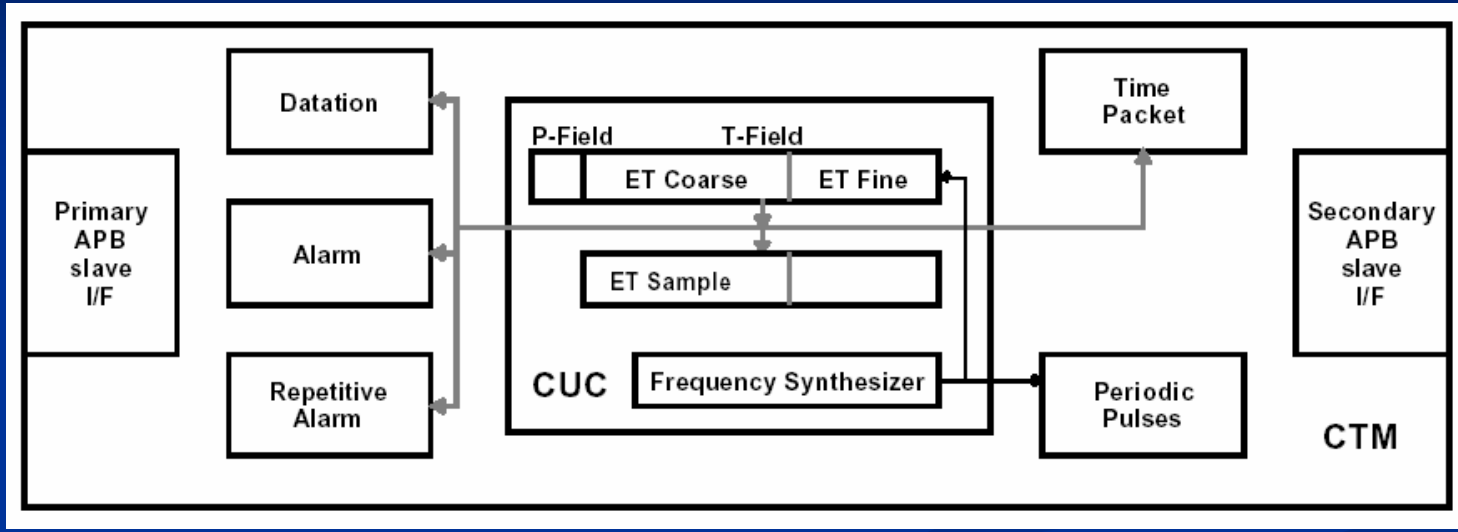
- In principle any Xilinx V2, V2 Pro, V4, and next generation devices can be used (with some limitations) for fault injection test
- Up to 416 DUT pins can be driven by the main board's FPGA (more pin in case of XTMR-ed designs)
- DUT FPGA accessible either through SelectMAP port or JTAG port
- Temperature control chip
- Two 240 pin connectors plus one 60 pin connector
- Powered by the main board
- FPGA configuration LEDs
- Size: 10 cm x 12 cm



Case Study

- Injection into a specific design
- ESA CUC-CTM IP core
  - Provides basic time keeping functions
- Evaluate XTMR version vs unmitigated one
  - Test-benches and XTMR version provided by ESA

CUC-CTM



- Provides alarm services and periodic pulses
- Can be accessed and programmed via AMBA APB slave interface

CUC-CTM Implementation
XQR2V6000

	Plain	XTMR
FF	785 out of 67,584 (1%)	2,361 out of 67,584 (3%)
LUT	1789 out of 67,584 (2%)	7,167 out of 67,584 (10%)
IOB	212 out of 824 (25%)	569 out of 824 (69%)
GCLK	1 out of 16 (12%)	3 out of 16 (18%)

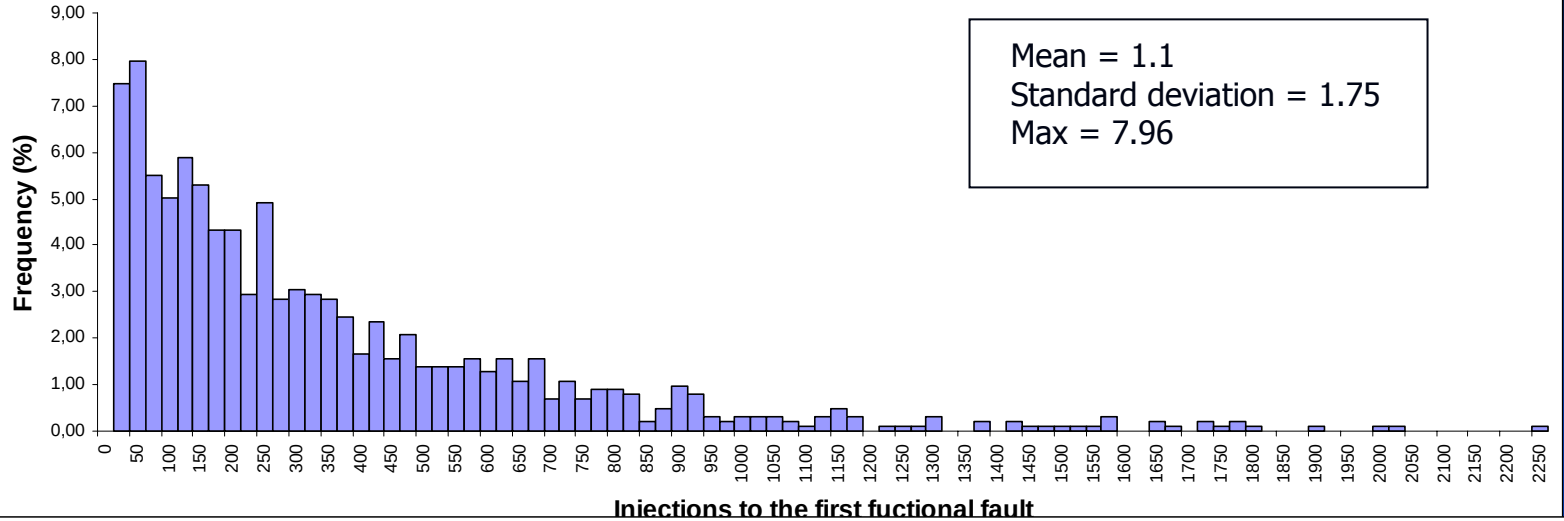
Test Structure

- Device configuration
- Injection by active partial reconfiguration
- Functional test
- Repeat from the injection without restoring the bitstream

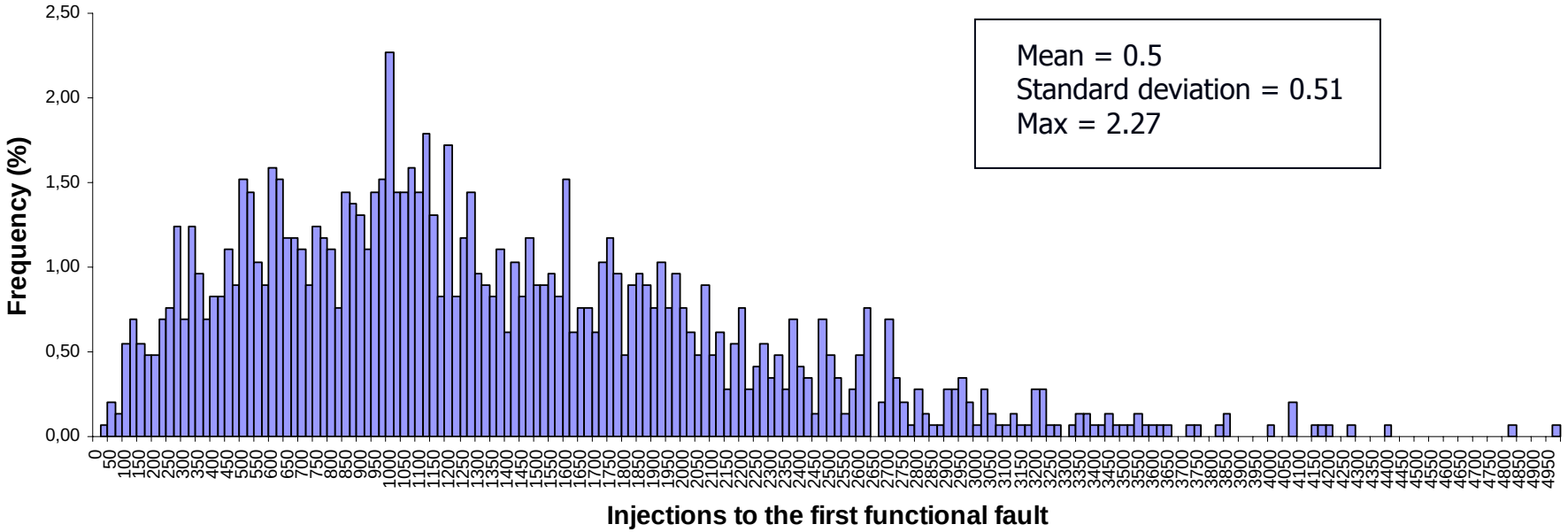
Test info

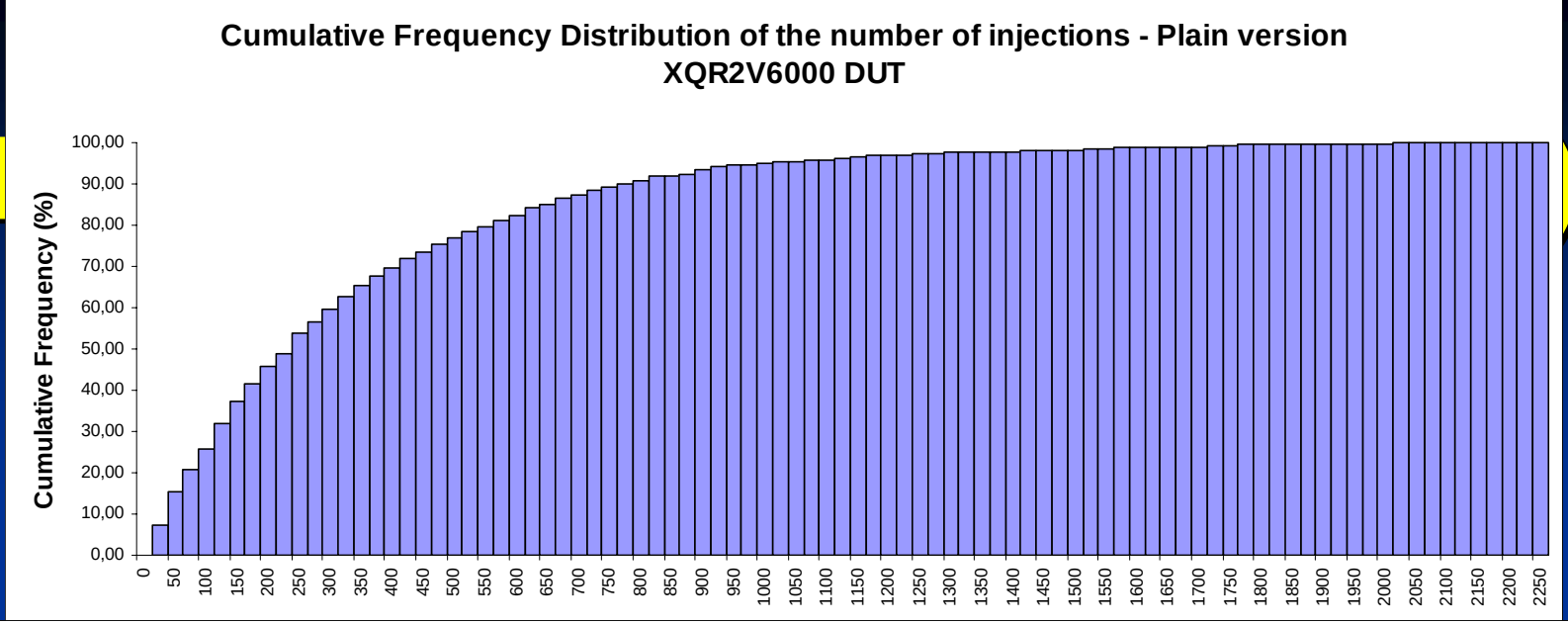
- Injection strategy
  - Single bit flip
  - Fault Accumulation
  - Stop condition → first functional fault
- Campaigns
  - plain/XTMR
- XTMR options
  - The "entire design" is triplicated
  - "Standard" as XMTR types
  - "Triple voted" output
- # run
  - 1000/2500
- # test vectors
  - 26452/26452

Distribution of the number of injections - Plain version
XQR2V6000 DUT



Distribution of the number of injections - XTMR version
XQR2V6000 DUT




Cumulative Frequency Distribution of the number of injections - Plain version
XQR2V6000 DUT
Cumulative Frequency (%)
100,00
90,00
80,00
70,00
60,00
50,00
40,00
30,00
20,00
10,00
0,00
0
50
100
150
200
250
300
350
400
450
500
550
600
650
700
750
800
850
900
950
1000
1050
1100
1150
1200
1250
1300
1350
1400
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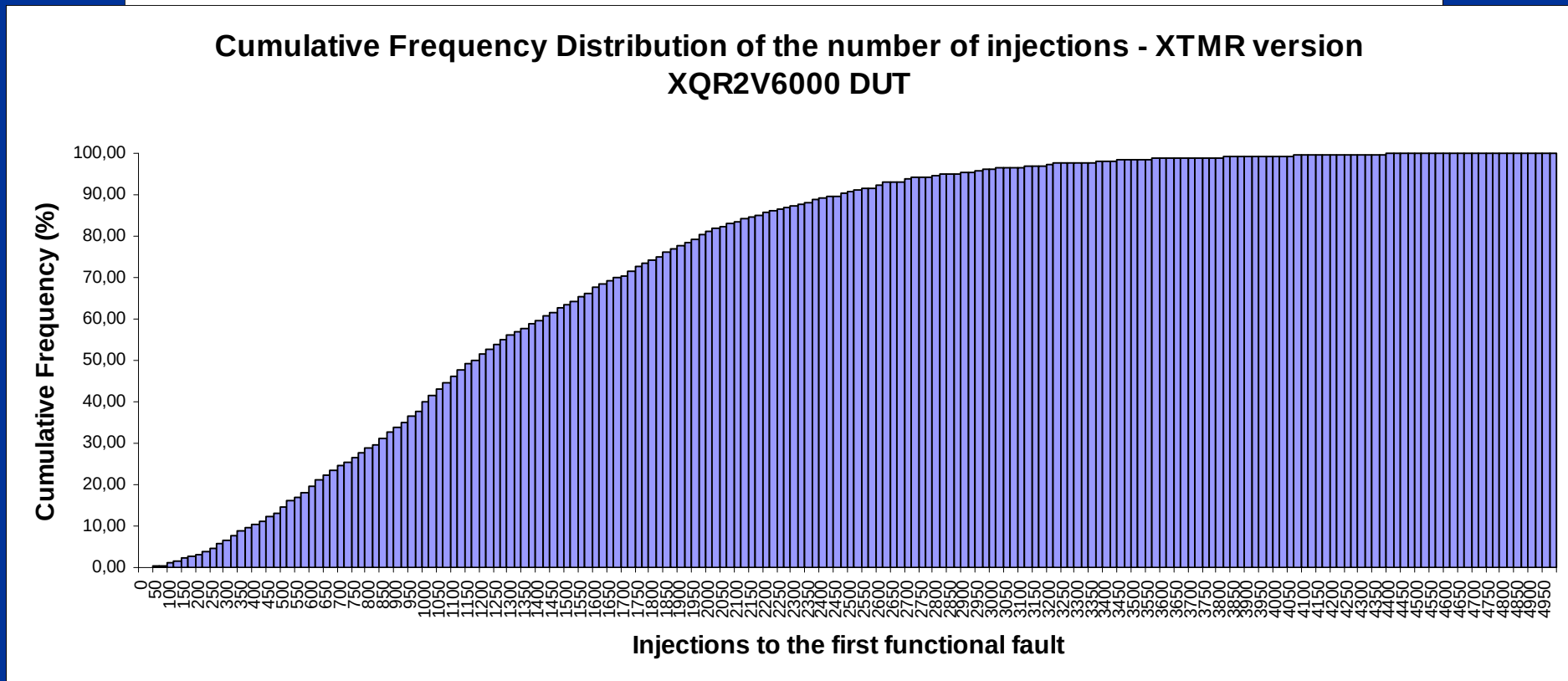
1900
1950
2000
2050
2100
2150
2200
2250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Cumulative Frequency (%)
100,00
90,00
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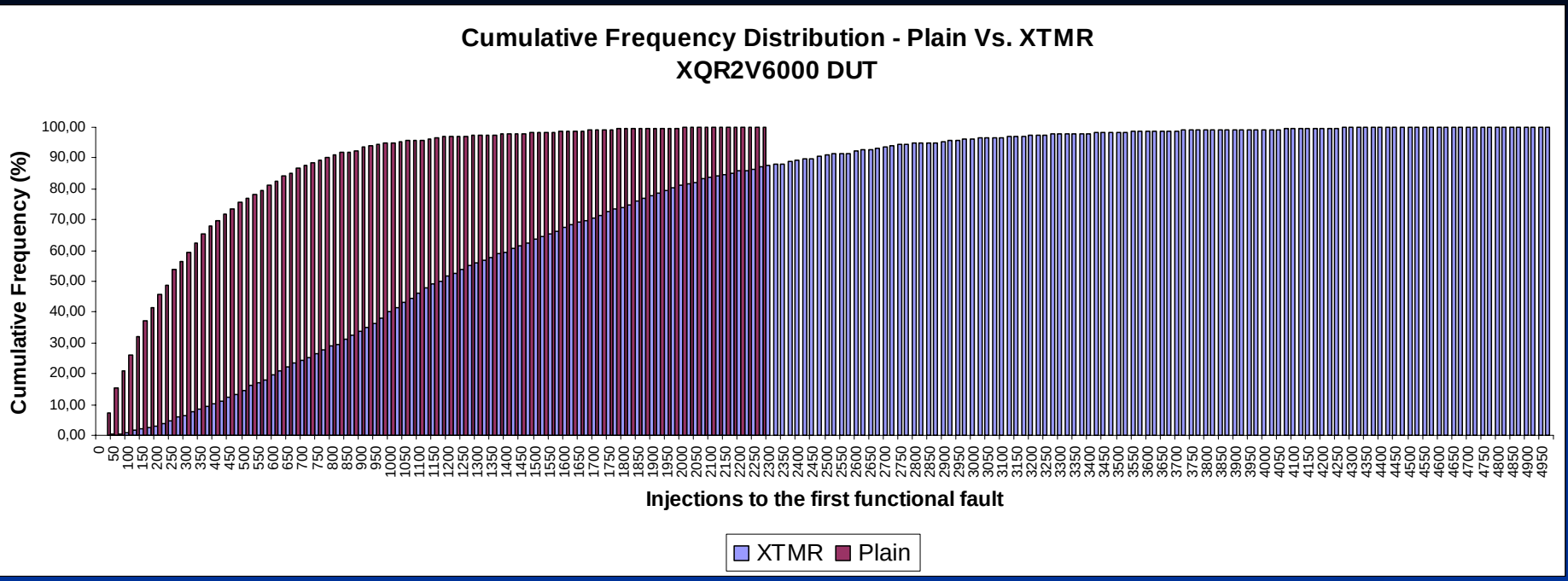
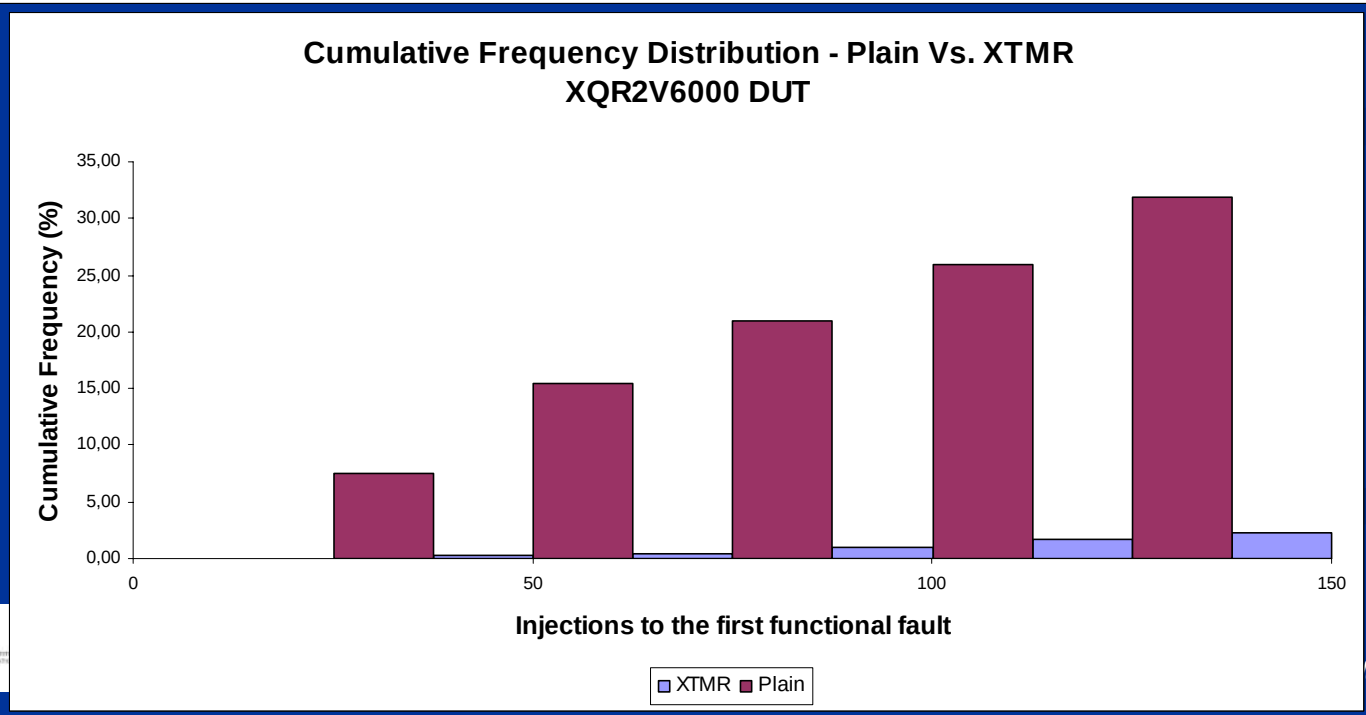
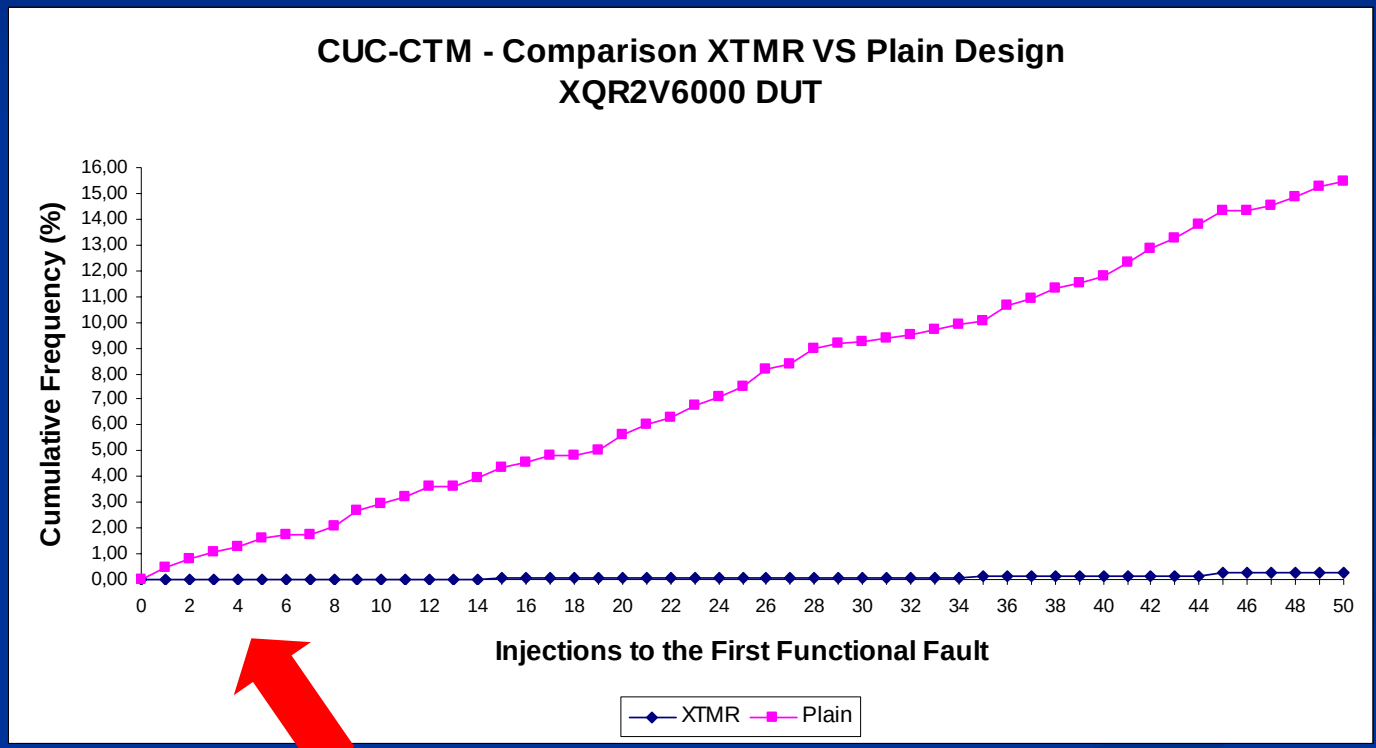
70,00
60,00
50,00
40,00
30,00
20,00
10,00
0,00
Injections to the first functional fault


Cumulative Frequency Distribution - Plain Vs. XTMR
XQR2V6000 DUT
Cumulative Frequency (%)
Injections to the first functional fault
XTMR
Plain


Cumulative Frequency Distribution - Plain Vs. XTMR
XQR2V6000 DUT
Cumulative Frequency (%)
Injections to the first functional fault
XTMR
Plain

Plain VS. XTMR



Conclusions

- Encouraging preliminary results
- Extension of the actual contract for FLIPPER upgrade
- Likely usage of FLIPPER in a proton radiation testing

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http://cosy.iasf-milano.inaf.it/flipper_index.htm