FLIPPER

SEU Fault Injection in Xilinx FPGAs

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Outline

- Overview
- Basic principle and main features
- Case study
- Preliminary results
- Conclusions
FLIPPER what is it?

FLIPPER is a flexible XC2VP20-based board conceived as a powerful hardware platform for the following main application:

- SEU emulation by fault injection in Virtex II devices (patent pending)

FLIPPER can be used in more general ways:

- radiation ground testing
- test equipment
- digital I/O board
- general purpose Virtex2 board
- ...

M. Alderighi, MPD07, March 7-8, 2007, Noordwijk, The Netherlands
Why FLI PPER?

- SEUs are of utmost concern for Xilinx devices as functionalities are sensitive to unintended change in configuration memory.

- **Fault Injection** tools able to adequately address “reachable” radiation sensitive parts, are useful.

- Our objective is providing one tool able to:
  - inject SEUs into the configuration memory
  - manage a high number of I/O pins
  - exercise a DUT device performing on board comparison of test results
**FLIPPER basic principle**

- SEU injection by *active partial reconfiguration*
- SEU injection by configuration adopted in an earlier prototype for Virtex I*
- Close approach, yet with different purposes, used by FT UNSHADES
- Reported approach by the literature in the FI field (e.g. R. Leveugle)

FLIPPER what’s for

- Analyze SEU effects in designs implemented in Xilinx FPGAs
- Study SEU effects in Xilinx FPGA reconfiguration logic
  - by means of a write operation into configuration logic registers
- Evaluate/compare mitigated designs in one/selected device(s)
FLIPPER features

- SEU emulator comprising hardware, firmware & software
- Fault injection based on frame modification and active partial re-configuration
  - Verified through JTAG & Impact verify
- Single bit and multiple bit upsets
- Test vectors and gold vectors imported from ModelSim simulation
- Test vectors up to 150 bit wide and gold vectors up to 120 bit wide
- $\approx 26000$ test vectors @10MHz $\rightarrow \approx 11$ injection/s with max. I/O port width
FLIPPER features (cont’d)

- After each injection the DUT is exercised for the whole set of test vectors
- Test/gold vectors comparison performed on board. In case of mismatch, a fault packet is sent to the PC containing:
  - # of the current injected fault
  - # of the current test vector
  - Ex-OR between the current DUT outputs and the expected (gold) values
- DUT FPGA’s pin wired together in triplets on the DUT board to implement XTMR-ed designs
- XQR2V6000 used as DUT for ESA contract
- Test execution either via GUI interface or in batch mode
- Injection mode and options selectable via software
**FLIPPER GUI Interface**

**TEST MODE**
- **sequential**
  - bit-flip location generated sequentially within the injection range
- **original frame restored after functional test**
- **fault accumulation**
  - random generation of fault locations
  - faulty frames persist
  - accumulate and clean up
  - original frames are restored after a number (user selectable) number of injections

**DUT CLOCK RATE**
- **5 MHz**
- **10 MHz**
- **50 MHz**
- **100 MHz**

**STOP TEST CONDITION**
- **first functional fault/configuration failure**
- **# bit flip**
- **none**

**ADDRESS RANGE**
Defines the area in which faults are injected (device dependent)

**Menu Items**
- **OPEN_PRJ demo**
- **ADHOC_TEST**
- **ADHOC_FILE**
- **SET_MASK_HH**
- **SET_RATE**
- **SET_RANGE**
- **SAVE_OPT**
- **SET_VEC**
- **SET_BSTR**
- **#NEW_PRJ**
- **SET_MODE accumulation**
Technical features

Main board:
- Xilinx XC2VP20-5 FF896
- USB 2.0 port with dedicated microcontroller
- Up to 128 MByte SDRAM or 256 MByte DDR memory
- 16 MByte Flash
- ISP Flash for FPGA configuration (JTAG configuration also allowed)
- 32 KByte I²C E²PROM for the microcontroller configuration
- Temperature control chip
- Two customizable frequencies through independent oscillators
- Two 240 pin connectors plus one 60 pin connector for DUT boards
- P160 connectors for standard expansion boards
- Single power supply (5V/10A)
- On-board voltage regulators for
  - 1.5V/15A
  - 2.5V/15A
  - 3.3V/6A
  - 1.8V/1.5A
- Power LEDs
- FPGA configuration LEDs
- Size: 22 cm x 12 cm
Technical features (cont’d)

Piggy-back DUT board:

- In principle any Xilinx V2, V2 Pro, V4, and next generation devices can be used (with some limitations) for fault injection test
- Up to 416 DUT pins can be driven by the main board’s FPGA (more pin in case of XTMR-ed designs)
- DUT FPGA accessible either through SelectMAP port or JTAG port
- Temperature control chip
- Two 240 pin connectors plus one 60 pin connector
- Powered by the main board
- FPGA configuration LEDs
- Size: 10 cm x 12 cm
Case Study

- Injection into a specific design
- ESA CUC-CTM IP core
  - Provides basic time keeping functions
- Evaluate XTMR version vs unmitigated one
  - Test-benches and XTMR version provided by ESA
- Provides alarm services and periodic pulses
- Can be accessed and programmed via AMBA APB slave interface
# CUC-CTM Implementation

## XQR2V6000

<table>
<thead>
<tr>
<th></th>
<th>Plain</th>
<th>XTMR</th>
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</thead>
<tbody>
<tr>
<td>FF</td>
<td>785 out of 67,584 (1%)</td>
<td>2,361 out of 67,584 (3%)</td>
</tr>
<tr>
<td>LUT</td>
<td>1789 out of 67,584 (2%)</td>
<td>7,167 out of 67,584 (10%)</td>
</tr>
<tr>
<td>IOB</td>
<td>212 out of 824 (25%)</td>
<td>569 out of 824 (69%)</td>
</tr>
<tr>
<td>GCLK</td>
<td>1 out of 16 (12%)</td>
<td>3 out of 16 (18%)</td>
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Test Structure

- Device configuration
- Injection by active partial reconfiguration
- Functional test
- Repeat from the injection without restoring the bitstream
Test info

- Injection strategy
  - Single bit flip
  - Fault Accumulation
  - Stop condition → first functional fault
- Campaigns
  - plain/XTMR
- XTMR options
  - The “entire design” is triplicated
  - “Standard” as XMTR types
  - “Triple voted” output
- # run
  - 1000/2500
- # test vectors
  - 26452/26452
Preliminary results

**Distribution of the number of injections - Plain version**

**XQR2V6000 DUT**

- Mean = 1.1
- Standard deviation = 1.75
- Max = 7.96

**Distribution of the number of injections - XTMR version**

**XQR2V6000 DUT**

- Mean = 0.5
- Standard deviation = 0.51
- Max = 2.27
Cumulative Frequency Distribution of the number of injections - Plain version
XQR2V6000 DUT

Cumulative Frequency Distribution of the number of injections - XTMR version
XQR2V6000 DUT

Injections to the first functional fault
Injections to the first functional fault

Cumulative Frequency Distribution - Plain Vs. XTMR
XQR2V6000 DUT

Cumulative Frequency (%)
Plain VS. XTMR

CUC-CTM - Comparison XTMR VS Plain Design
XQR2V6000 DUT

Cumulative Frequency (%)

Injections to the First Functional Fault

XTMR
Plain

scrubbing
Conclusions

- Encouraging preliminary results
- Extension of the actual contract for FLIPPER upgrade
- Likely usage of FLIPPER in a proton radiation testing
END

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http://cosy.iasf-milano.inaf.it/flipper_index.htm