SpaceWire Router ASIC

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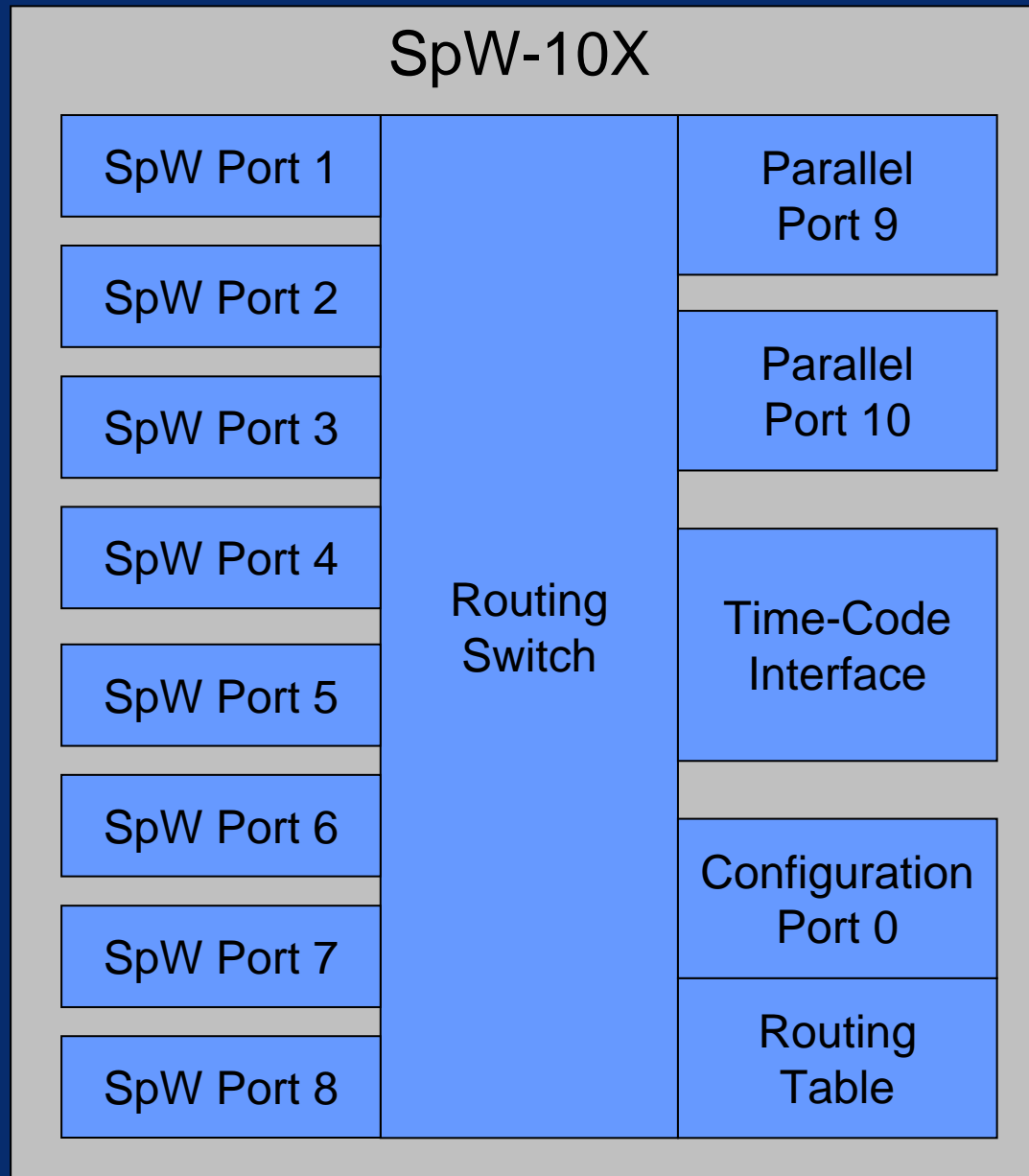
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ESA, ESTEC

SpW-10X Architecture

SpW-10X

SpW Port 1		Parallel Port 9
SpW Port 2		Parallel Port 10
SpW Port 3	Routing Switch	
SpW Port 4		Time-Code Interface
SpW Port 5		
SpW Port 6		
SpW Port 7		Configuration Port 0
SpW Port 8		Routing Table

SpaceWire Ports

- SpaceWire compliant
- Data Signalling Rate
  - 200 Mbits/s maximum
  - Selectable 2 – 200 Mbits/s
- Each SpaceWire port can run at a different speed
- LVDS drivers and receivers on chip
  - Avoids size, mass, cost of external LVDS chips
- Receiver auto-start mode
- Power control
  - Each SpaceWire port can be completely disabled
    - including clock tree
  - LVDS can be tri-stated with auto-enable
  - Links can be held disconnected until there is data to send

Parallel Ports

- Parallel ports to support connection to
  - Processors
  - Simple logic
- 8-bit data + control/data flag
- FIFO type interface
- Operate at speed of SpaceWire links
 - i.e. 200 Mbits/s

Routing Switch

- Switches packet being received to
- Appropriate output port
- SpaceWire and Parallel ports treated the same
- Non-blocking
  - If the required output port is not being used already
  - Guaranteed to be able to forward packet
  - Rapid packet switching times
  - Low latency
- Worm-hole routing

SpaceWire Packets

- **Packet Format**

  ← `<DESTINATION> <CARGO> <END OF PACKET MARKER>`

- **Destination**

  – represents either path to, or identity of destination node

- **Cargo**

  – data or message to be transferred from source to destination

- **End of Packet Marker**

  – indicates end of packet

Wormhole Routing
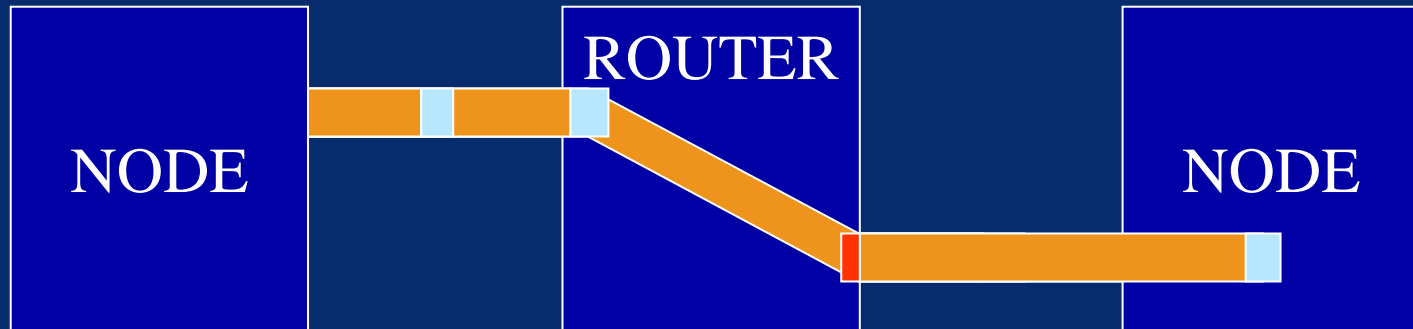
Node sends out packet
Router receives header and checks requested output port
Router connects input to output and packet flows through router
When EOP marker seen, router terminates connection
and frees output port

Wormhole Routing

- **Advantages**
  - No packet buffering
  - Little buffer memory
  - Can support packets of arbitrary size
  - Rapid switching
- **Disadvantages**
  - If output port not ready
  - Then have to wait
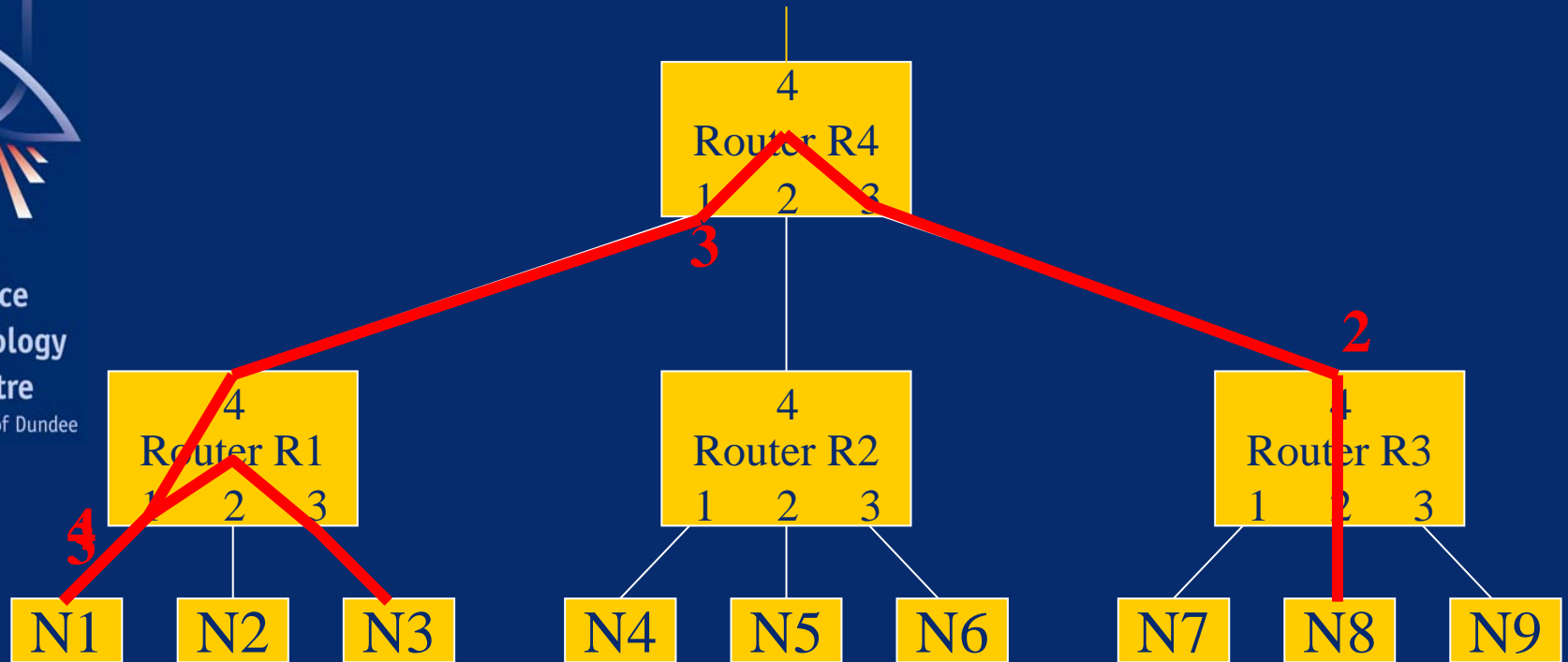 - Blocks all links being used for the waiting packet

Routing Table

	Address	Port 0	Port 1	Port 2	Port 3	Port 4
Configuration	0	1	0	0	0	0
Path Addressing	1	0	1	0	0	0
	2	0	0	1	0	0
	...					
Logical Addressing	32	0	1	0	0	0
	33	0	0	1	0	0
	34	0	0	0	0	1
	...					
Reserved	255	0	0	0	0	0

Path Addressing

- destination is specified as router output port number
- node 1 to node 3   <3><cargo><EOP>
- node 1 to node 8   <4><3><2><cargo><EOP>

Logical Addressing

43	1
163	3

4
Router R4
1   2   3

43	3
163	4

43	4
163	2

4
Router R1
1   2   3

4
Router R2
1   2   3

4
Router R3
1   2   3

N1	N2	N3	N4	N5	N6	N7	N8	N9
LA 41	LA 42	LA 43	LA 152	LA130	LA 131	LA 175	LA 163	LA 182
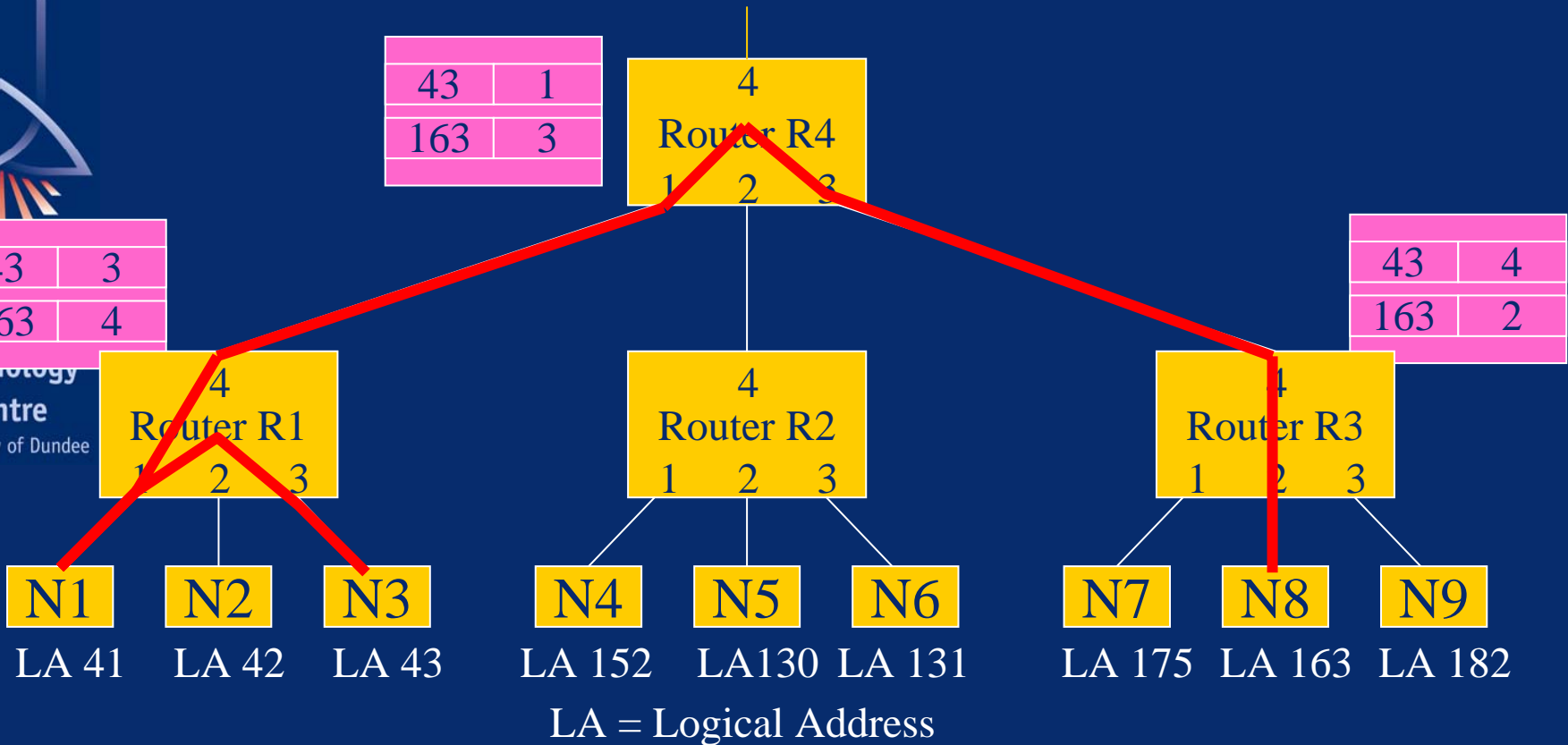
LA = Logical Address

- each destination has a unique logical address
- each router has a list of which port(s) to send data out for each possible destination
- node 1 to node with logical address 43   <43><cargo><EOP>
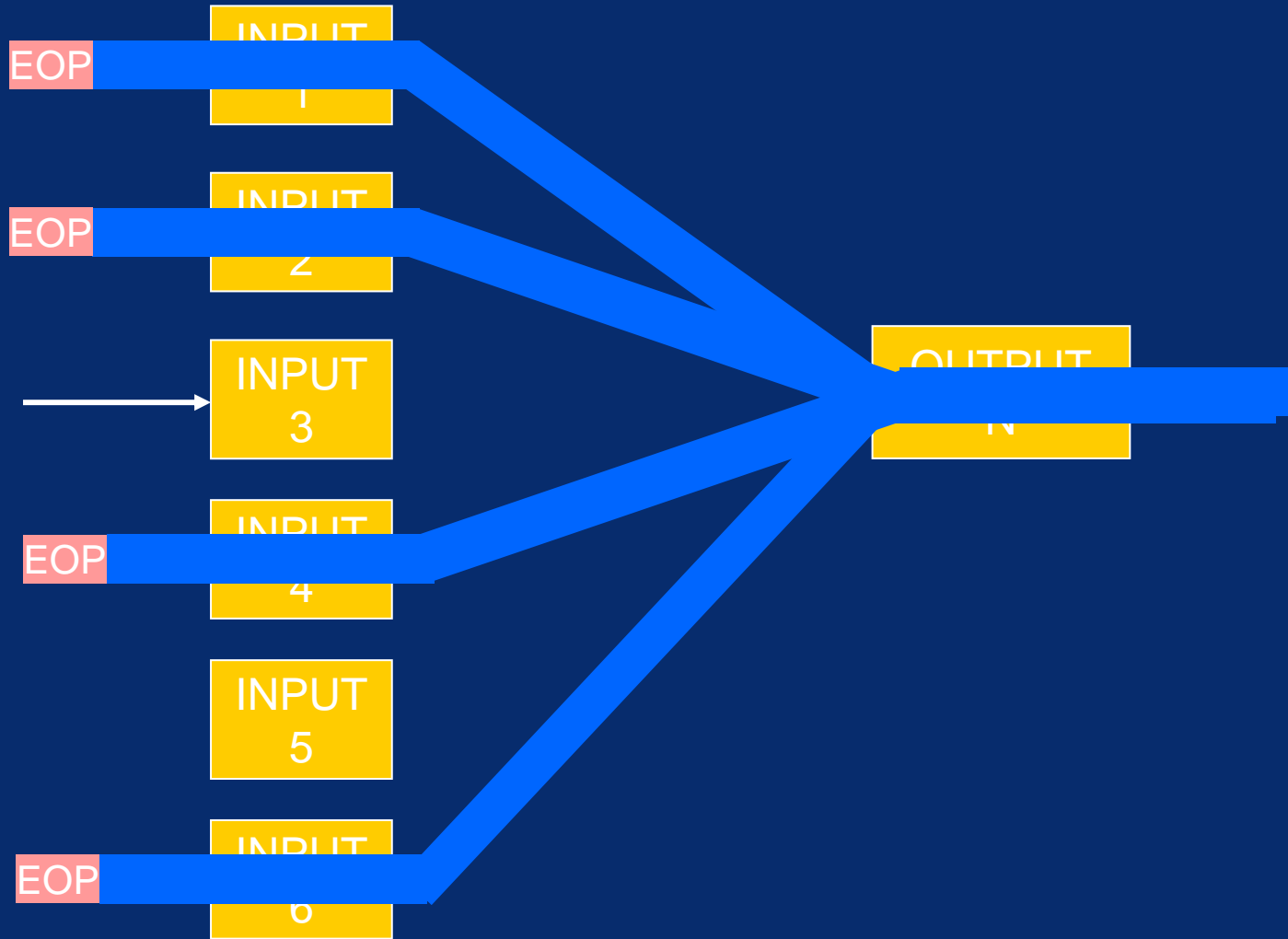- node 1 to node with logical address 163 <163><cargo><EOP>

Priority

- **Arbitration in Router**
  - Fair arbitration
  - Priority based
- **SpaceWire header contains address only**
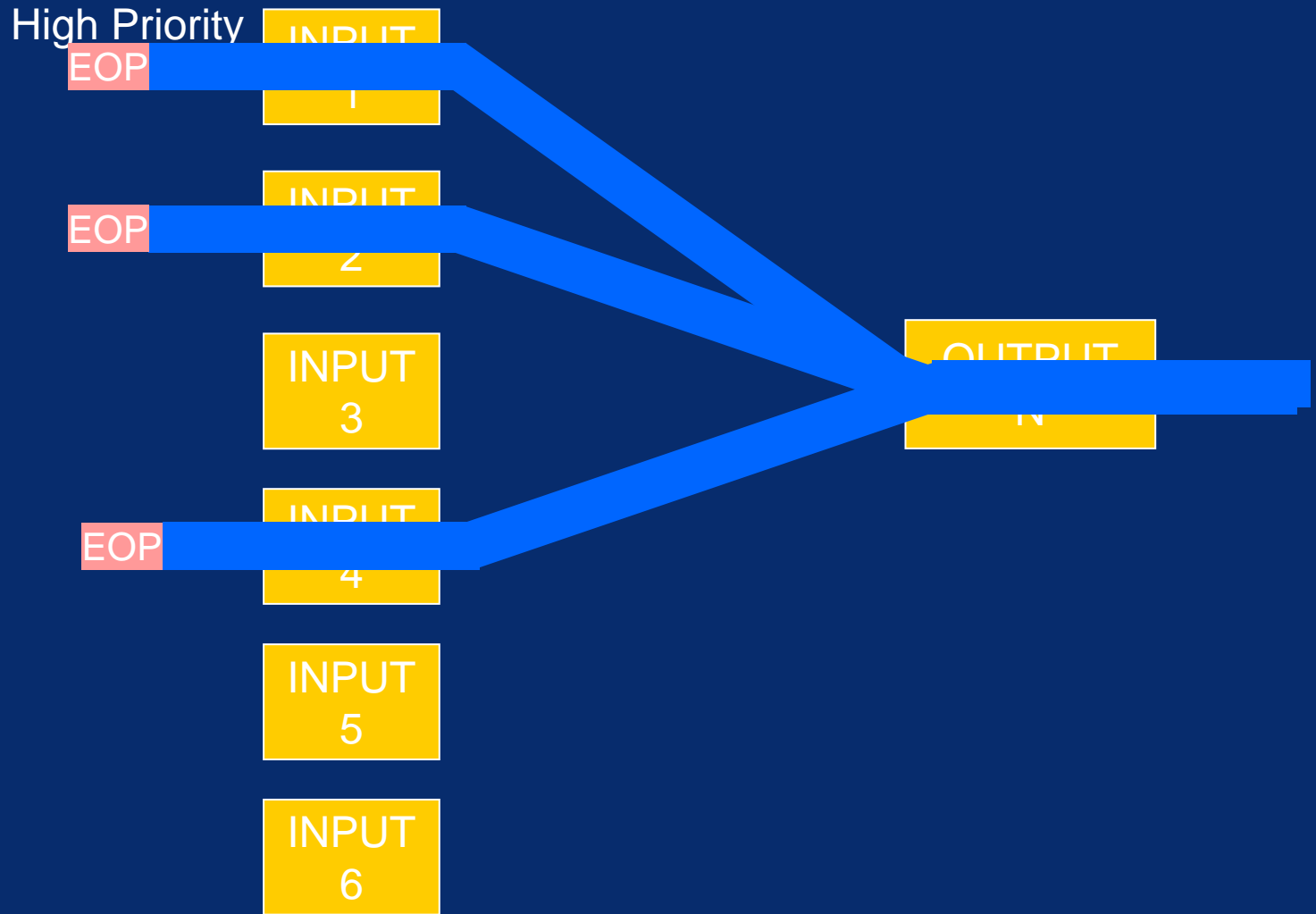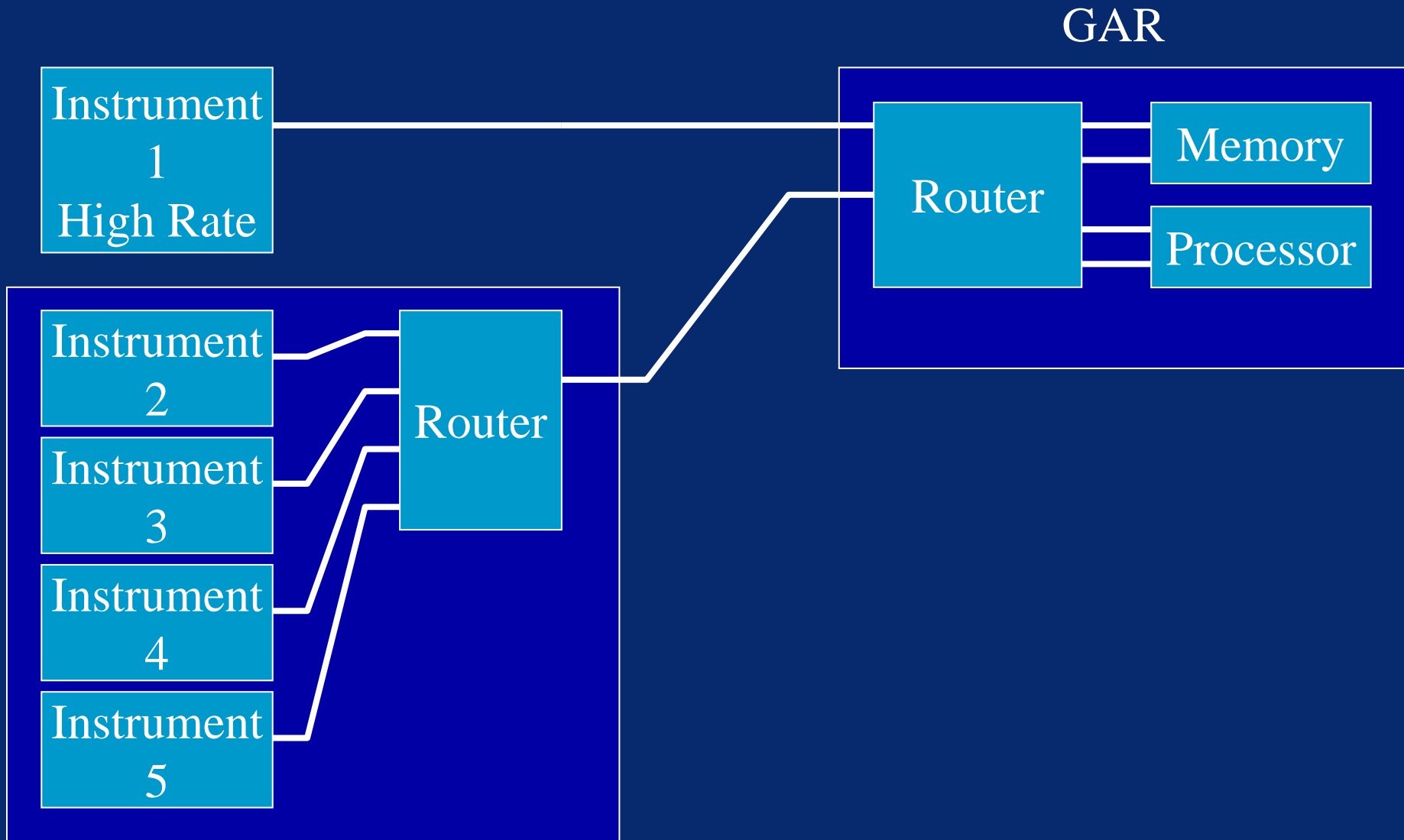- **Assign priority to logical addresses**

Arbitration

Priority

	Address	Priority	Port 0	Port 1	Port 2	Port 3	Port 4
Configuration	0	0	1	0	0	0	0
Path Addressing	1	0	0	1	0	0	0
	2	0	0	0	1	0	0
	…						
Logical Addressing	32	0	0	1	0	0	0
	33	1	0	1	0	0	0
	34	0	0	0	0	0	1
	…						
Reserved	255	0	0	0	0	0	0

Arbitration with Priority

High Priority

EOP INPUT 1

EOP INPUT 2

INPUT 3

EOP INPUT 4

INPUT 5

INPUT 6

OUTPUT N

15

Group Adaptive Routing

GAR

Instrument 1 High Rate

Instrument 2

Instrument 3

Instrument 4

Instrument 5

Router

Router

Memory

Processor

Group Adaptive Routing

	Address	Priority	Port 0	Port 1	Port 2	Port 3	Port 4
Configuration	0	0	1	0	0	0	0
Path Addressing	1	0	0	1	0	0	0
	2	0	0	0	1	0	0
	...						
Logical Addressing	32	0	0	1	1	0	0
	33	1	0	1	1	0	0
	34	0	0	0	0	1	1
	...						
Reserved	255	0	0	0	0	0	0

Configuration Port

- **Used to configure router device**
  - Routing tables
  - Link speeds
  - Power states
  - Etc
- **Used to read router status**
- **RMAP Remote Memory Access Protocol**
- **Used for reading and writing configuration port registers**
- **Router can be configured over**
  - Any SpaceWire port
  - Any Parallel port

Time-Code Port

- Sends and receives time-codes

- Tick-in
  - Internal time-counter incremented and time-code sent
  - Or
  - Value on the time-code input port is sent as a time-code

- Tick-out
  - Indicates valid time-code received
  - Value of time-code on time-code output port

Status/Configuration Interface

- On power up holds some configuration information
- Thereafter provides status according to four address lines
- 0-10: Port status
  - 0: Configuration port
  - 1-8: SpaceWire port
  - 9-10: Parallel port
- 11: Network discovery
  - Return port
  - This is a router
- 12: Router control
  - Enables and timeouts
- 13: Error active
- 14: Time-code
- 15: General purpose
  - Contents of general purpose register
  - Settable by configuration command

Router ASIC Performance

- ## ASIC
  - Implementation in Atmel MH1RT gate array
  - Max gate count 519 kgates (typical)
  - 0.35 µm CMOS process

- ## Radiation tolerance
  - 100 krad
  - SEU free cells to 100 MeV
  - Used for all critical memory cells
  - Latch-up immunity to 80 MeV

- ## Performance
  - SpaceWire interface baud-rate 200 Mbits/s
  - LVDS drivers/receivers integrated on-chip

- ## Power
  - 4 W power with all links at maximum data rate
  - Single 3.3 V supply voltage

- ## Package
 - 196 pin ceramic Quad Flat Pack 25 mil pin spacing

ESA SpaceWire Router Performance

**SpaceWire Router Latency and Jitter Measurements (Bit rate = 200Mbits/s)**

Description	Symbol	Value	Units
Switching Latency	T_{SWITCH}	133.3	ns, max
Router Latency – SpaceWire to SpaceWire port	T_{SSDATA}	546.6	ns, max
Router Latency – SpaceWire to External port	T_{SEDATA}	316.6	ns, max
Router Latency – External to SpaceWire port	T_{ESDATA}	363.3	ns, max
Router Latency – External to External port	T_{EEDATA}	166.6	ns, max
Time-code Latency – SpaceWire to SpaceWire port	T_{SSTC}	409.3	ns, max
Time-code Latency – SpaceWire to External port	T_{SETC}	316.6	ns, max
Time-code Latency – External to SpaceWire port	T_{ESTC}	359.9	ns, max
Time-code Jitter	T_{TCJIT}	116.6	ns, max

[1] Note all figures are worst case

Applications – Standalone Router
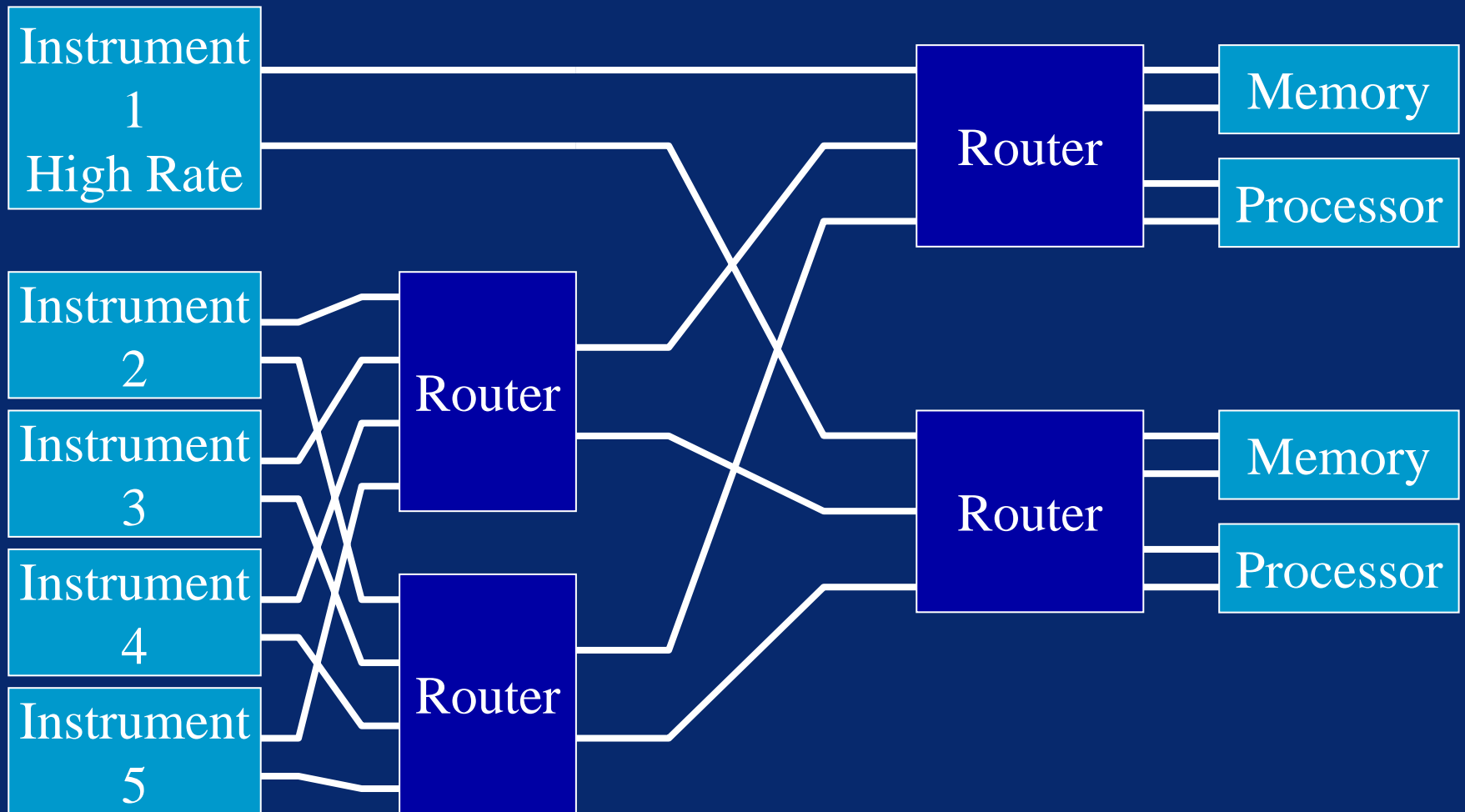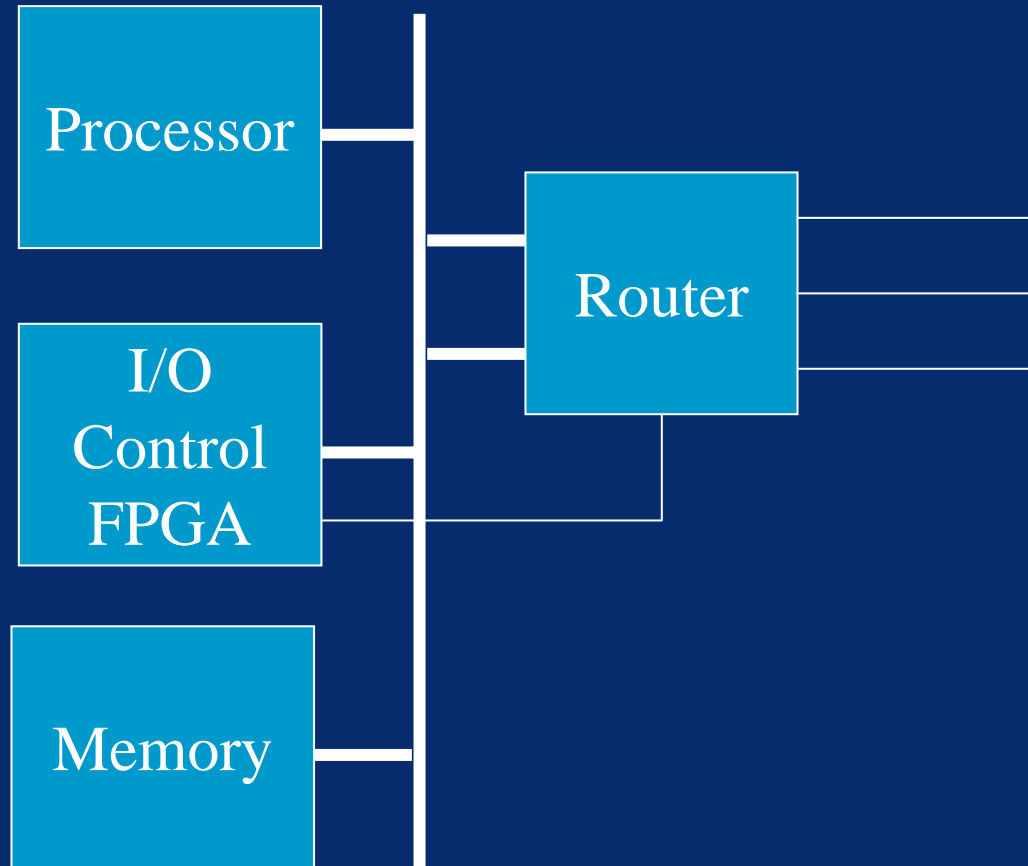
Applications – Embedded Router

Applications – Node Interface

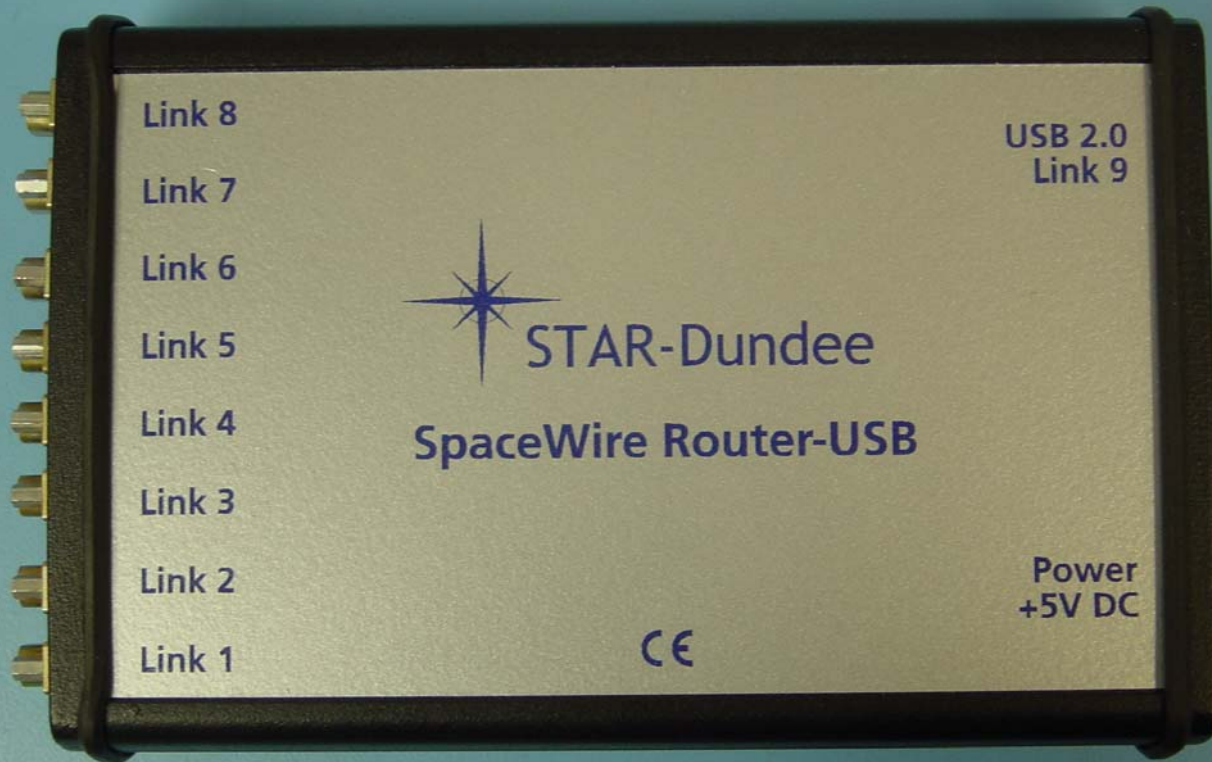Instrument 1 High Rate — Instrument Control FPGA — Router
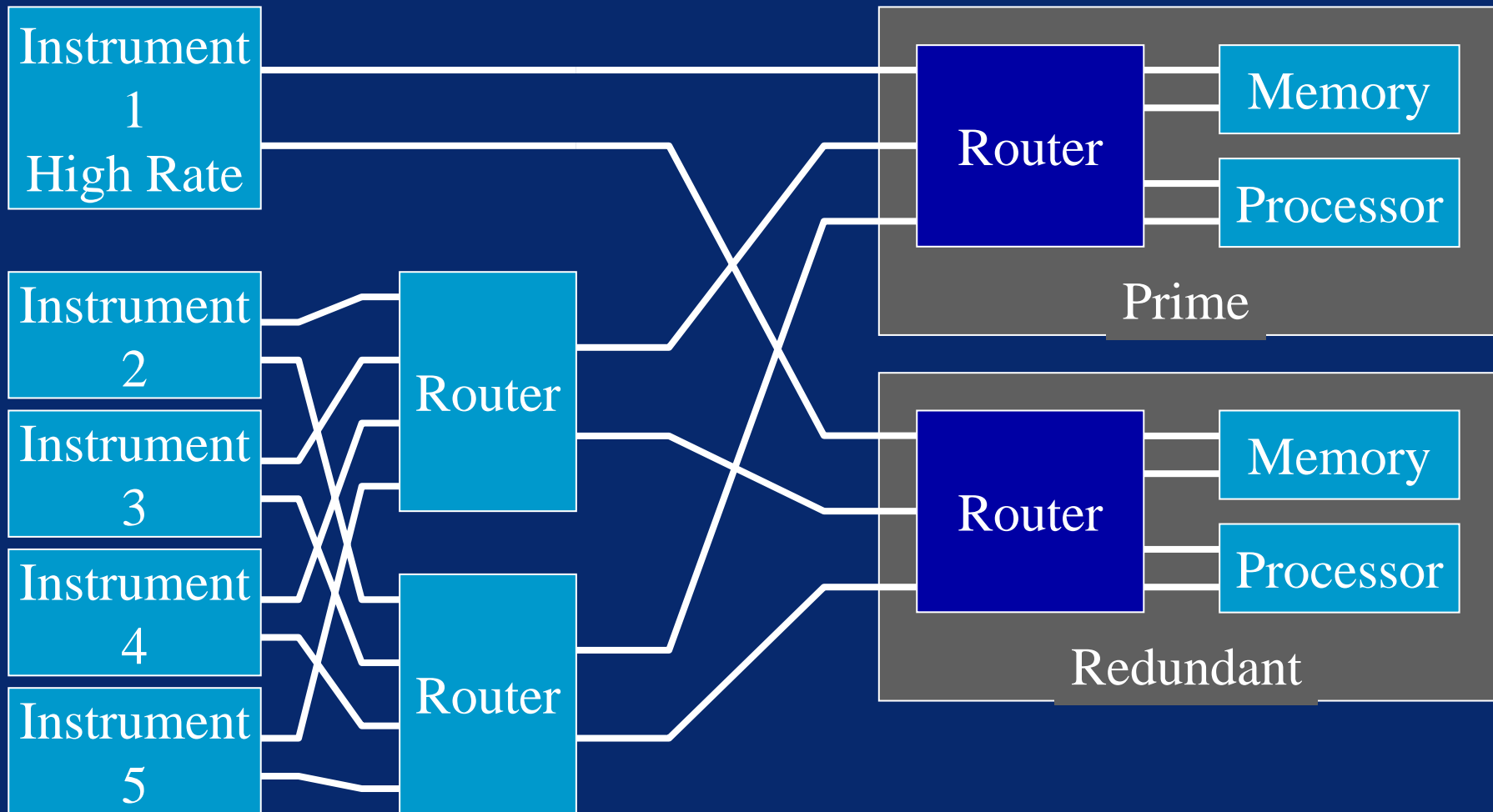
Applications – Node Interface

Applications – Node Interface

Router Prototype Implementations

Router Prototype Implementations

Router Prototype Implementations

Team

- **University of Dundee**
  - Design and Testing
- **Austrian Aerospace**
  - Independent VHDL Test Bench
  - Transfer to ASIC technology
- **Astrium GmbH**
  - Functional Testing
- **Atmel**
  - ASIC Manufacture
- **STAR-Dundee**
  - Support and Test Equipment

Conclusions

- ESA router has extensive capabilities
- Suitable for a wide range of applications
- Independently tested
- Extensively validated
- Full range of support services available