The SpaceWire Remote Terminal Controller

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The SpaceWire Remote Terminal Controller (SpW-RTC)

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SpW-RTC Overview

- Bridge between SpaceWire Network and I/O such as ADCs, DACs, FIFOs and CAN bus sensors
- Developed by Saab Space as prime contractor, with Gaisler Research as subcontractor
- Atmel ATC18RHA radiation hard 180 nm standard cell ASIC technology
- 970 kGate
- MCGA349 package
- Prototypes available 2007 Q4
- Flight parts 2008
SpW-RTC Architecture

![SpW-RTC Architecture Diagram]
Leon2-FT Processor in SpW-RTC

• LEON2-FT Fault Tolerant SPARC V8 processor, 34 MIPS@50 MHz
• Version 1.0.9.16.1, same as planned to be used for Atmel’s upcoming AT697F processor
• IEEE-754 Floating Point Unit
• 4 kbytes direct mapped instruction cache
• 4 kbytes direct mapped data cache
• Debug Support Unit (DSU) with 512 trace lines
SpW-RTC Interfaces (1/2)

- Two ECSS-E-50-12A SpaceWire Interfaces capable up to 200 MHz/160 Mbps, based on the UoD SpaceWire Codec IP core.
- Hardware support for Remote Memory Access Protocol (RMAP) compliant with ECSS-E-50-11 Draft F
- CAN bus controller based on the ESA HurriCANe CAN controller, supporting redundant CAN buses up to 1 Mbps
- Two UART serial links
- Debug Support Unit with Debug Link
SpW-RTC Interfaces (2/2)

- 40 bits General Purpose Input Output, supporting input, output and pulse generation
- 8-bit/16-bit interface to external FIFO
- Interface to external 8-bit/16-bit ADC
- Interface to external 8-bit/16-bit DAC
- Five 32-bit timers
- LEON2-FT memory controller for SRAM and PROM/EEPROM with EDAC protection
## SpW-RTC Evolution

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<tr>
<th>Item</th>
<th>Requirement in ITT</th>
<th>SpW-RTC implementation</th>
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<tbody>
<tr>
<td>Processor</td>
<td>Microcontroller</td>
<td>Leon2-FT SPARC V8 32-bit processor</td>
</tr>
<tr>
<td>Floating Point</td>
<td>-</td>
<td>Meiko IEEE-754 FPU</td>
</tr>
<tr>
<td>Performance</td>
<td>- (a 803X microcontroller has 2-3 integer MIPS)</td>
<td>34 Dhrystone MIPS, 2 MFlops @ 50 MHz</td>
</tr>
<tr>
<td>On-chip memory</td>
<td>32 kbytes</td>
<td>64 kbytes</td>
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<tr>
<td>SpaceWire Links</td>
<td>Two ECSS-E-50-12A SpaceWire 200 MHz links</td>
<td>Two ECSS-E-50-12A SpaceWire 200 MHz links</td>
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<tr>
<td>Remote Memory Access Protocol</td>
<td>-</td>
<td>Hardware support for RMAP ECSS-E-50-11 draft F</td>
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SpW-RTC FPGA Validation Board

- Xilinx Virtex-2 FPGA with SpW-RTC design
- 16 Mbytes Flash PROM
- 4 Mbytes SRAM
- 2 SpaceWire links, redundant CAN bus, 2 UARTs
- 24-bit GPIO and FIFO interfaces
- ADC and 4 channel multiplexer
- DAC
- 30 MHz operating frequency, 100 MHz SpaceWire