The SpaceWire Remote Terminal Controller

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GAISLER RESEARCH

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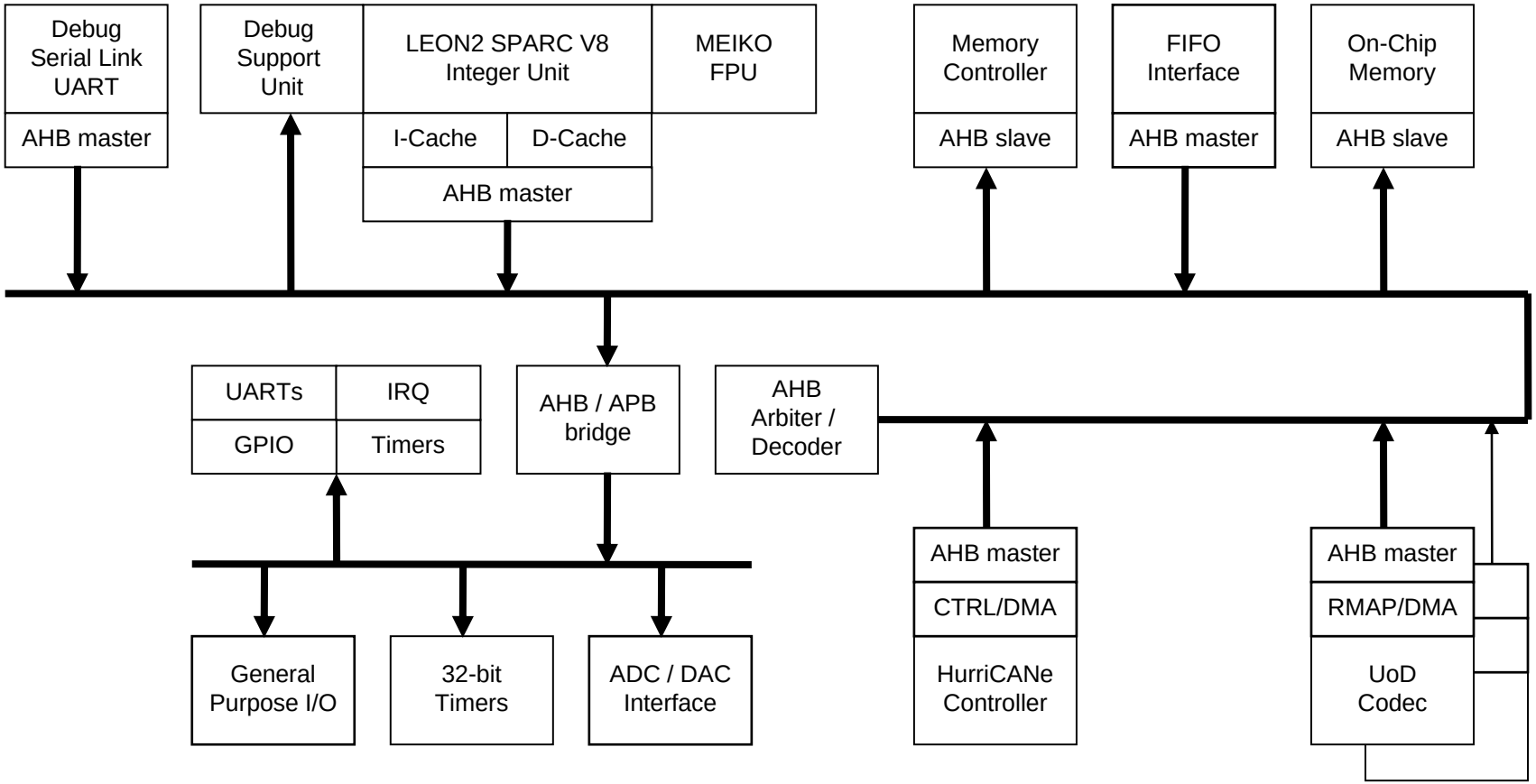
The SpaceWire Remote Terminal Controller (SpW-RTC)

- SpW-RTC Overview
- SpW-RTC Architecture
- Leon2-FT Processor in SpW-RTC
- SpW-RTC Interfaces
- SpW-RTC Evolution
- SpW-RTC FPGA Validation Board

SpW-RTC Overview

- Bridge between SpaceWire Network and I/O such as ADCs, DACs, FIFOs and CAN bus sensors
- Developed by Saab Space as prime contractor, with Gaisler Research as subcontractor
- Atmel ATC18RHA radiation hard 180 nm standard cell ASIC technology
- 970 kGate
- MCGA349 package
- Prototypes available 2007 Q4
- Flight parts 2008

SpW-RTC Architecture



Leon2-FT Processor in SpW-RTC

- LEON2-FT Fault Tolerant SPARC V8 processor, 34 MIPS@50 MHz
- Version 1.0.9.16.1, same as planned to be used for Atmel's upcomig AT697F processor
- IEEE-754 Floating Point Unit
- 4 kbytes direct mapped instruction cache
- 4 kbytes direct mapped data cache
- Debug Support Unit (DSU) with 512 trace lines

SpW-RTC Interfaces (1/2)

- Two ECSS-E-50-12A SpaceWire Interfaces capable up to 200 MHz/160 Mbps, based on the UoD SpaceWire Codec IP core.
- Hardware support for Remote Memory Access Protocol (RMAP) compliant with ECSS-E-50-11 Draft F
- CAN bus controller based on the ESA HurriCANe CAN controller, supporting redundant CAN buses up to 1 Mbps
- Two UART serial links
- Debug Support Unit with Debug Link

SpW-RTC Interfaces (2/2)

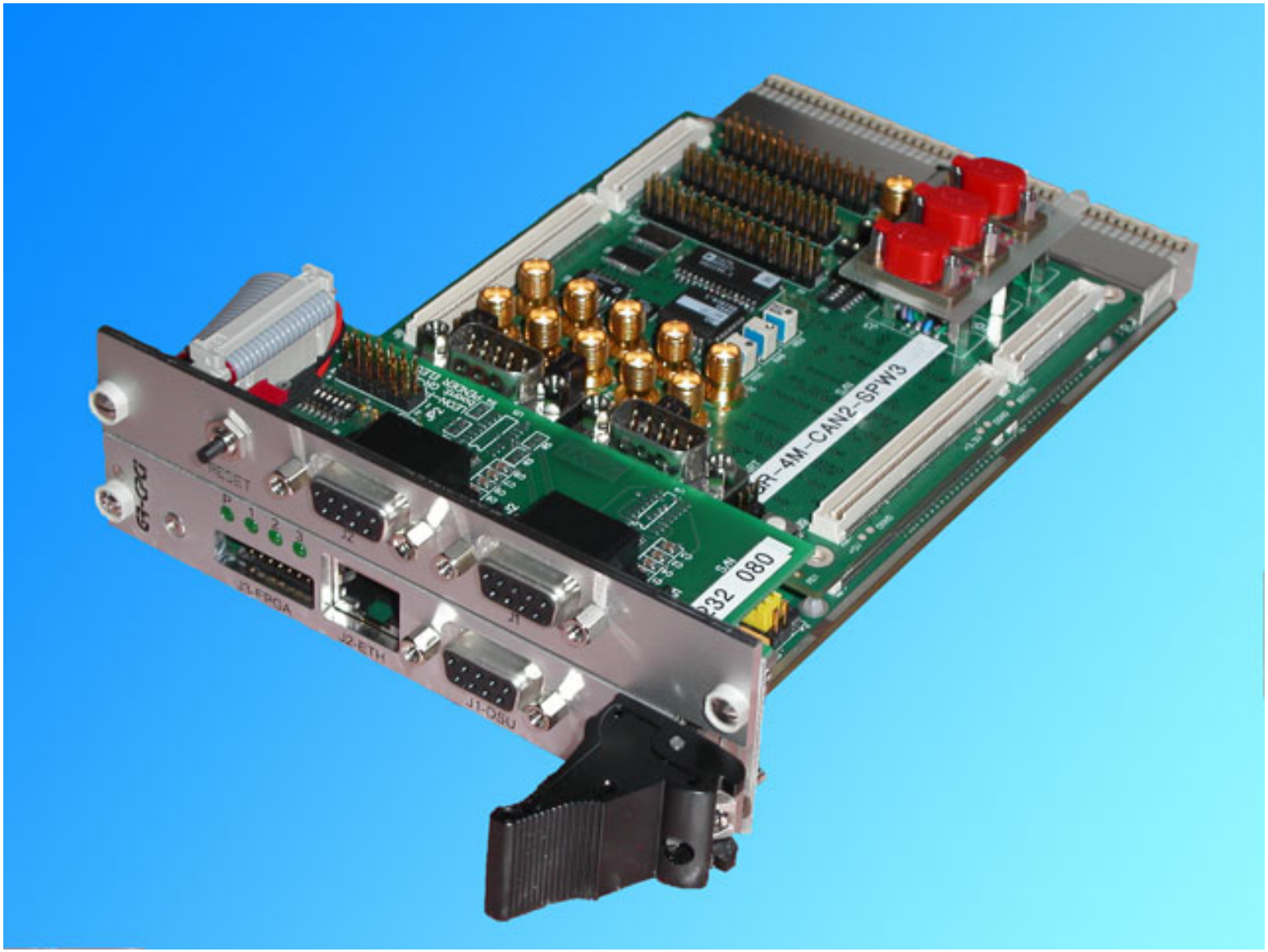
- 40 bits General Purpose Input Output, supporting input, output and pulse generation
- 8-bit/16-bit interface to external FIFO
- Interface to external 8-bit/16-bit ADC
- Interface to external 8-bit/16-bit DAC
- Five 32-bit timers
- LEON2-FT memory controller for SRAM and PROM/EEPROM with EDAC protection

SpW-RTC Evolution

Item	Requirement in ITT	SpW-RTC implementation
Processor	Microcontroller	Leon2-FT SPARC V8 32-bit processor
Floating Point	-	Meiko IEEE-754 FPU
Performance	- (a 803X microcontroller has 2-3 integer MIPS)	34 Dhrystone MIPS, 2 MFlops @ 50 MHz
On-chip memory	32 kbytes	64 kbytes
SpaceWire Links	Two ECSS-E-50-12A SpaceWire 200 MHz links	Two ECSS-E-50-12A SpaceWire 200 MHz links
Remote Memory Access Protocol	-	Hardware support for RMAP ECSS-E-50-11 draft F

SpW-RTC FPGA Validation Board

- Xilinx Virtex-2 FPGA with SpW-RTC design
- 16 Mbytes Flash PROM
- 4 Mbytes SRAM
- 2 SpaceWire links, redundant CAN bus, 2 UARTs
- 24-bit GPIO and FIFO interfaces
- ADC and 4 channel multiplexer
- DAC
- 30 MHz operating frequency, 100 MHz SpaceWire


RESET
J1-FPGA
J2-ETH
J1-DSU
SR-4M-CAN2-SPW3