Single Event Transients characterisation of the ATC18RHA ASIC family

CNES contract 04/1643/00

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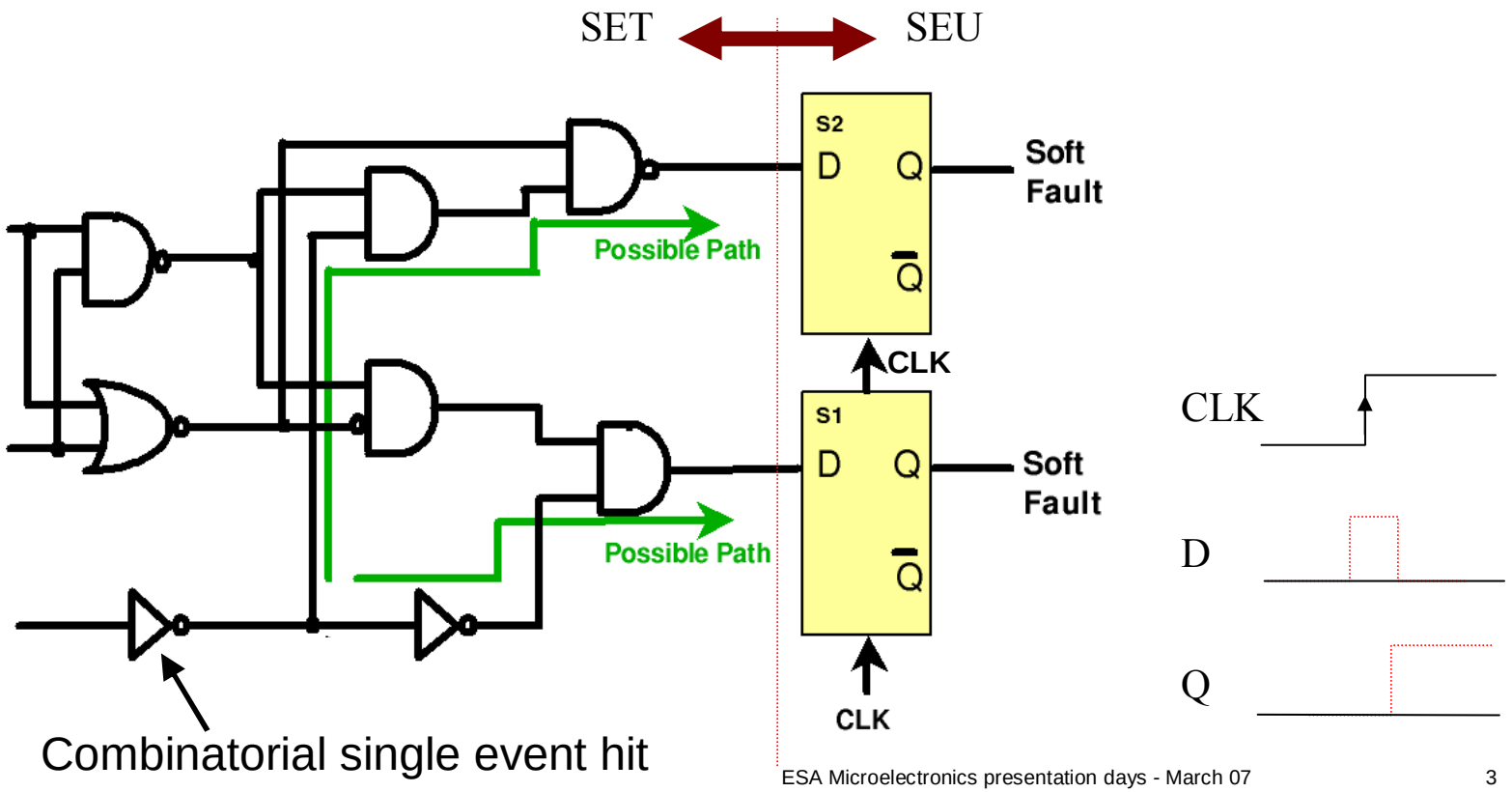
Overview

- Introduction on SET
- SET characterisation
- Status and remaining actions

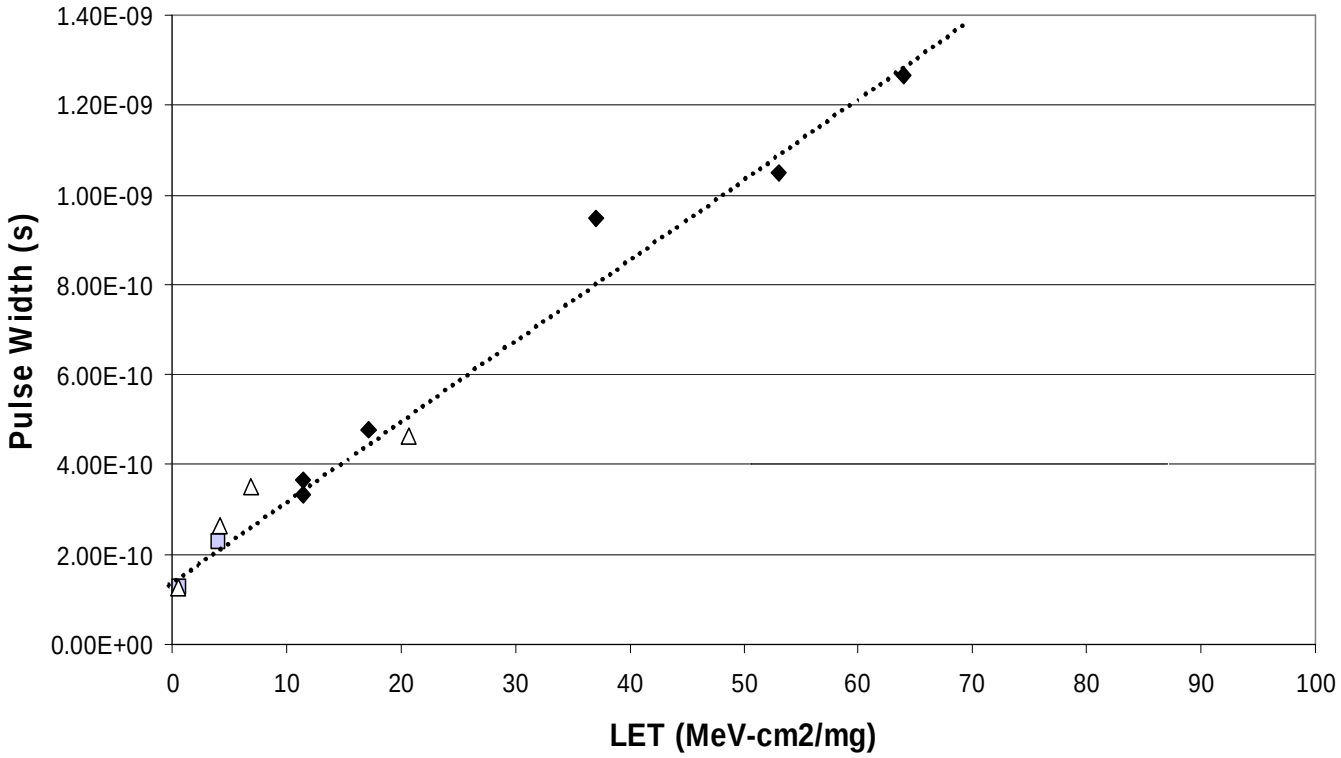
Single Event Transients

- An heavy ion impact can imply
  - An upset of a memory element (or more) : Single Event Upset
  - A glitch in the combinatorial logic : Single Event Transient
    - The propagation of the glitch towards the input of a memory element => error



SET on CMOS 0.18 µm technologies

- **A number of publications in Europe and the USA**
  - **Exemple below : publication from Eaton et al** "SET pulse width measurements using a variable temporal latch technique"

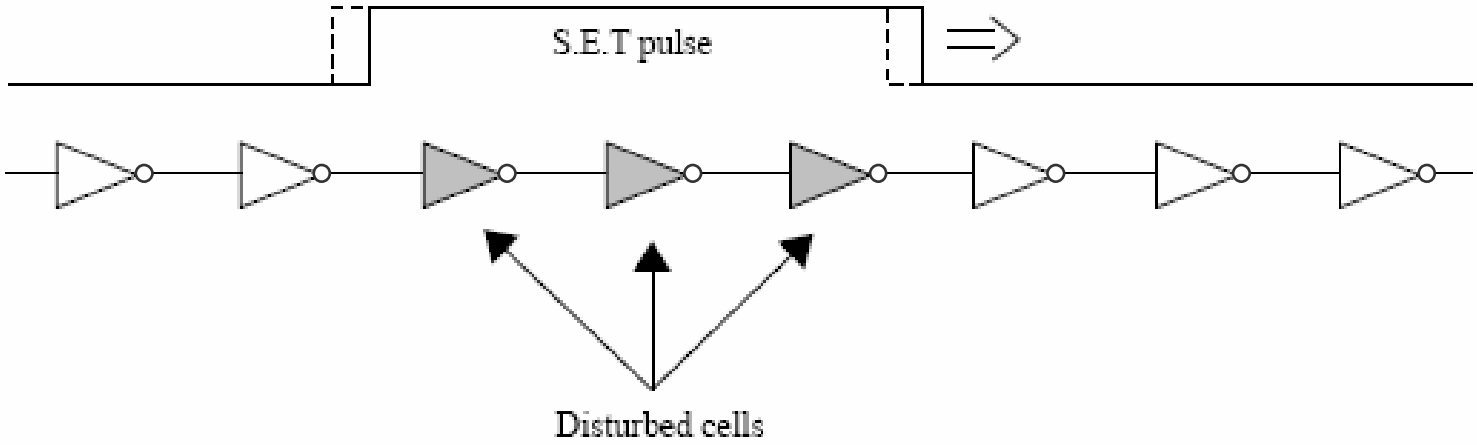


Objectives of the work

- Characterisation of the SET phenomena on ATC18RHA
  - Design of a dedicated test vehicle
- 3D simulation to prepare the test and correlate with the result
  - SRAM (comparison with SEU test results)
  - Inverter
- Heavy ions and proton test of the test vehicle
- Results analysis – information to ATMEL customers
  - ATC18RHA library SET characterisation
  - Potential mitigation techniques (overview only)

Characterisation of the SET pulse width

- **Principle of measurement : chains of cells**

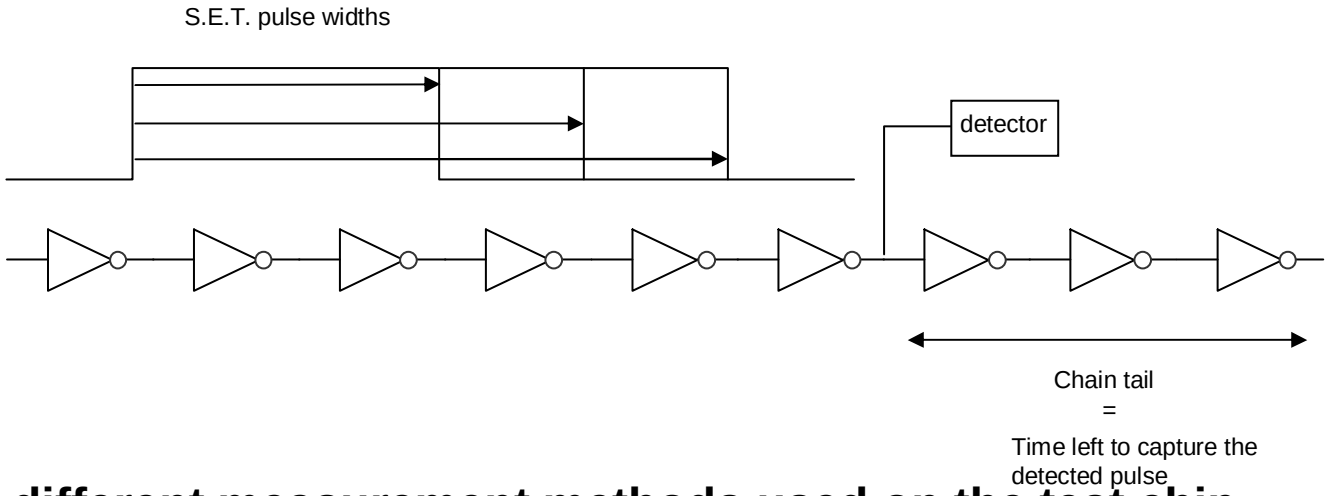


Pulse width = N disturbed cells x cell propagation delay

Typical delay = 50 to 100ps/cell

Pulse width measurements

- Different ways to detect the pulse at the output of the chains



- 3 different measurement methods used on the test chip
  - Frequency related
  - Event related
  - Temporary shift registers (more complex)
- Optimisation of the sensitive area and integrity of the pulse
  - short chains of 64 cells (total > 36000 sensitive gates)

Statistical block

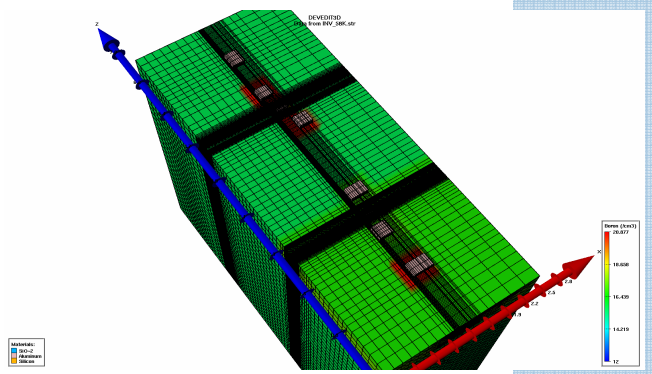
- Objective : count the number of SET pulses detected for various elements of the library (no information on the pulse width itself)
- List of cells of the library :
  - Inverters, nand, nor, flip-flops
  - Various loads and drives
- Extensive multiplexing as the number of chains is > 700
- Some new cells to evaluate possible mitigation techniques
- One SRAM 8Kx8 bits for SEU data (comparison purpose)

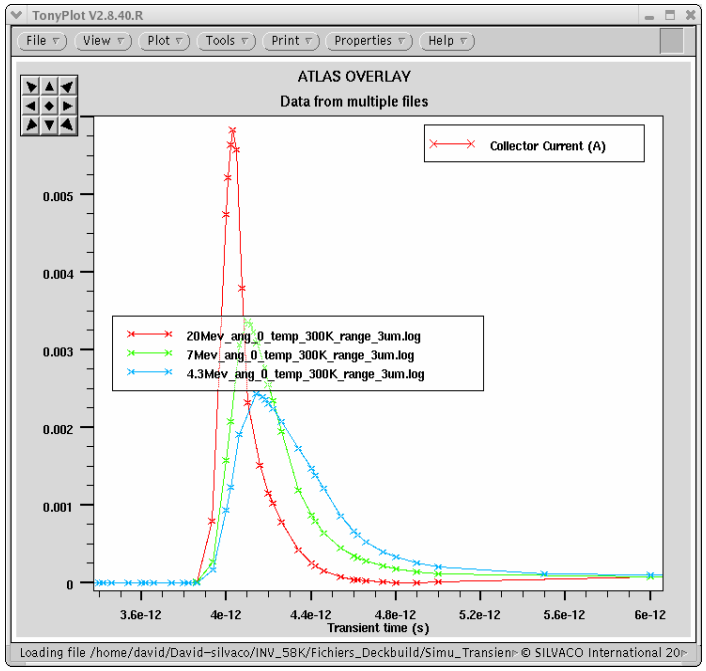
3D Simulations

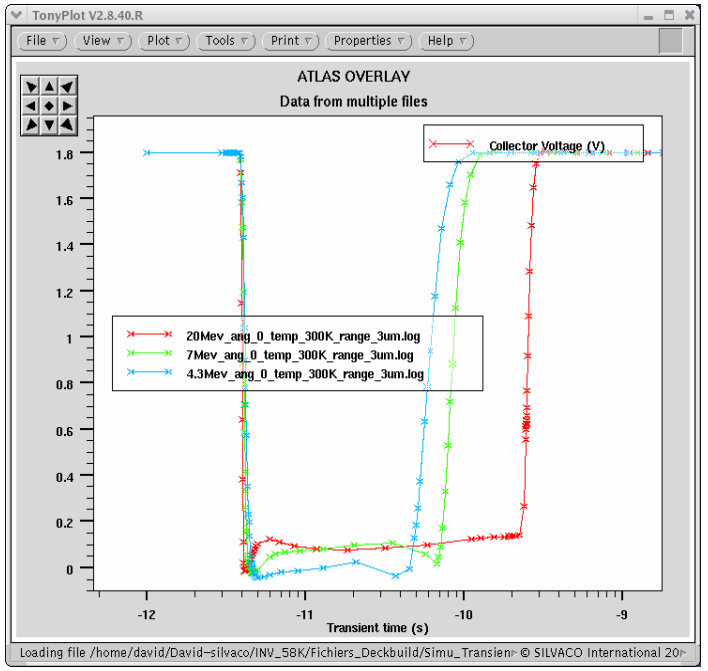
- AT58KRHA technological information
  - SRAM used to correlate between 3D simulation results and SEU test results
- Estimation of the SET pulse width for an inverter
  - Influence of various parameters such as temperature or ion distance to the drain (RADECS 2006 publication)
- Will be used during the test results analysis

SET pulse width

- 3D simulation of an inverter of the ATC18RHA CMOS 0.18µm technology



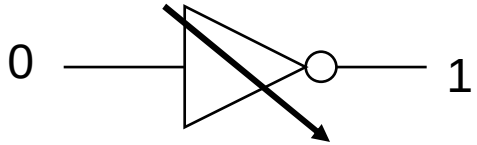


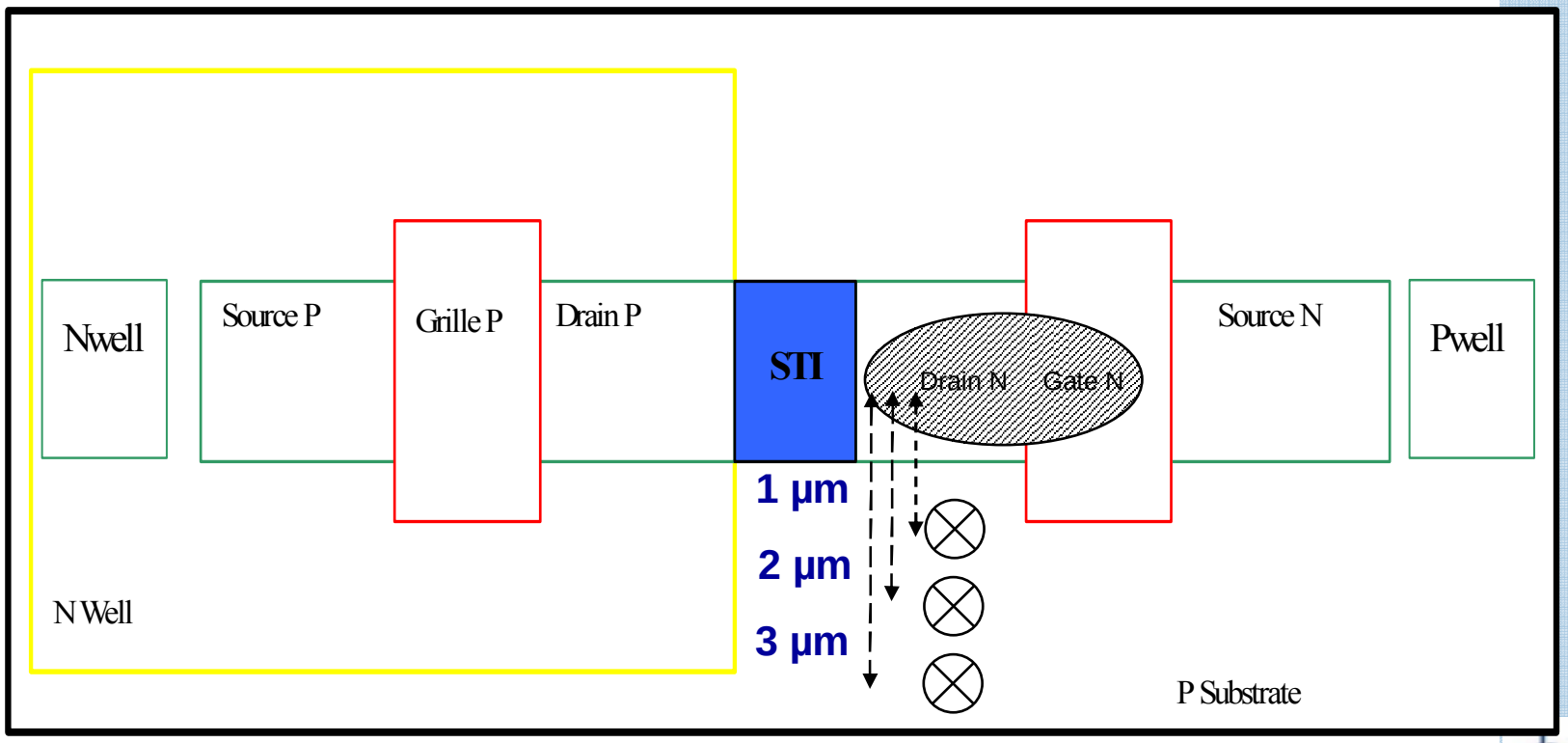


The Voltage duration increases with LET.

Influence of heavy ion impact location

- Inverter

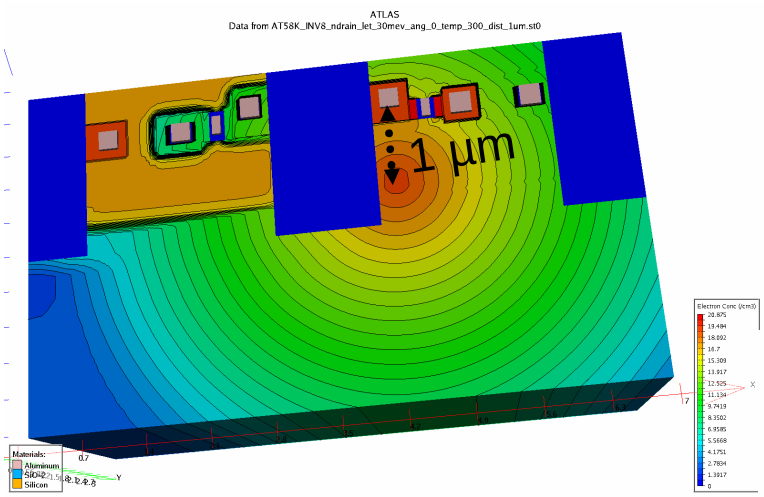


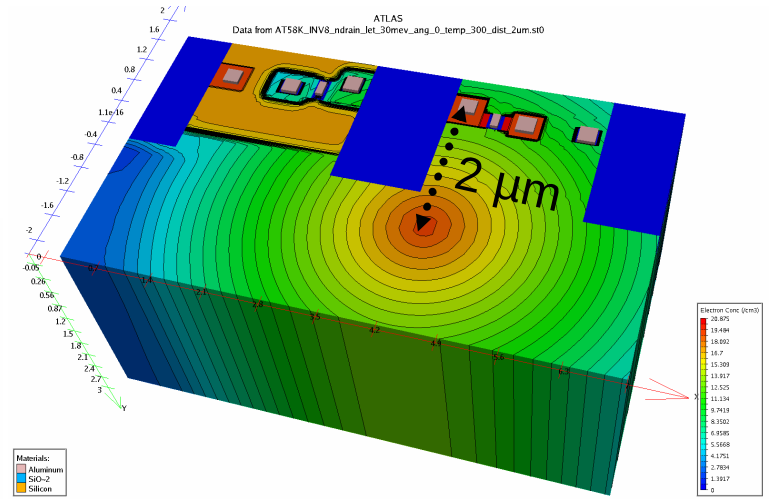


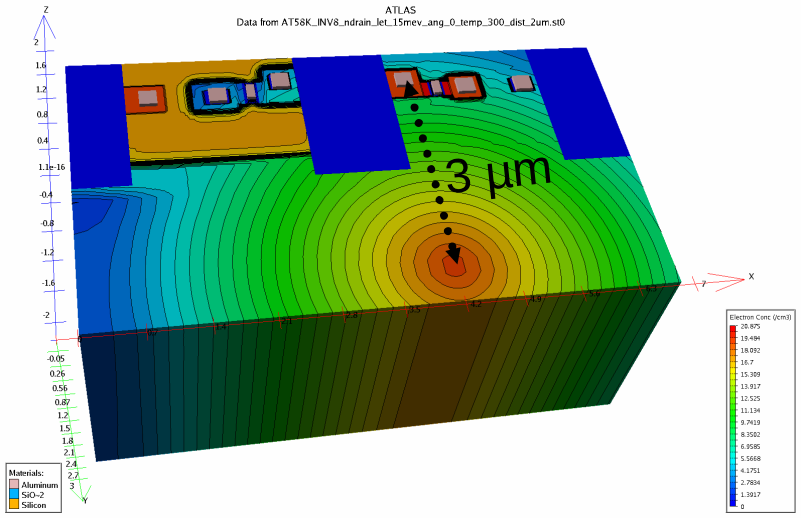
: The most sensitive area

: Heavy-ion impact

Heavy ion impact

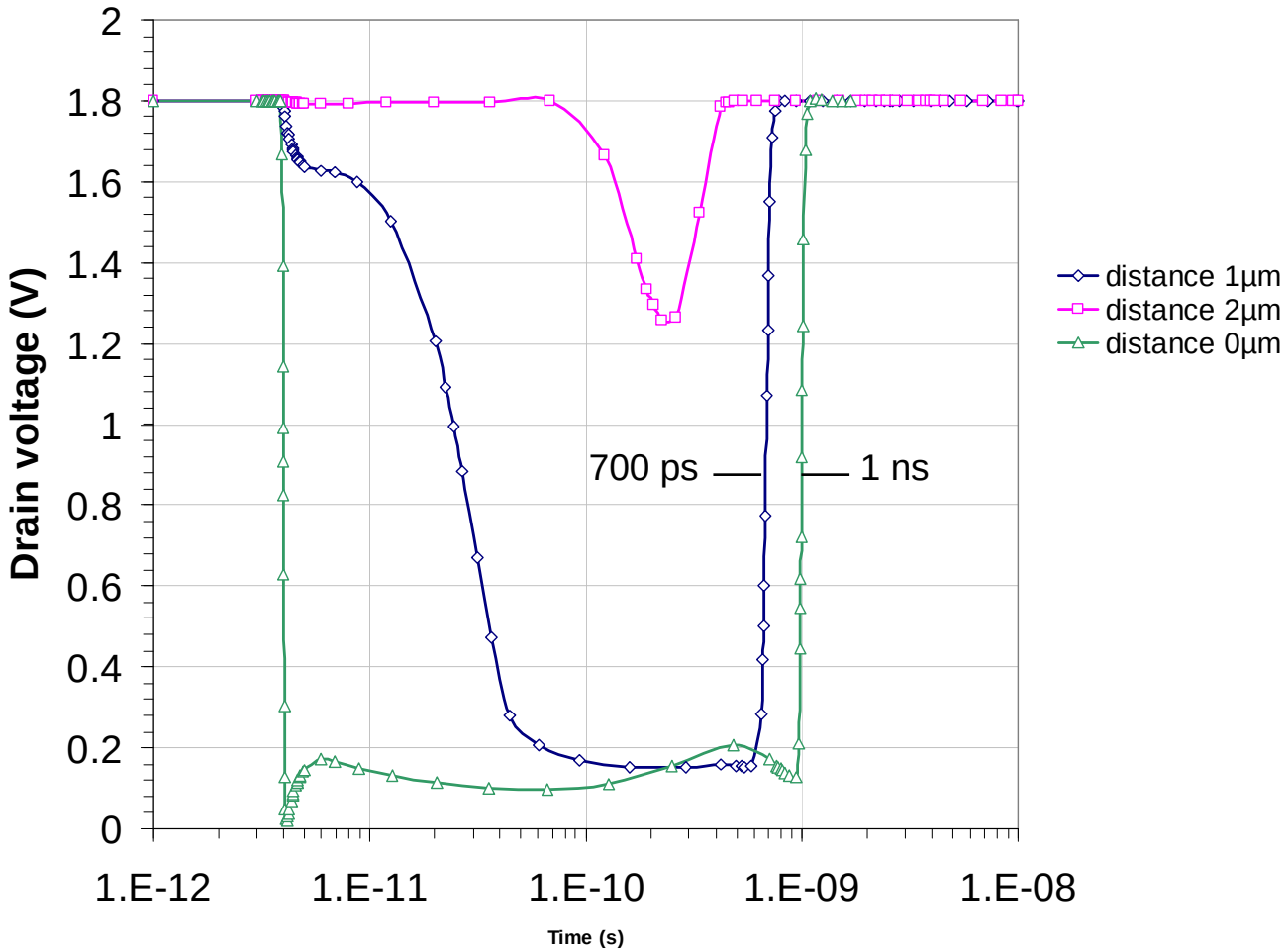






Example of location impact influence

- LET = 30 MeV/mg/cm2



LET influence on pulse shape

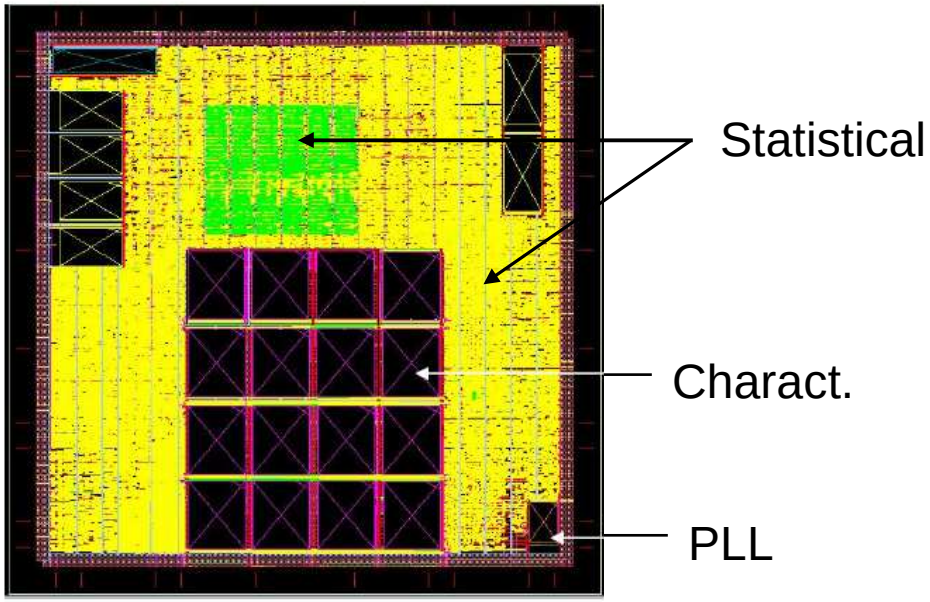
- For a given LET value, when the distance increases:
  - The current magnitude and duration decrease
  - The voltage magnitude and duration decrease
  - Moreover, both current and voltage pulses are delayed.

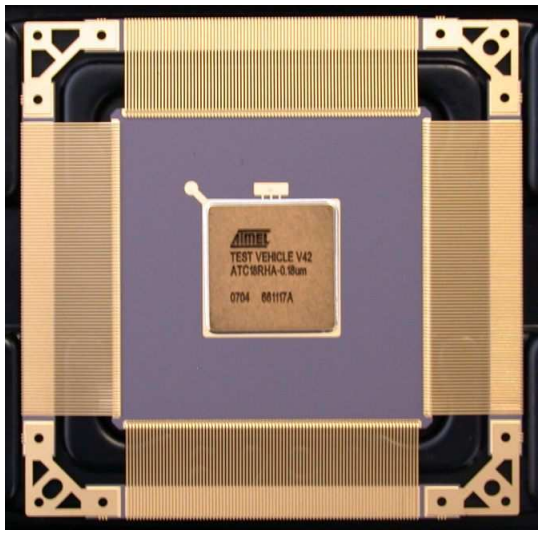
- No trivial law to assess V and I variation with the LET and the ion location
  - Pulse width and amplitude distribution

Status

- **The SET test vehicle is available**

Die size 8.6 x 8.6 mm = 74mm²





MQFP-F 352 pins

Remaining actions

- Heavy ions and protons test
- Report on SET characterisation of the ATC18RHA
- Evaluation of possible mitigation techniques

The end

Thank you for your attention !