

SCOC3 (Spacecraft Controller On Chip)

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1) Project history

- **SCoC1** : First contract 2000: ESA 13345 contract called "Building Blocks for System on a Chip" to:
 - Define a methodology for the integration of system within an ASIC
 - Design a large SCOC1 ASIC through FPGA prototyping based on LEON1. Contract stopped at FPGA prototyping step
- **SCoC2** : ASTRIUM SCoC2 development continuation based on LEON2 with MAEVA FPGA prototype board to improve the architecture and develop new IPs
- **SCoC3** : The aim of the current ESA contract SCoC3 is a continuation process:
 - by moving to the LEON3 and improving the architecture in terms of performance,
 - by developing new IPs and improving existing IPs
 - to simulate and validate the SCoC3,
 - to assess the gate level design phase by performing synthesis and static timing analysis on a selected technology.

2) Project Applications

- Main issue: P/F applications
- Telecommunication satellites: High Reliability
- Earth Observation and Science satellites: From High Reliability to simplex implementation
- Micro satellites with same reliability factor as EO & Science but also low cost approach
- Others like Probes, Launchers, Navigation, Formation flying, ...

3) Activities

- **Phase 1 (TRP)**

Financing	Tasks
ESA	Initial analysis and requirement specification
ESA	Architectural design: <ul style="list-style-type: none"> – Architecture study of block interconnect scheme – Functional specification of the IP macros – Development / modification for adaptation of the IP macros – Simulation at VHDL RTL level / Environment developed in VHDL on a « standard » basis
ASTRIUM	S/W development (drivers, boot, self-tests, ...)
ASTRIUM	SOC approach is verified / debugged on a FPGA demonstration board with SOC function integrated in a reprogrammable FPGA: <ul style="list-style-type: none"> – Activity performed in parallel with the simulation and S/W development – Progressive integration of the IP macros

3) Activities

- **Phase 2 (GSTP under construction)**

Financing	Tasks
ESA	Asic back-end
ESA	Foundry
ASTRIUM	Board validation

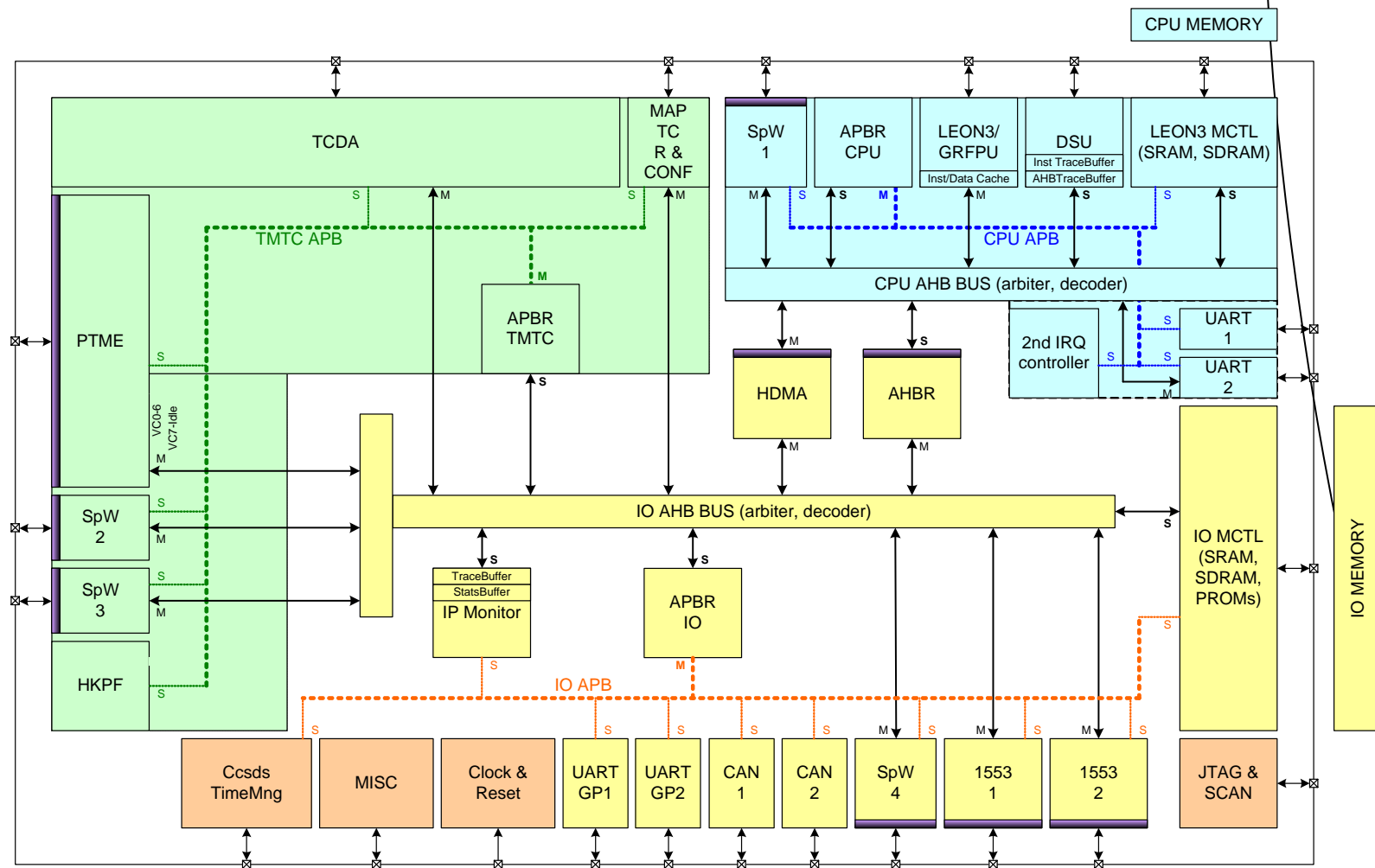
4) SCoC3 Specification

- AOCS/Data Handling on single chip including I/O (1553, SpW, CAN, UART,...), CCSDS TC, CCSDS TM, CCSDS Time Mngt
- Processor LEON3-FT with GRFPU-FT at 120 MHz
- AMBA architecture
- Power management
- IP Monitor: AMBA statistics and trace
- Mature technology: ATC18RHA with qualified package BGA472

5) SCOC3 Architecture

- The processor bloc is based on LEON3 μ P with GRFPU, a memory controller, UART and Spacewire interfaces communicating via the CPU-AHB AMBA bus
- The on-board I/O subsystem providing UART, CAN, SpW, MIL1553 BC/RT. Data exchanges are of DMA type in the I/O memory
- The TM/TC subsystem provides one packet telemetry encoder (PTME) and one telecommand decoder (TCDA) unit, with MAP interface
- The CCSDS time generator and an event switch matrix, clock and reset distribution, debug support

5) SCOC3 Architecture



IO Count: 307
 Gates Count: 900 kgates

Date: 2007/03/07
 MPD ESA

5) SCOC3 Architecture - Main IP block module

Module	Source
LEON3-FT SPARC μ P IP -MMU, GRFPU-FT -AHB/APB	Gaisler Research
Spacewire IP with RMAP functionality	EADS Astrium
CCSDS TM IP	ESA
CCSDS TC IP	EADS Astrium
CCSDS Time Mngt IP	ESA
1553 IP	EADS Astrium
CAN IP	ESA
UART IP	Gaisler Research
Memory Controller IP (SRAM, SDRAM)	EADS Astrium
Miscellaneous (AHB/AHB, Clocks, Housekeeping)	EADS Astrium
Monitor IP (real time debug and tests)	EADS Astrium

5) SCOC3 Architecture - Operating modes

- Full mode - SCOC3 acts as spacecraft main computer
- Processor and I/O only - SCOC3 can be used for payload data handling and processing
- TM/TC only - SCOC3 can replace a conventional TM/TC subsystem using 'discrete' components
- Processor and TM/TC - SCOC3 can be used as main computer next to a separate on-board communication structure

6) SCoC3 Software

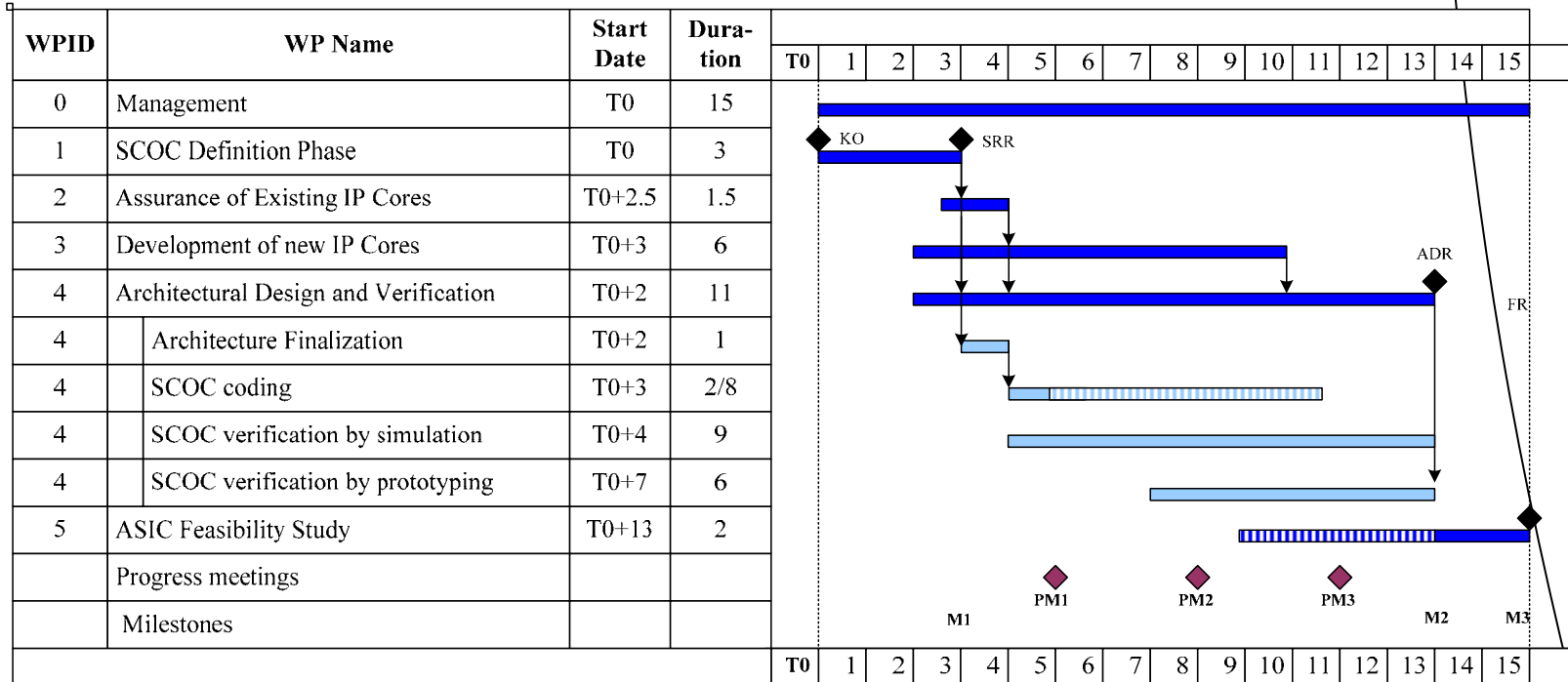
- Drivers with IPs
- Development environment based on C
- Tools: GRMON, TSIM, ...
- SCoC3 simulator created
- RTEMS and/or VxWORKS Operating System
- Service Interface software
- Reuse of DHS layers from Pleïades or Bepi-Colombp

7) SCoC3 Development methodology

- SOC Design leads to find out solutions for:
 - Standardization of the interfaces, internal and external
 - Internal for easy interconnect of IP based on the use of a catalogue of IP
 - External to reduce the number of IP to develop
 - Current standardization of the methodology of validation of SOC model (RTL)
 - Hardware/Software Co-simulation with proprietary solutions
 - Prototype of the SCoC on FPGA and deliver to users/software developers models
 - Simulation remains simulation and only emulates the use of the SOC in modelled environment
 - Accelerate the bug discovery
 - SCoC validation in equipment environment

8) SCoC3 planning

Phase 1:



Phase 2:

Under discussion

9) Conclusion

- Product: On Board Computer core low power/low cost/ low volume
- Methodology: Ever improving the reuse from IPs and standard bus
- Software: Development improved using commercial tools and could be provided with dedicated software support
- Integration: One ASIC allowing different operating modes and several architecture
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