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Radiometric Performance Enhancement of APS

3rd Microelectronic Presentation Days,
Estec, March 7-8, 2007

Outline

- Introduction
- Backside illuminated APS detector
  - Approach
  - CMOS APS (readout) design:
    - Sensor and pixel architecture
    - Readout modes
- Technological developments
  - Thin wafer processing
  - Special features on hybrid arrays
  - Backside surface treatment
  - AR coating
- Conclusions

Introduction

- European Space Agency funded project “Hybrid APS” (ITT AO/1-3970/02/NL/EC)

  Partners:

  - FillFactory/Cypress: design
  - IMEC: technology development
  - Galileo Avionica: radiometric characterization

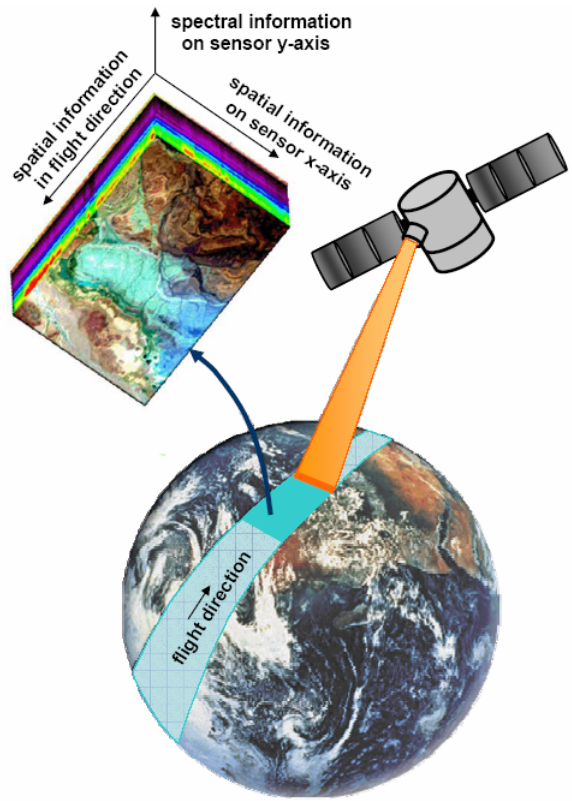
- Aim: snapshot shutter CMOS APS demonstrator for high-end spaceborne imaging

- Hyperspectral imaging

  2-D sensor with spectrometer slit:

  - Spatial information on x-axis
  - Spectral information on y-axis
  - Spatial information by scanning

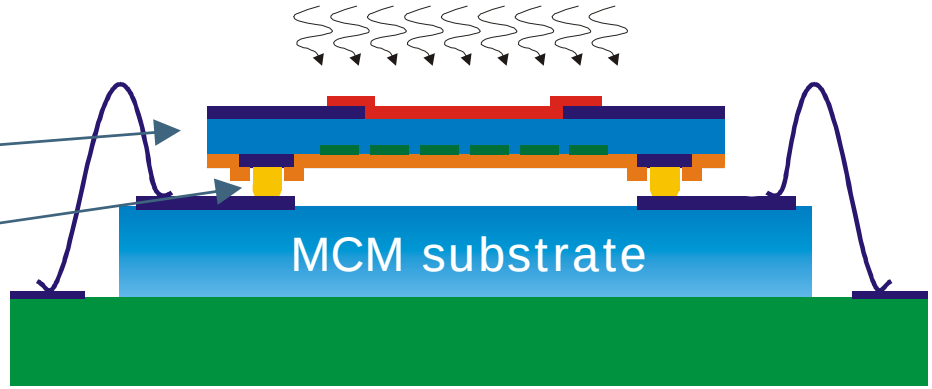
  ⇨ image cube

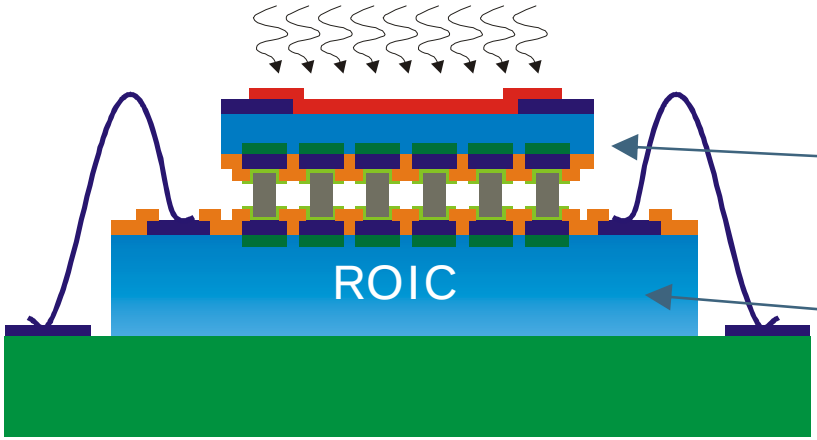


Backside illuminated detector: approach

Monolithic approach

backside thinned CMOS readout array mounted on MCM substrate using Au stud bumps





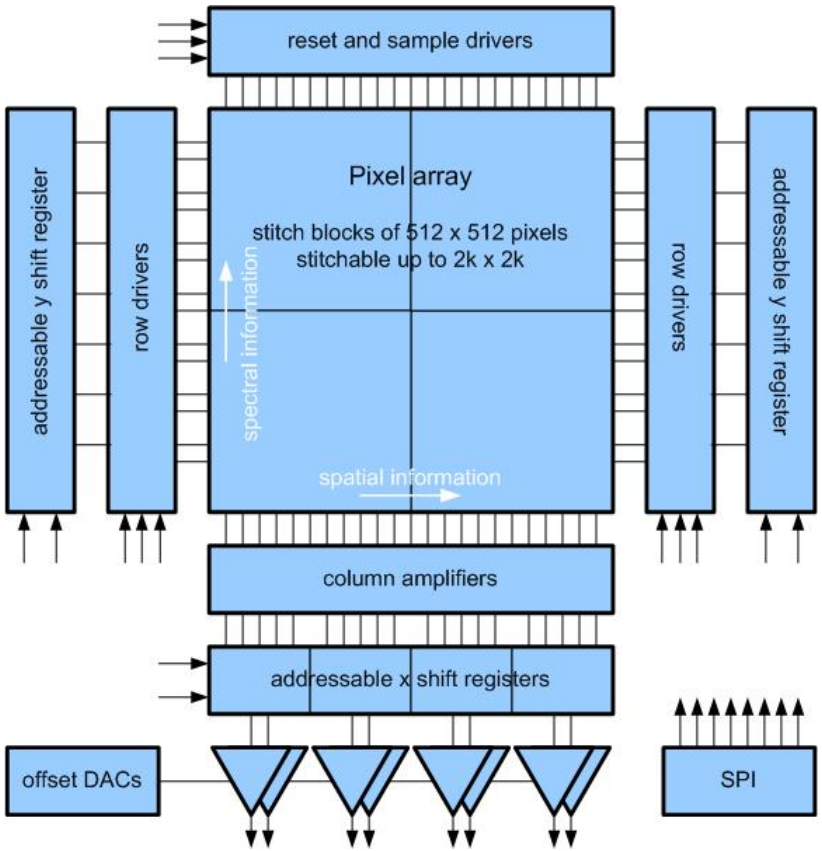
Hybrid approach

backside thinned diode array flip-chip integrated using In bumps

CMOS readout array

Backside illuminated detector: CMOS APS design

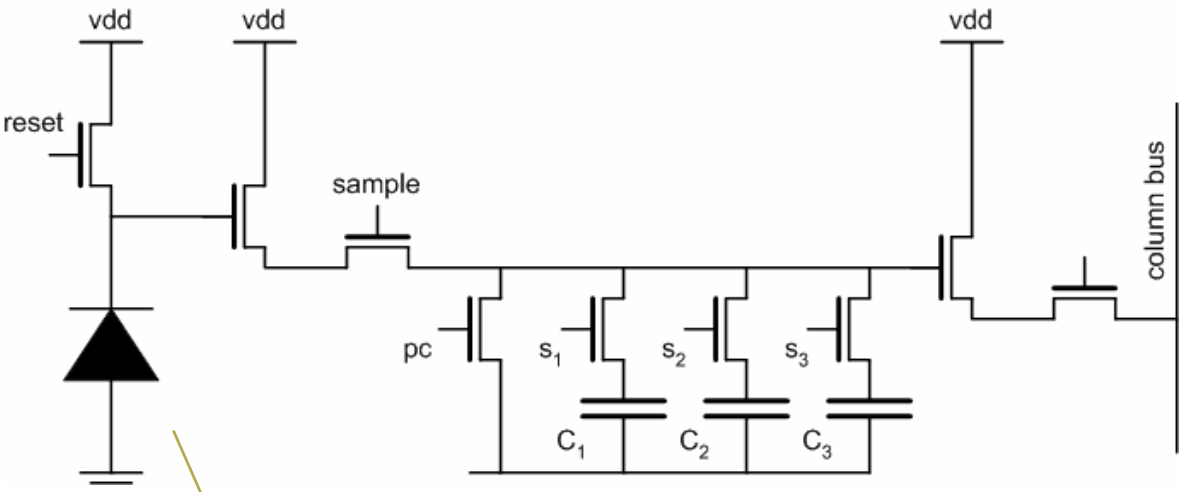
Sensor architecture



- synchronous pipelined shutter
- 22.5 µm pixel pitch
- stitched design:
  - 512 x 512 pixels stitch blocks
  - up to 2048 x 2048 pixels
- pseudo-differential output per 256 columns
- 20 Mpixels/s per output
- SPI interface for upload:

  addressing, gain & offset, NDR, non-linear amplifier, etc.

Backside illuminated detector: CMOS APS design



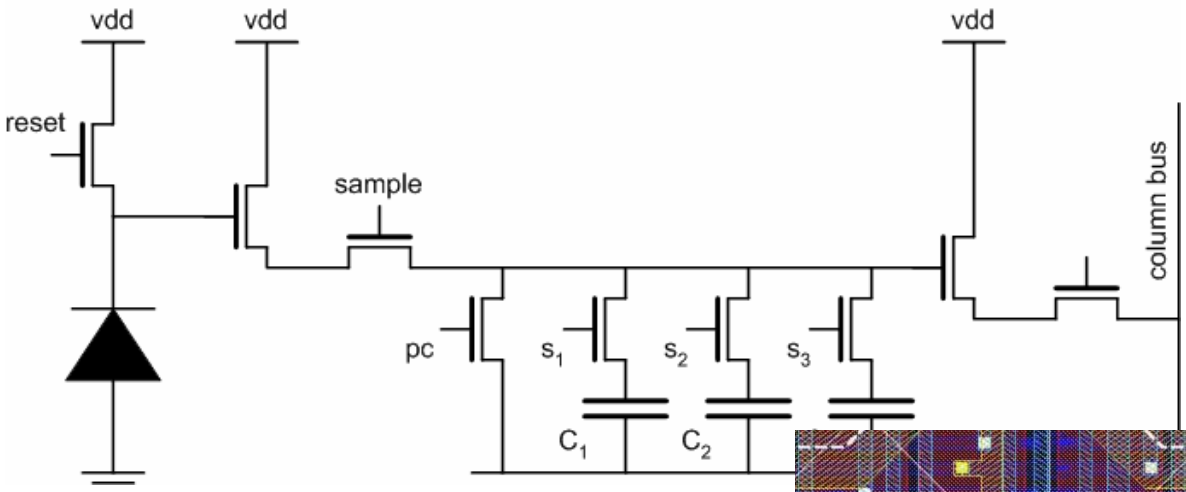
C_{ph} determines charge handling capacity (FWC) and conversion gain

on-chip CDS with synchronous pipelined shutter

$C_{1,2,3}$ determine read noise and dynamic range

	monolithic	hybrid
in-pixel storage capacitance (fF)	350	350
full well charge (x 1000 electrons) (FWC)	150 - 200	250 - 1000
read noise (electrons)	15 - 20	25 - 100
dynamic range (FWC/dark noise) (dB)	80	80
maximum SNR	388-447	500 - 1000

Backside illuminated detector: CMOS APS design

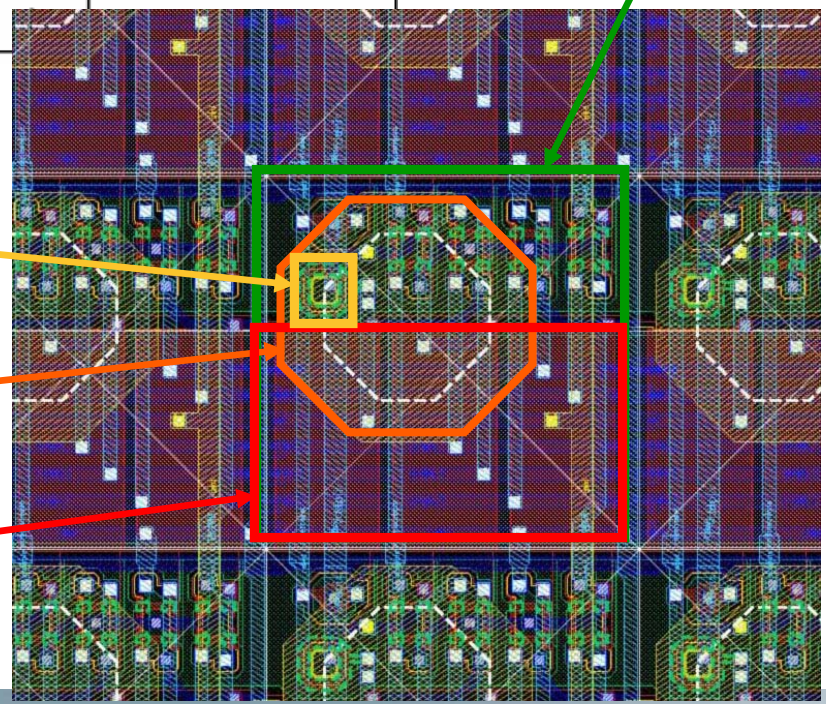


single pixel

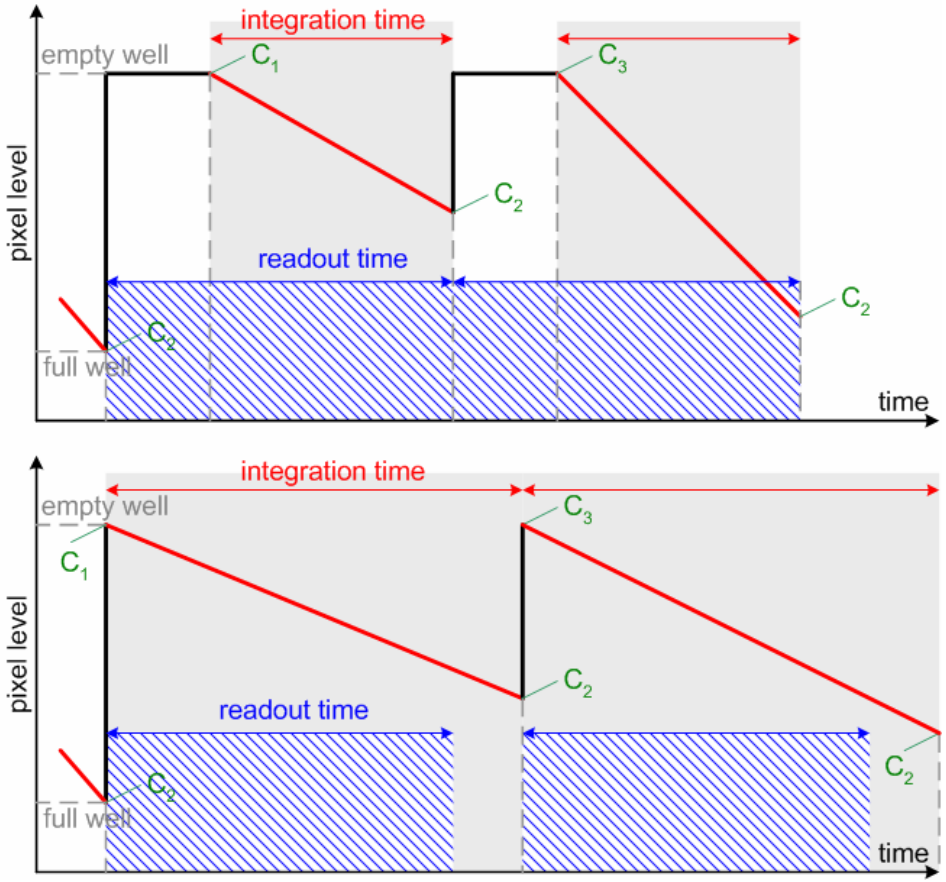
photodiode

pad for hybridization

sample capacitors



Backside illuminated detector: normal readout mode



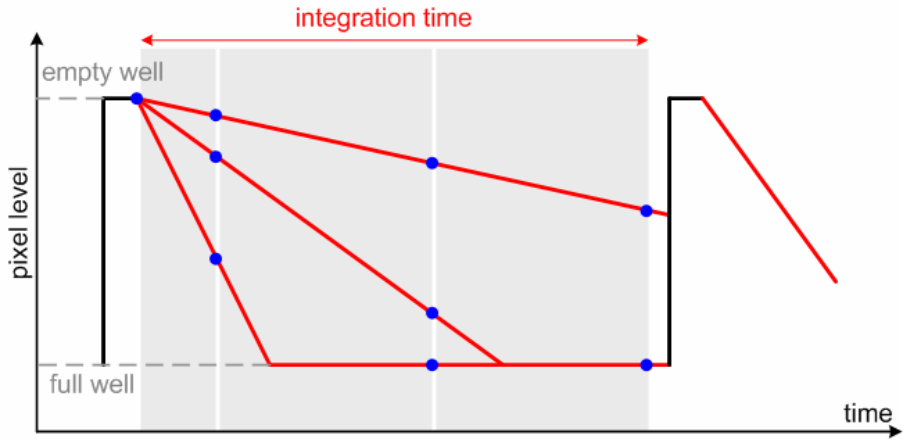
- synchronous shutter:
  all pixels integrate in parallel
- pipelined:
  readout while integrate
- correlated double sampling

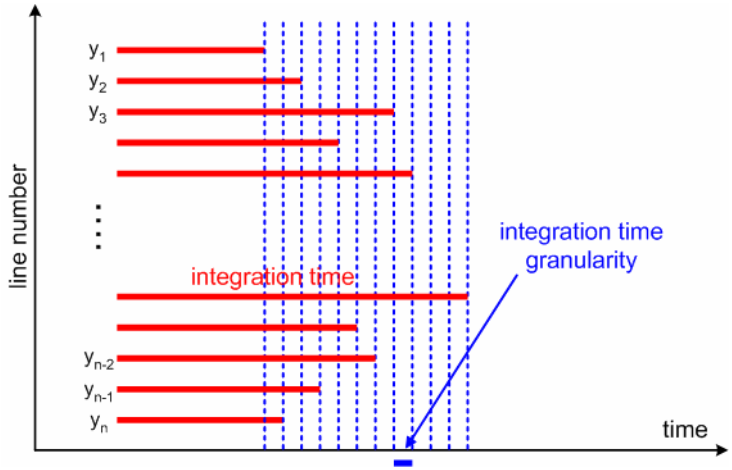
→ $T_{int} < T_{read}$

C_1 and C_3: reset level
C_2: signal level

→ $T_{int} > T_{read}$

Backside illuminated detector: Optimized readout modes



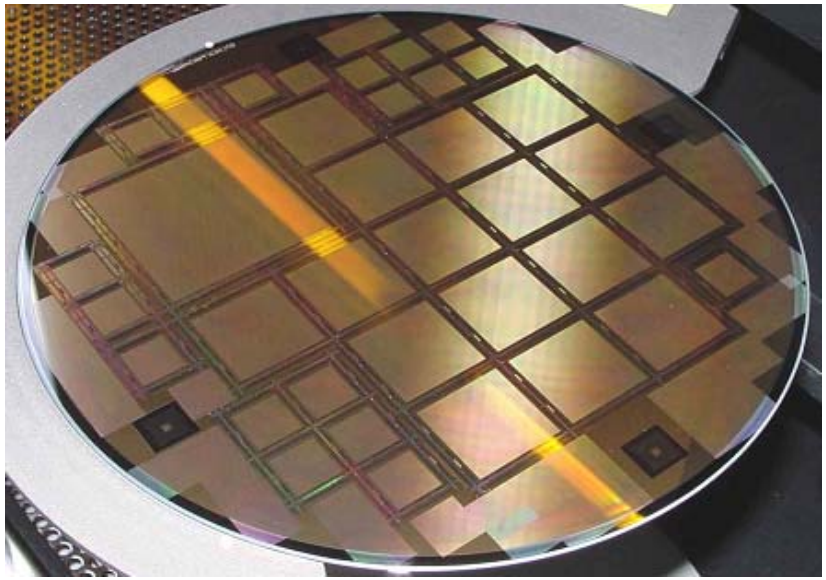


- Non-destructive readout (NDR)
- Line by line variable integration time
- Ref.: J. Bogaerts et al.: 2005 IEEE Workshop on CCD and Advanced Image Sensors, Nagano, Japan, June 2005

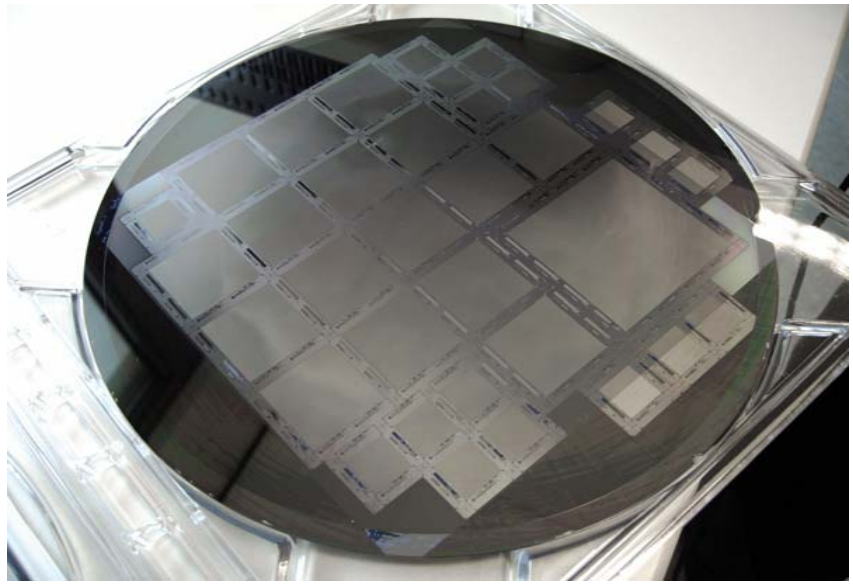
Technology development & challenges

- Realized through stitching stepper lithography
  512^2, 1024^2 and 2048^2 pixel arrays

Readout: 0.35 µm technology @ commercial foundry

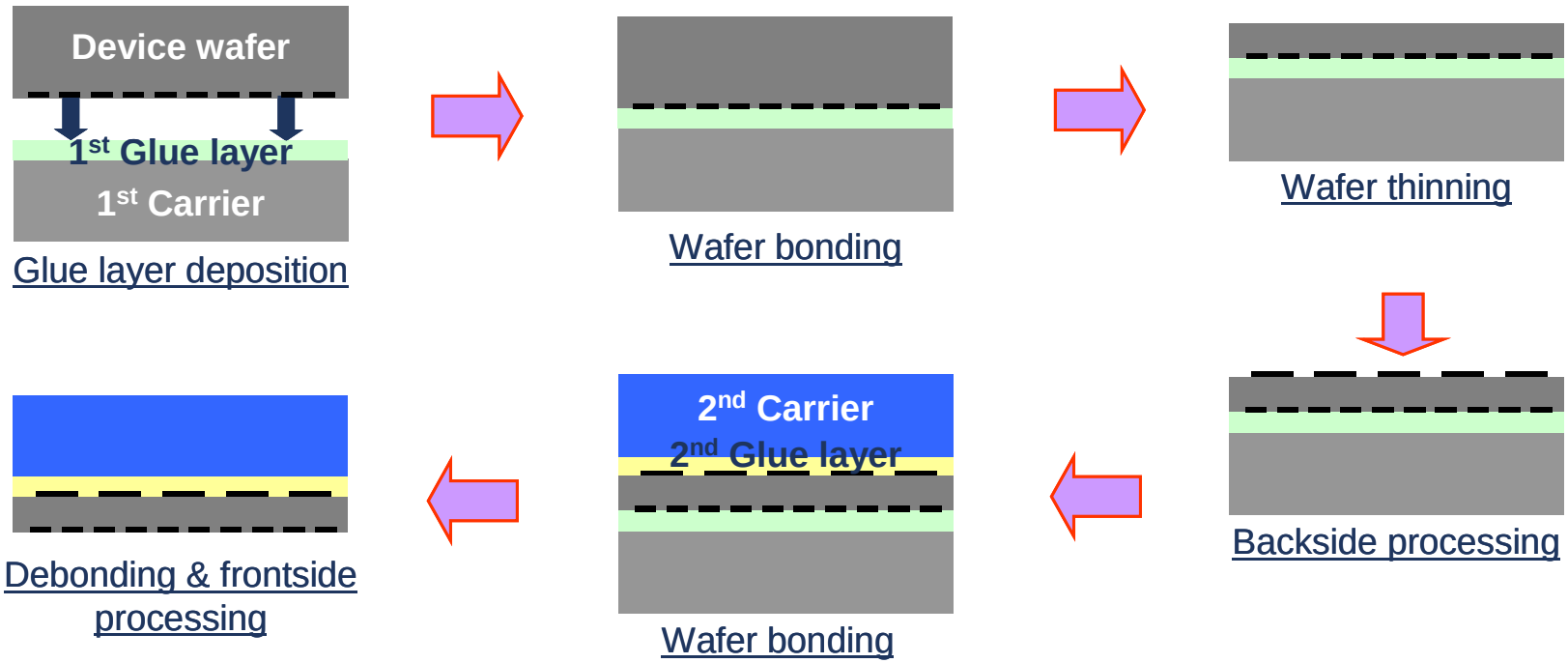


Hybrid diode array: 0.13 µm technology @ Imec



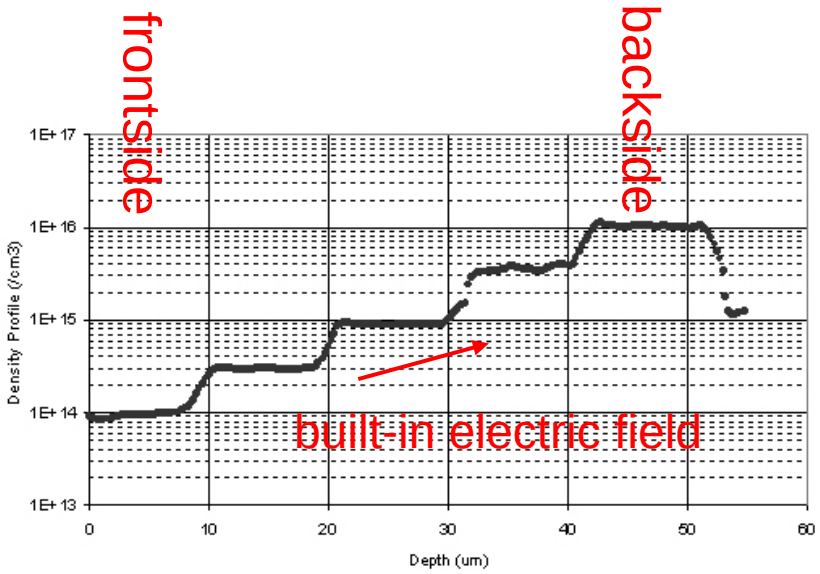
Technology development & challenges: thin wafer processing

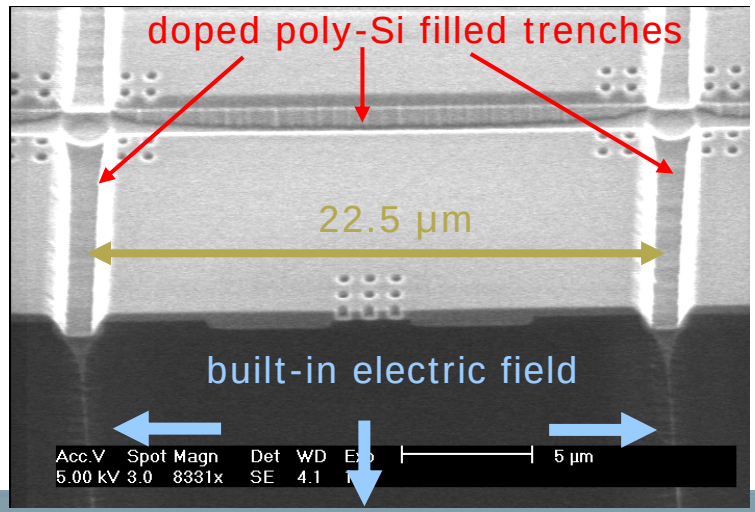
- (post-) processing of thin wafers (35 um)
  - Backside thinning with excellent thickness (uniformity) control (< 1 um)
  - use of temporary carrier for thin wafer handling
  - Ref.: K. De Munck et al., IMAPS Device Packaging 2006, IEDM 2006

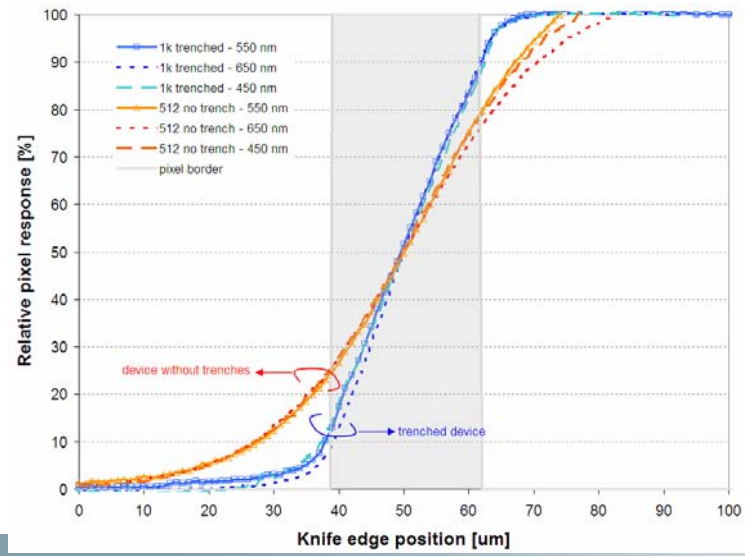


Technology development & challenges: special features

- Hybrid diode array: special features
  - Graded epi for built-in electrical field: enhanced charge collection at low voltage operation
  - Doped poly-Si filled trenches for cross-talk reduction

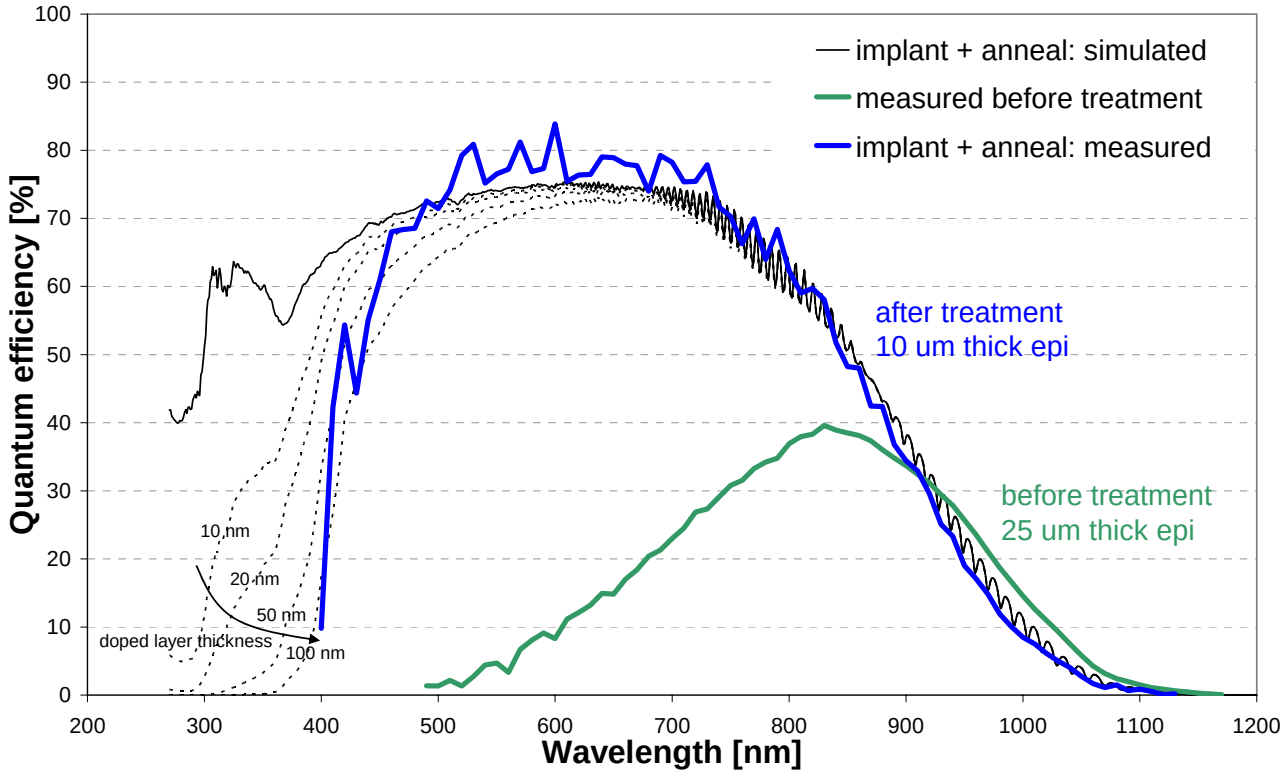






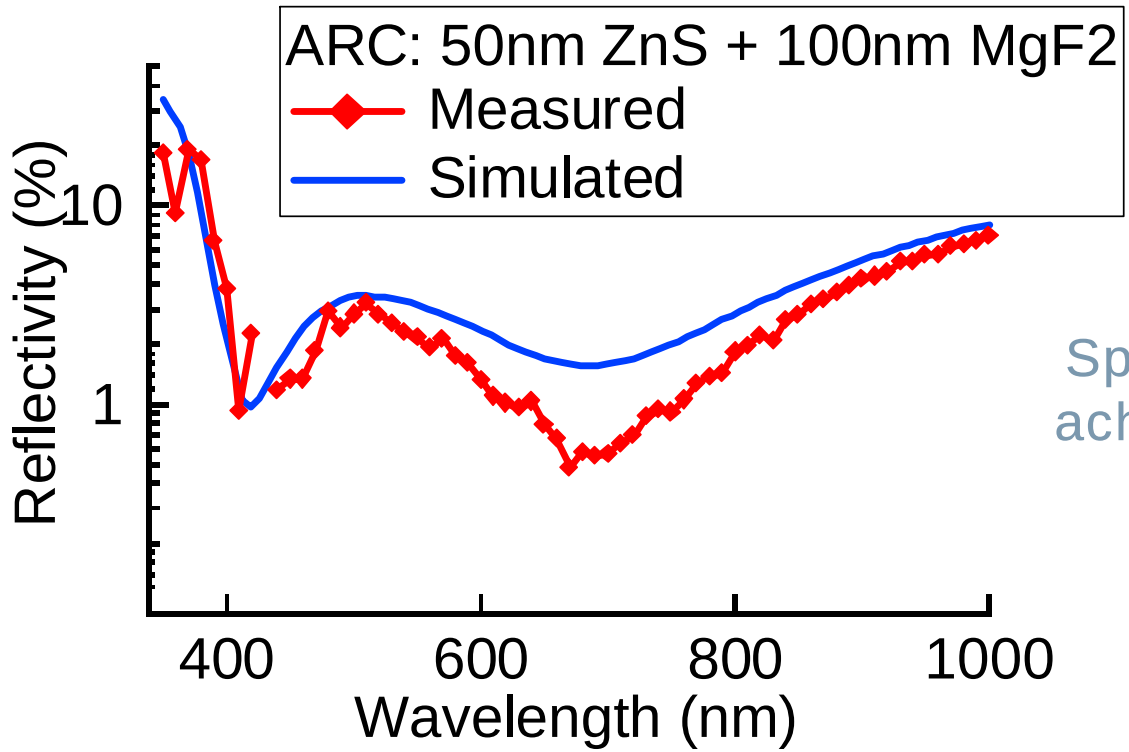
Technology development & challenges: backside passivation

- Backside surface treatment after thinning
  - Damage removal by dry/wet etch
  - Shallow (50nm) backside implantation
  - Dopant activation by laser annealing



Technology development & challenges: AR coating

- Optimized broadband ARC
  - Reflectivity <3% @ 400 to 850nm
  - Spectral response: 60% → >80%

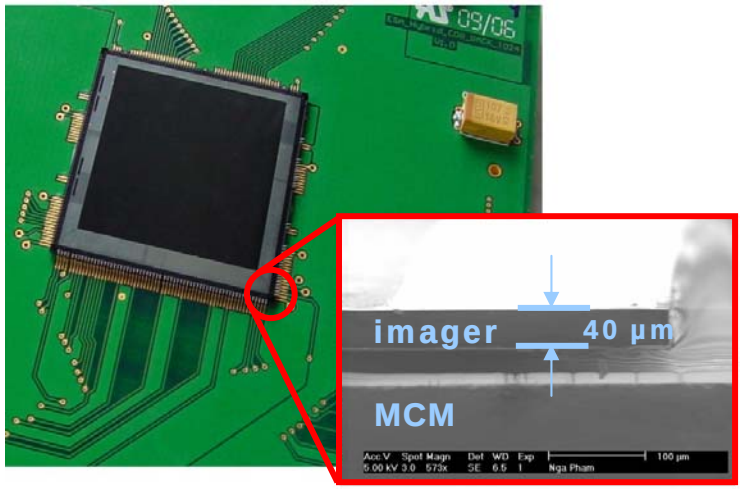


Spectral response spec achieved @ 450-850nm

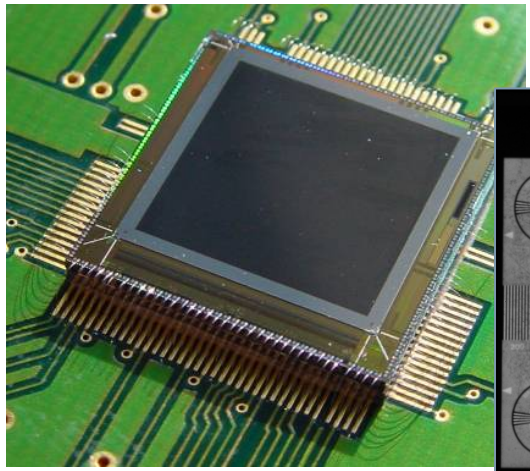
Technology development & challenges

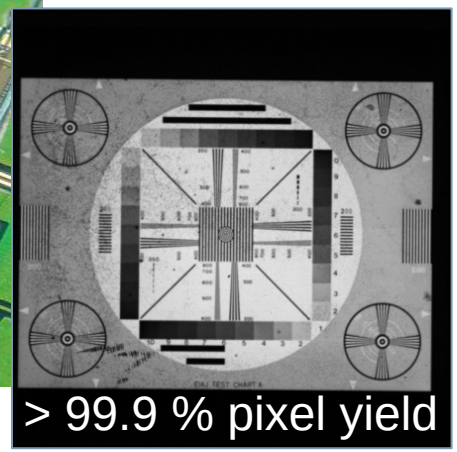
- Working detectors realized: COB package

Monolithic: 1024^2 pixels

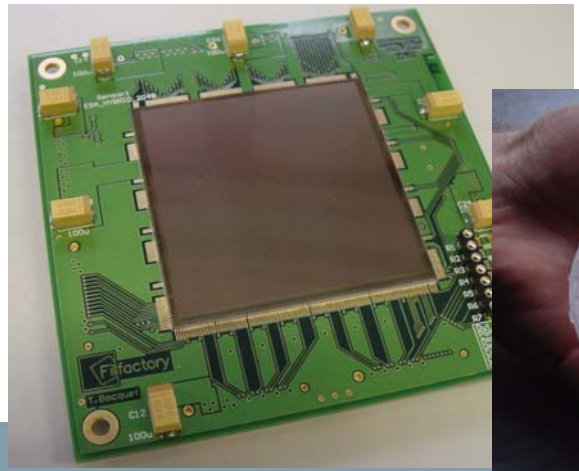


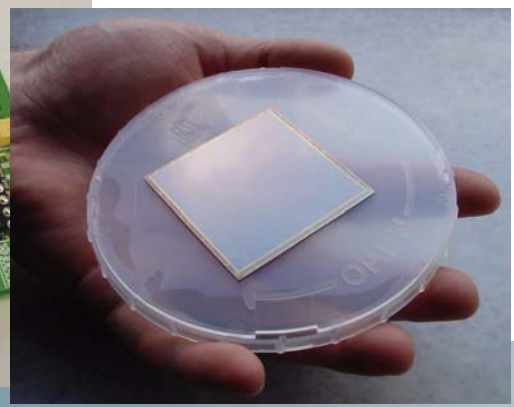
Hybrid: both 512^2 and 1024^2 pixels





Readout: 2048^2 pixels





Conclusions

- Thinned backside illuminated imagers realized
  - Hybridized and monolithic
  - CMOS APS: synchronous pipelined shutter with true CDS
- New 3D process technology for thin wafer handling and processing
  - Use of temporary carriers and glues
  - 200 mm thin wafer processing on carrier with standard equipment
- Performance enhancing concepts implemented
  - Graded EPI → lower cross-talk and improved QE for same voltage
  - Poly-Si filled pixel separating trenches → low cross-talk
- Working demonstrators
- Detailed characterization is currently ongoing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