



The ADPMS experience

***An Advanced Data & Power Management System
for small satellites & missions***

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Introduction



In a contract for the European Space Agency, Verhaert Space developed a state-of-the-art control unit for small but high demanding satellites.

Built on the experience gained with the PROBA-I satellite that has been in daily use since its launch in 2001. This next generation avionics has been developed and will have its first in-orbit demonstration in 2007 as the satellite control unit for PROBA-II.

The need for a performant, easily adapted and configured satellite control unit has been identified as crucial to succeed in the system design of small satellites with high autonomy demands.

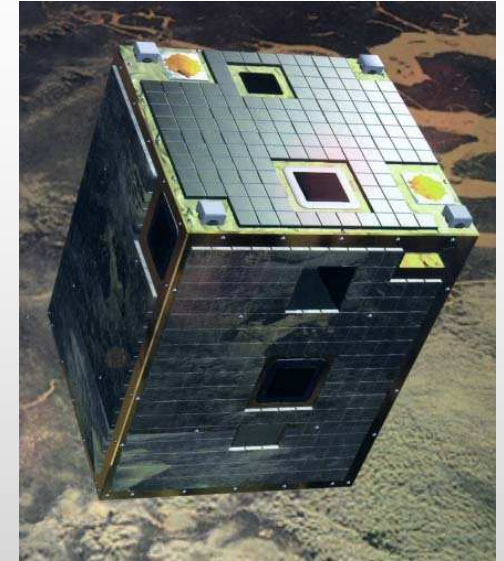
The European Space Agency initiated different programs to demonstrate the concept and feasibility of small satellites with high performances in terms of:

- **Autonomy**
- **On board processing capabilities**
- **Payload management**

Introduction (2)

The PROBA-I satellite, currently in orbit, has shown some limitations in its Data Handling System, Payload Processing Unit and Power Conditioning System in terms of:

- **Power consumption**
- **Mass and Volume**
- **Design complexity due to a lack of uniformity**
- **Proprietary 'closed' architecture (black box design)**
- **Limited computing and data-handling performance**
- **Modularity**
- **Scalability**
- **Testability**



A detailed look at the above top-level requirements identifies however some contradictions:

- Low power consumption versus high computing performance
- Low mass and volume versus modularity
- Highly integrated system versus testability

This presentation describes how the ADPMS design has provided an answer to all above criteria without penalising one of them.

Satellite requirements



For Earth Observation instruments

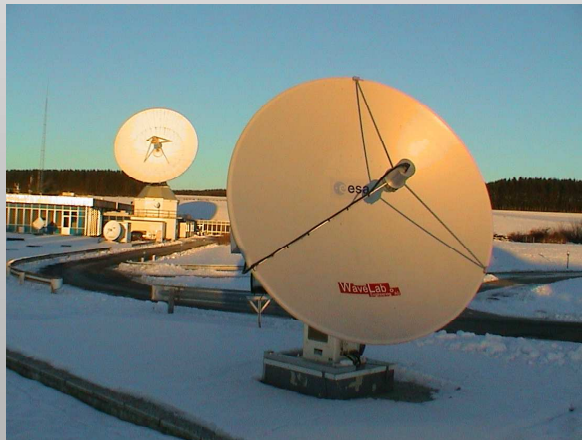
1 image
=
1 command

(target latitude and longitude)



Onboard Autonomy Features

- Autonomy in planning / scheduling
- Autonomy in attitude control system
- Autonomous target prediction and trajectory generation
- High level payload management
- Powerful automated on-board functions



Ground Segment Automation

- Internet access for payload activity requests
- Internet access for payload data distribution
- "Light-out" ground segment

Satellite requirements (2)

Pointing Modes

Inertial Pointing

Possible Utilisation:

- Astronomy
- Solar physics



Earth Pointing

Possible Utilisation:

- Earth Observation (pushbroom)
- Telecommunications
- Space Environment



Fixed Earth Target Pointing

Possible Utilisation:

- Earth Observation (snapshot high resolution imaging)
- Elevation Modeling
- Disaster Monitoring



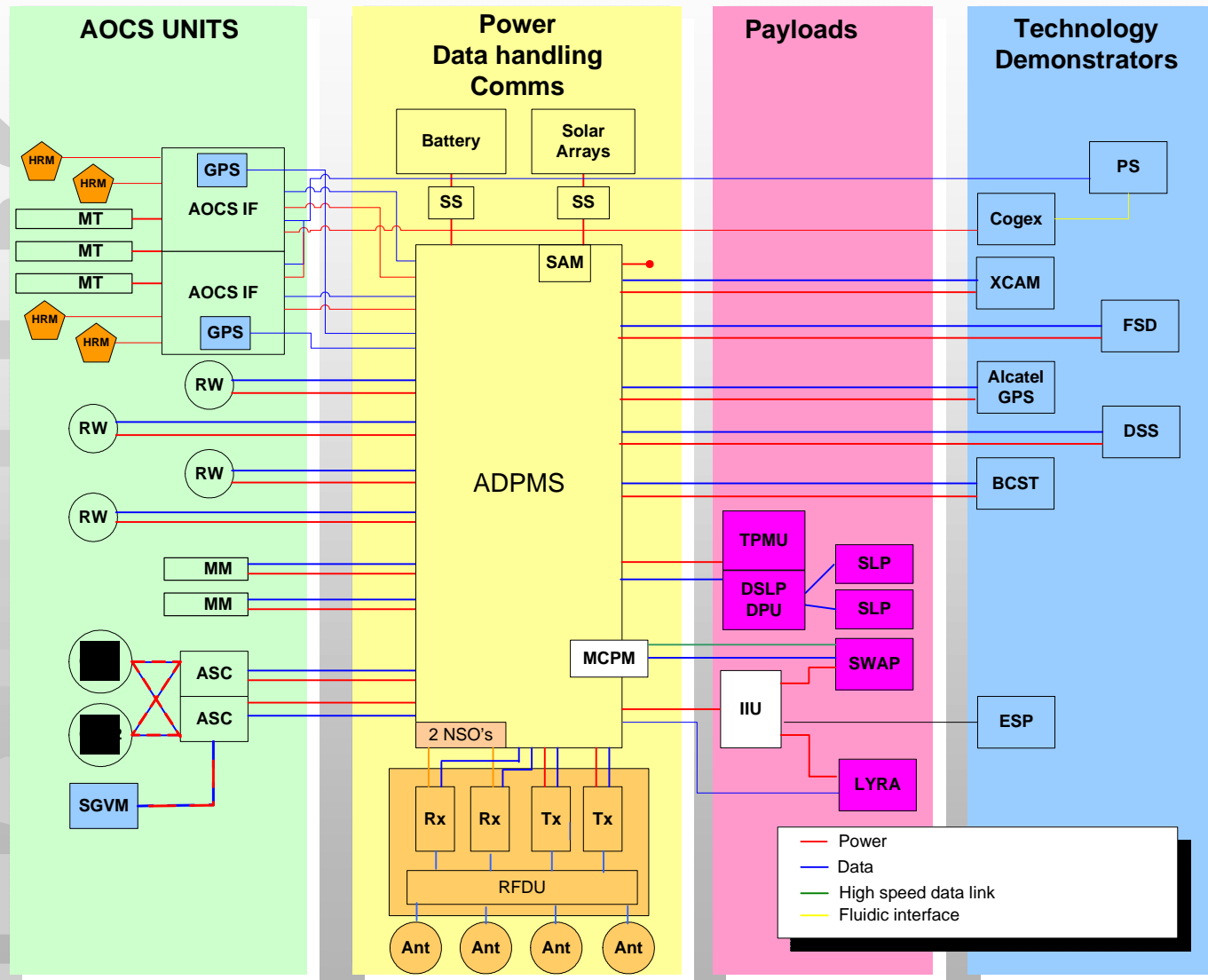
Complex Manoeuvring

Possible Utilisation:

- Earth Observation
- Multiple target imaging
- Image Paving



Satellite requirements (3)



Satellite requirements (4)



Satellite Objective: more resources available for the Payloads

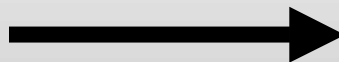
PROBA-I ***Mass***

~30% for the payloads
~70 % for the satellite bus

Power

~30% for the payloads
~70 % for the satellite bus

20% reduction
for the bus
elements

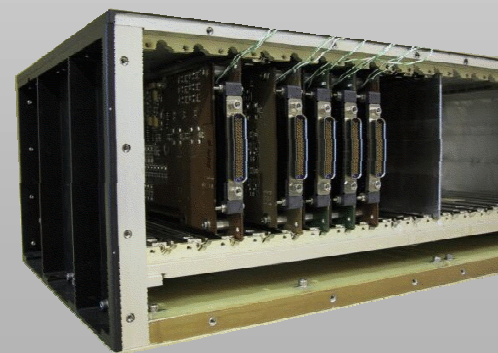


PROBA-II ***Mass***

~50% for the payloads
~50 % for the satellite bus

Power

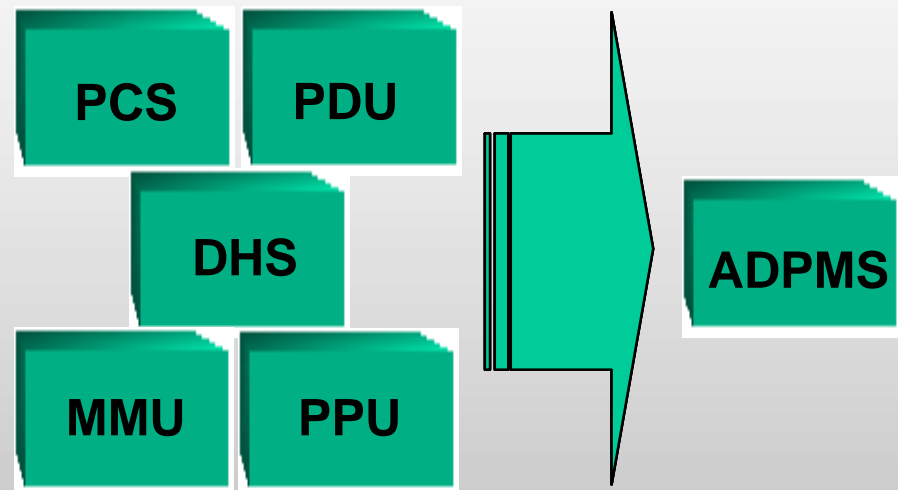
~50% for the payloads
~50 % for the satellite bus





In order to fulfil the top-level requirements listed before some drastic changes were needed. Therefore the following five essential satellite bus elements have been incorporated into one system:

- S/C Power Conditioning System (PCS)
- S/C Power Distribution Unit (PDU)
- S/C Data Handling System (DHS)
- S/C Mass Memory Unit (MMU)
- S/C Payload Processing Unit (PPU)



A very effective power, mass and volume reduction could be achieved by the integration of these elements. Resulting at Satellite level in a:

- **centralisation of all data handling, storage and processing**
- **centralisation of all analog- and temperature sensor acquisition**
- **elimination of the harness that interconnected the formerly separate units**
- **reduction of the mechanics because of the integration into one physical enclosure.**



Architectural overview

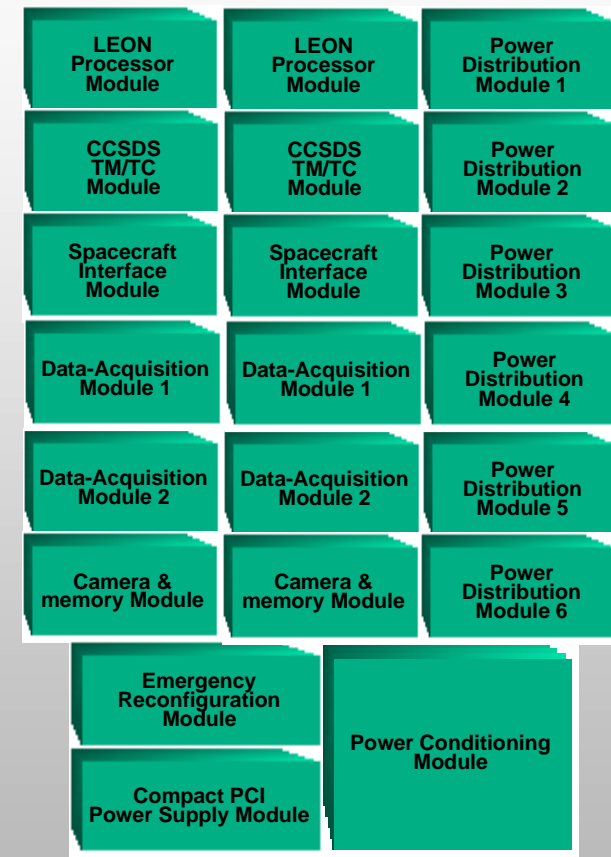
The computer is partitioned into sub-modules in the form of 3U Compact-PCI boards.

The main modules consist of:

- a processor board with memory
- a TM/TC board
- a spacecraft interface board
- one or more data-acquisition boards
- a camera board with mass memory
- a reconfiguration board.

The integrated power system consists of:

- a power conditioning module
- several power distribution modules
- a Compact-PCI power supply module.



Re-use of industrial standards

The design complexity of the ADPMS has been significantly reduced by the implementation of some well-proven industrial specifications resulting in a higher uniformity of the FPGA and board designs. The selection of these widely-used standards

Compact PCI standard → key-features:

- open specification (coordinated by PCISIG and PICMG)
- widely accepted → reviewed by a large user community
- protocol-, electrical-, mechanical- and configuration-aspects guarantee compatibility between plug-in boards
- electrical- and pcb-layout guidelines allow reliable product-design
- suited for rugged environments
- low power consumption (reflected wave-switching <-> fixed bus terminations)
- high throughput data communication
- light weight, high-density, low EMC connector technology
- expandable
- multi-processor support.

AMBA™ AHB standard → key-features:

- open specification
- widely accepted
- high throughput data communication
- expandable
- multi-processor support

Off-the-shelf IP-blocks and testbenches enable reliable IP re-use & validation

Off-the-shelf 19" racks, backplanes, processors and analysers available to facilitate board level testing

Peripheral DMA engines

In many existing systems, communication between modules with unequal data rates or large data latencies create blocking of the shared buses, such as the PCI bus or on-chip AMBA buses.

Fast processor and high speed bus

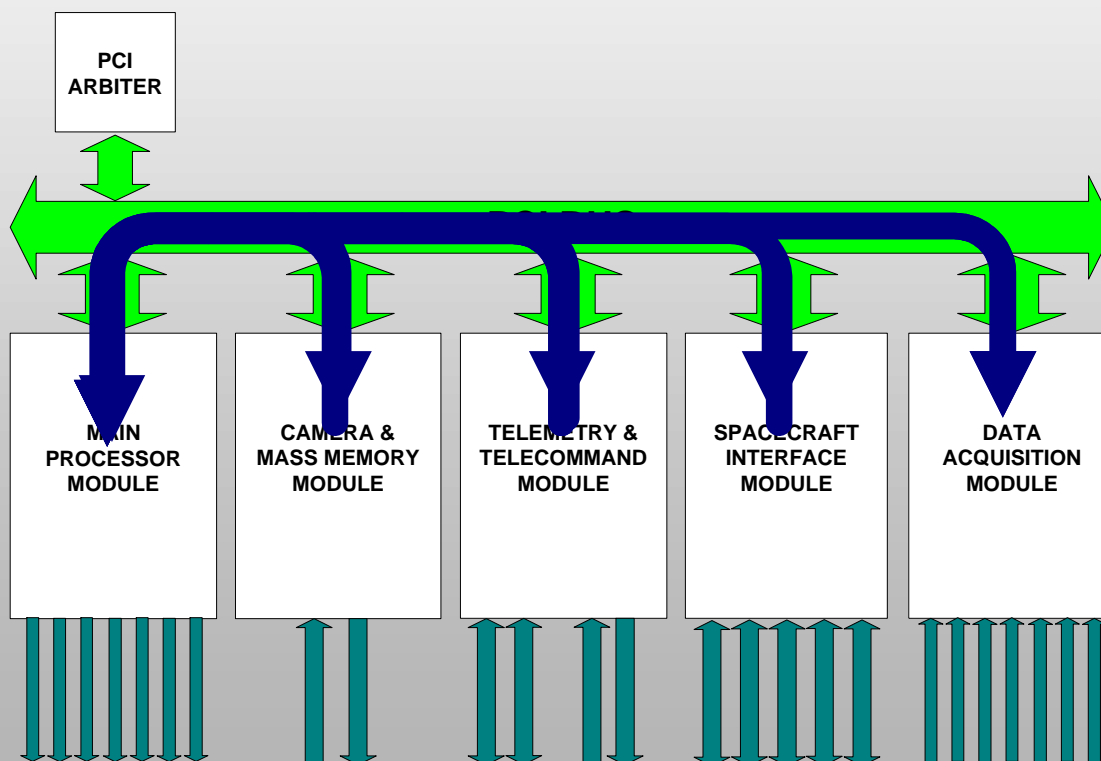
↔ slow peripherals

→ Data bottlenecks

- waitstates
- retry cycles
- processor DMA
- interrupts

→ Peripheral DMA engines

- know when data can be transferred
- no local FIFO buffers
- lower power consumption
- no processor time
- full bandwidth usage
- growth potential

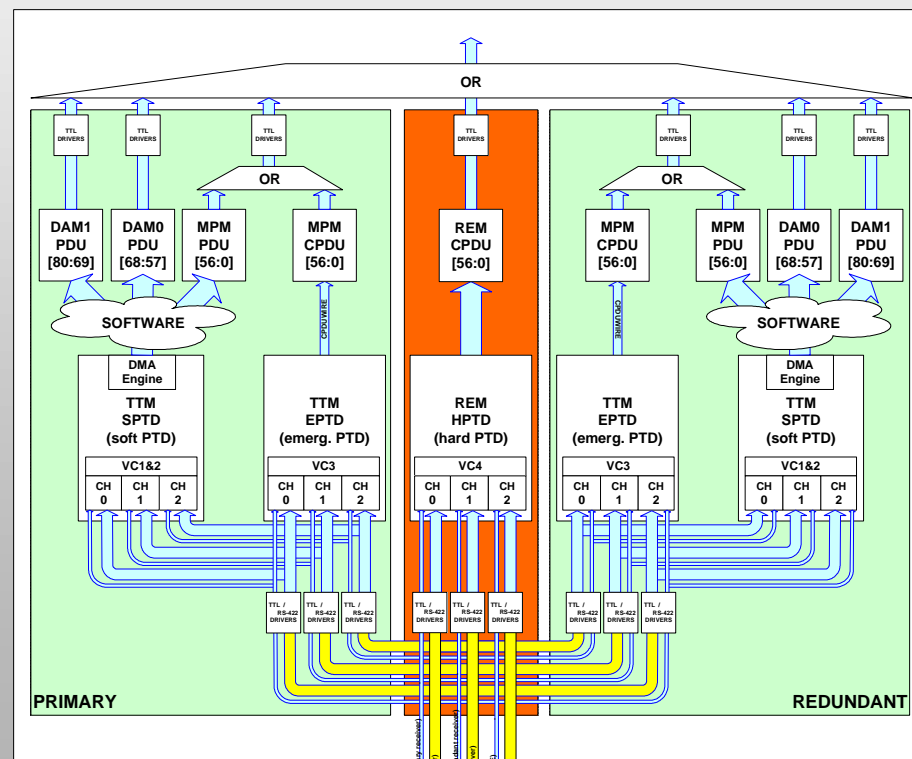


Software packet telecommand decoder

Having a H/W recovery TC decoder, the need for a full blown hardware TC decoder in the nominal and redundant lanes might not be so strong. Since the recovery TC decoder is 'hot' and since the nominal and redundant lanes have a limited emergency TC-decoder in hardware, this requirement is no longer needed for the nominal TC decoder. Therefore this nominal TC decoder can be implemented in software.

The benefits:

- the protocol can be changed to future versions without hardware redesign
- Authentication can be added in software
- Additional VC-ID's can be easily added
- Additional MAP-ID's can be easily added
- the (hardware) failure rate decreases since less logic is needed
- no large FPGA needed anymore
- no PROM needed anymore
- no radiation-hard static RAM needed anymore
- the power consumption is reduced
- virtually no extra power required since the processor performance needed is less than 10 KIPS

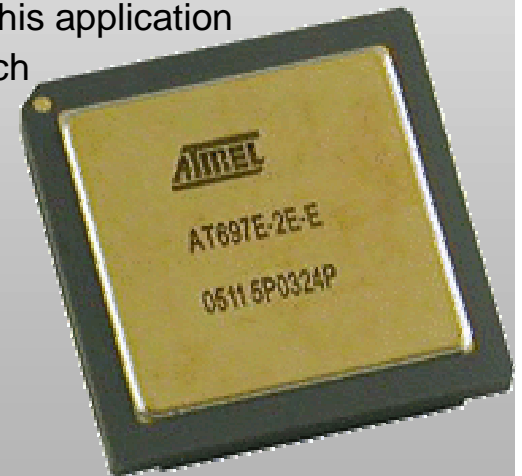


A new processor

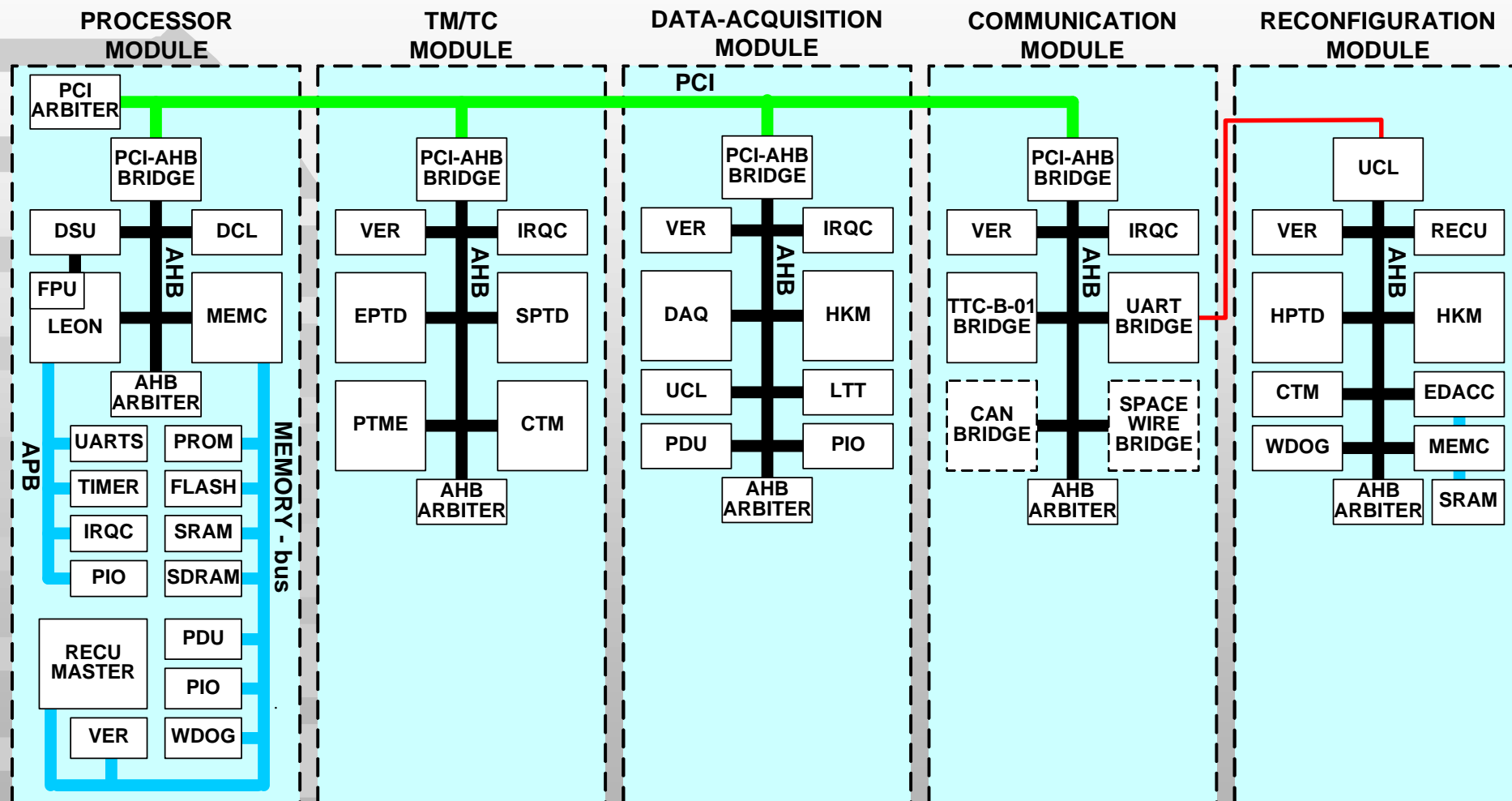
A trade-off was made between LEON2 and LEON3 in both FPGA and ASIC implementation.

Where the LEON3 (implemented in an ACTEL RTAX2000 FPGA) gives slightly better performance than the former ERC-32. For this project there was a need to demonstrate high computing performance. Therefore the LEON2-FT (AT697 from ATMEL) has been selected. It has a superior performance with respect to its successor the ERC-32 not only because it can run at a higher clock frequency but especially because of the following key-features:

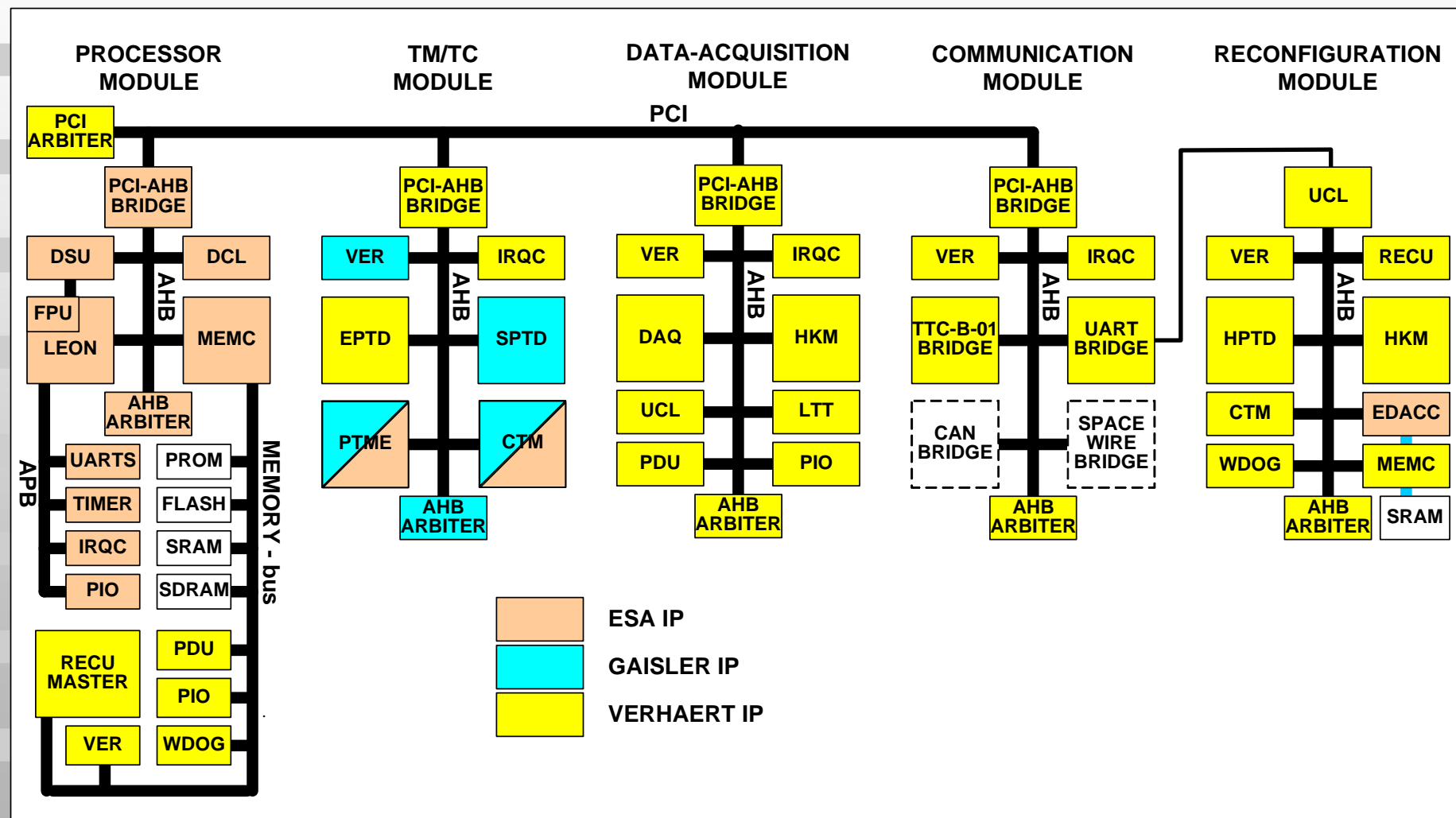
- The **on-chip PCI host bridge** makes the connection to a high throughput PCI backplane straightforward
- The availability of a **powerful debug support unit** made it very suitable for this application
- The LEON **supports** via its PCI-target interface **direct memory access** which allows the onboard software to concentrate on its processing tasks while all data movement is done with a **minimal software interaction**
- the **high clock frequency**
- the **7-stage pipeline**
- the **data- and instruction cache**
 - less sensitive to slow memories
- the **little power consumption.**
- the **SDRAM memory controller**
 - **large memory footprint** for minimal board space and little power consumption



ADPMS Chip Design



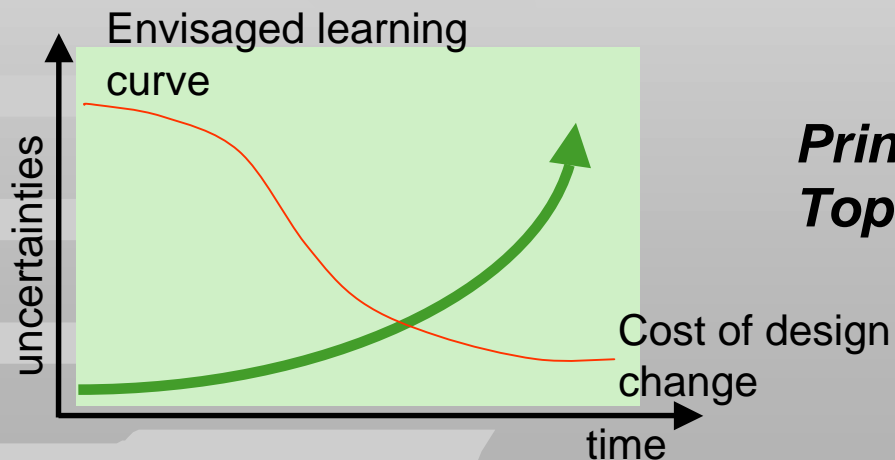
ADPMS Chip Design (2)





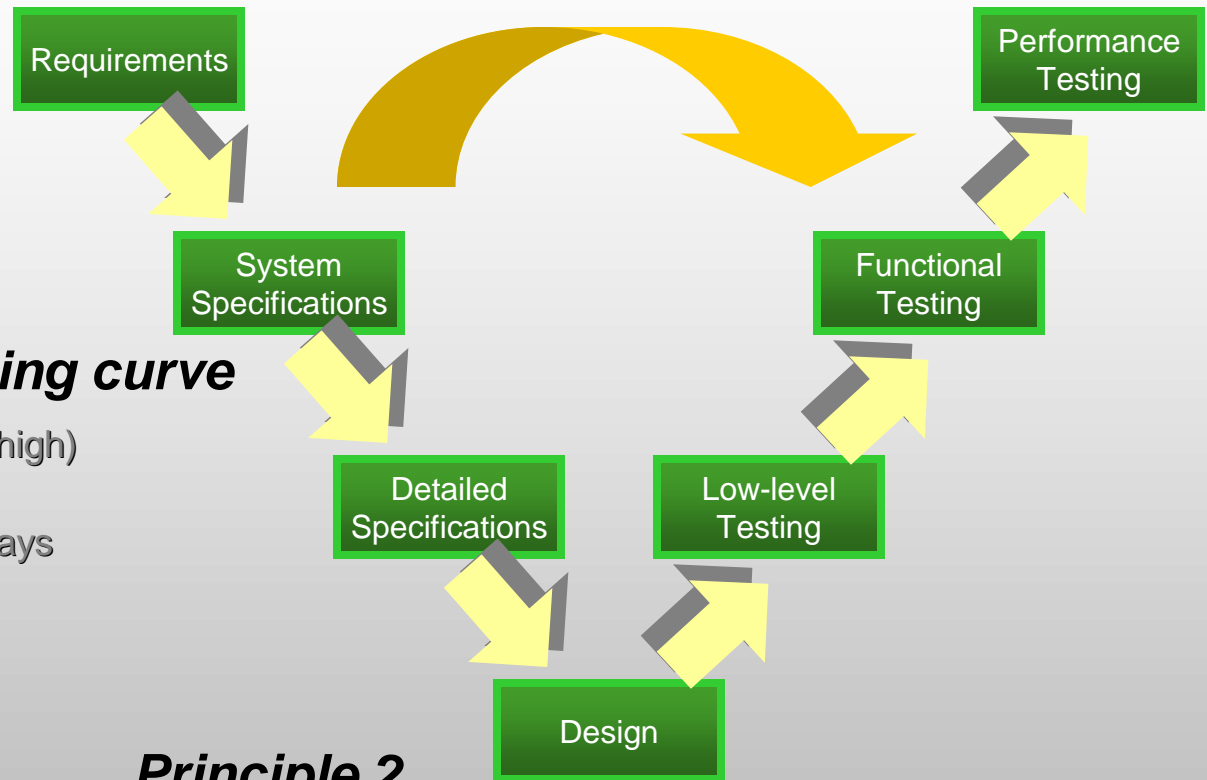
Principle 1 *Turning around the learning curve*

- Virtual testing prohibits *unexpected* (high) costs at the end + *planning* delays
- Virtual testing = an investment that pays off in one project

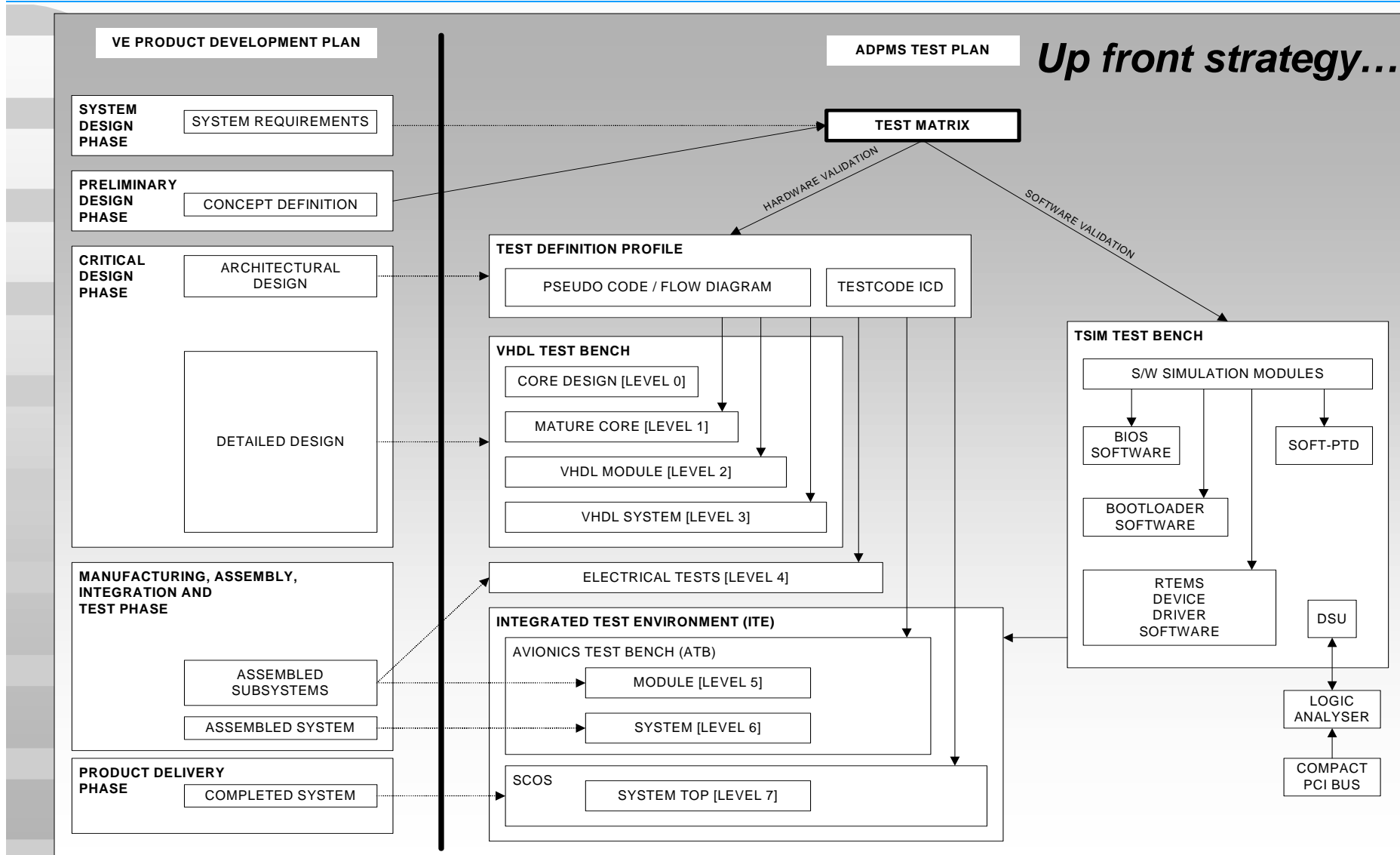


Principle 2 *Top down specification, bottom up testing*

- The V-model allows to test and re-test all functionality in an efficient way.
- V-model approach = an investment that pays off in one project



Validation Approach (2)



Validation Approach (3)

An integrated test environment...

Spacecraft Debugger Control System
Pentium IV PC
LINUX SuSE



Spacecraft Operator Control System
ULTRA-SPARC WKS
UNIX

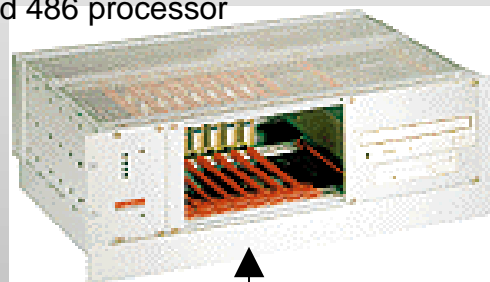


LAN

Avionics Test Bench (ATB)
2 Embedded Pentium III processors
RT Linux



Test Interface Bridge (TIFB)
1 Embedded 486 processor
RT Linux



Power Test Equipment
Hewlett packard



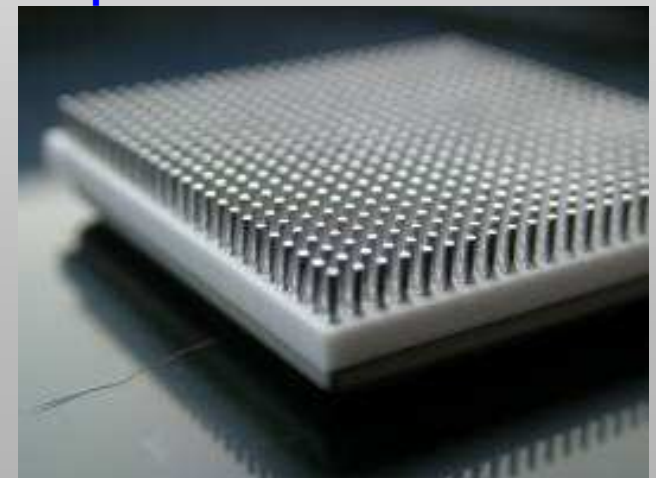
GPIB

ADPMS
Rtems or
VxWorks



Herewith an shortlist of the most important problems encountered during the ADPMS development

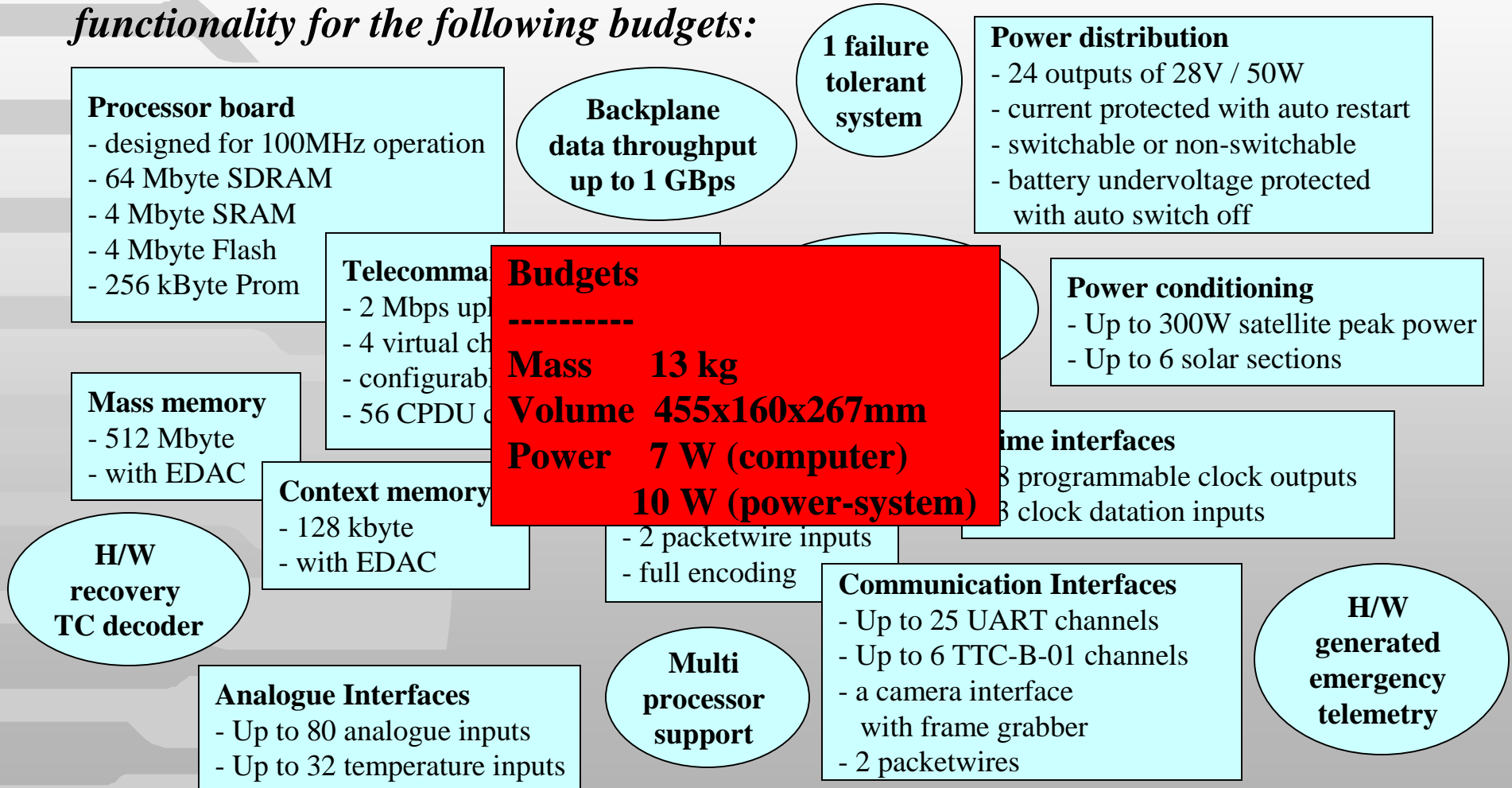
- Achieving the PCI I/O timing in an ACTEL RTAX2000 FPGA
- Finding a low voltage DC/DC converter with good efficiency
- Estimating the power-consumption of ACTEL RTAX2000 SoC designs
- Qualifying the reflow-process for a 624-pin CCGA for use in space
- Qualifying the pcb-process for a 324-pin MCGA for use in space
- Soldering RoHS compliant parts



ADPMS The Result



The ADPMS configured for the Proba-II satellite offers the following functionality for the following budgets:



ADPMS Key features

High performance

- 100MIPS LEON processor
- 1Gbit/s high throughput backplane
- 4Gbit mass memory (easily expandible)
- 100Mbit/s downlink capability

Low power consumption

- low power, low voltage components (3,3V & 1,5V)
- utilisation of large radiation tolerant FPGA's

Miniaturised avionics (mass & volume)

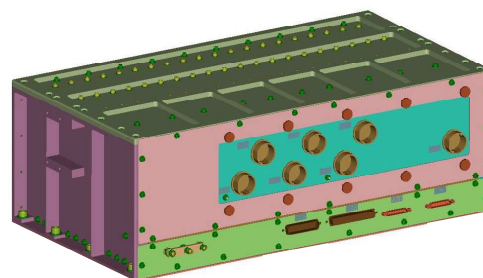
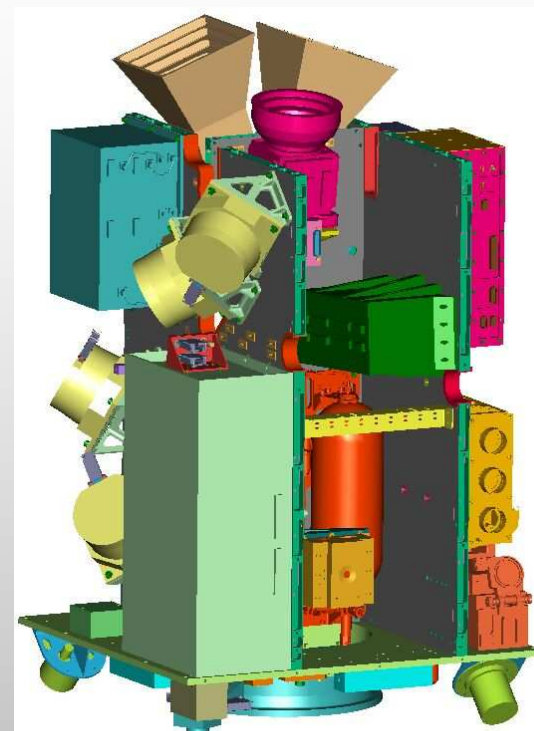
- Optimal highly integrated housing design
- Qualification of new high pin-count packages (CGA)
- 99% surface mount technology (SMD)

Easy satellite integration

- Easy test access guaranteed after S/C integration
- Open architecture (\leftrightarrow black box design)
- Improved testability
- Thermal control fully passive

Growth potential – High re-use factor

- High throughput backplane
- Multiprocessor support
- Modular & scalable design



The team

The ADPMS development has been carried out by

Verhaert Space a leading Belgian small space systems company.

With a track record of more than 30 years Verhaert Space develops advanced small space systems for agencies, large systems integrators and governments. Ranging from advanced small satellites, advanced space mechanisms & structures, and instruments & facilities for micro gravity research in manned and unmanned missions.

But could also be realised thanks to a good support from ESA and ATMEL

Mr. André Pouponnot, Mr. Roland Weigand, the PROBA-project team and Mr. Nicolas Renaud

And by a teaming with some renomated experts in their specific field

- GPV Printca A/S (DK)
- Spacebel (B)
- Gaisler Research (SE)
- Spur Electron Limited (UK)



Thank you for your attention

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