Integrating Additional Functionality with APS Sensors

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Introduction

- Optical / image sensors for GNC see a move from CCD to CMOS Active Pixel Sensors (APS)
- ***CMOS APS provide the potential for integration of analogue, logic, and system functions on single chip***
- High level functional integration on chip raised many feasibility questions.
- **FillFactory / Cypress have completed the LCMS Technology demonstrator under ESA contract 17235/03/NL/FM to address these.**
- Final presentation 10th March 2006

Rationale for integration (1)

- Benefits of on-chip integration at unit level?
  - dimension / mass / cost reduction (fewer parts)
  - power reduction and reliability improvements
  - Easier, quicker and cheaper unit integration
    - eliminate FPGAs, amplifiers, line drivers, thermistors, ...
  - Exploitation of design methodologies not applicable to board-level design
    - automated testing
    - self-test
    - dynamic power management
    - ...
    - → see highly-integrated battery-powered consumer applications (PDAs, MP3s, mobile phones, ...)

Rationale for integration (2)

- Benefits on system level?
  - Miniaturized low power sensors are enabling technologies for micro- and nano-satellites and intelligent landers
  - Enabling technology for use of multiple sensor suites
    - for given mass / power / cost budget
    - Improved redundancy and robustness
    - Fewer blinding/ dead zone problems – simplified control logic
    - fusing multi-source data in enhanced-accuracy position determination
  - Lower unit costs, lower launch mass

Integration Risks and Mitigation

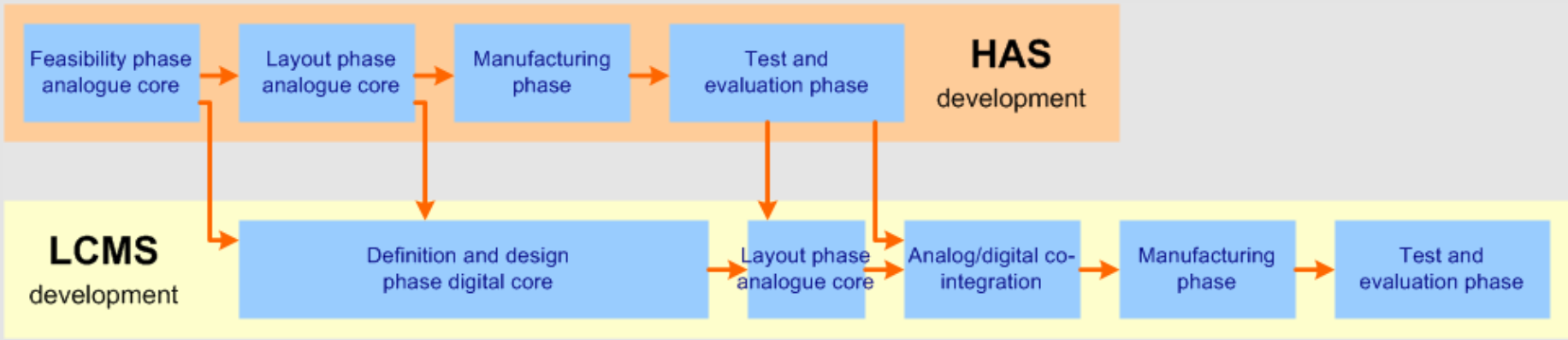
- logic switching noise
  - impacts on electro-optical signal, at pixel site or later
  - couples through die substrate
  - couples through shared power supply
  - → careful spacing / guarding of blocks, synchronous design
- power dissipation of extra functions
  - increased die temperature, thermal gradients
    - increased pixel dark current + noise
  - → advanced power management techniques
- reduced flexibility
  - design decisions ‘carved-in-silicon’
  - → programmability, even of hardwired logic
- Radiation Tolerance with increased processing
  - → RT design rules for pixels and analogue (Fillfactory patent)
  - → Triple redundancy for all flip flips
  - → EDAC and memory scrubbing for all memories
  - → Use of existing radiation hardened IP cores

LCMS Functional Requirements

- **Idea: Star Tracker Optical Head ‘on a chip’ demonstration**

- Full-frame images every 200 ms (acquisition mode)
- 20 Windows of up to 20x20 pixels every 100 ms (tracking mode)
- User programmable windows (size, position, gain, offset, threshold, integration time…) - *for each window !*
- Simple dynamic user programming
- Processing: reject non-star signal
  - background level estimation and subtraction
  - pixel signal thresholding
  - On chip full correlated double sampling (removes Fixed Pattern Noise)
- 12 bit ADC
- Autonomous operation: clock + command in, data out
- Fully integrated easy to use interfaces options
  - SpaceWire / IEEE1355
  - universal serial
  - parallel bus
- Digitisation of on chip temperature sensor and 4 external analogue inputs
- Single supply, 3.3V

Development logic – how to do it cheaply!



One contract, two chips

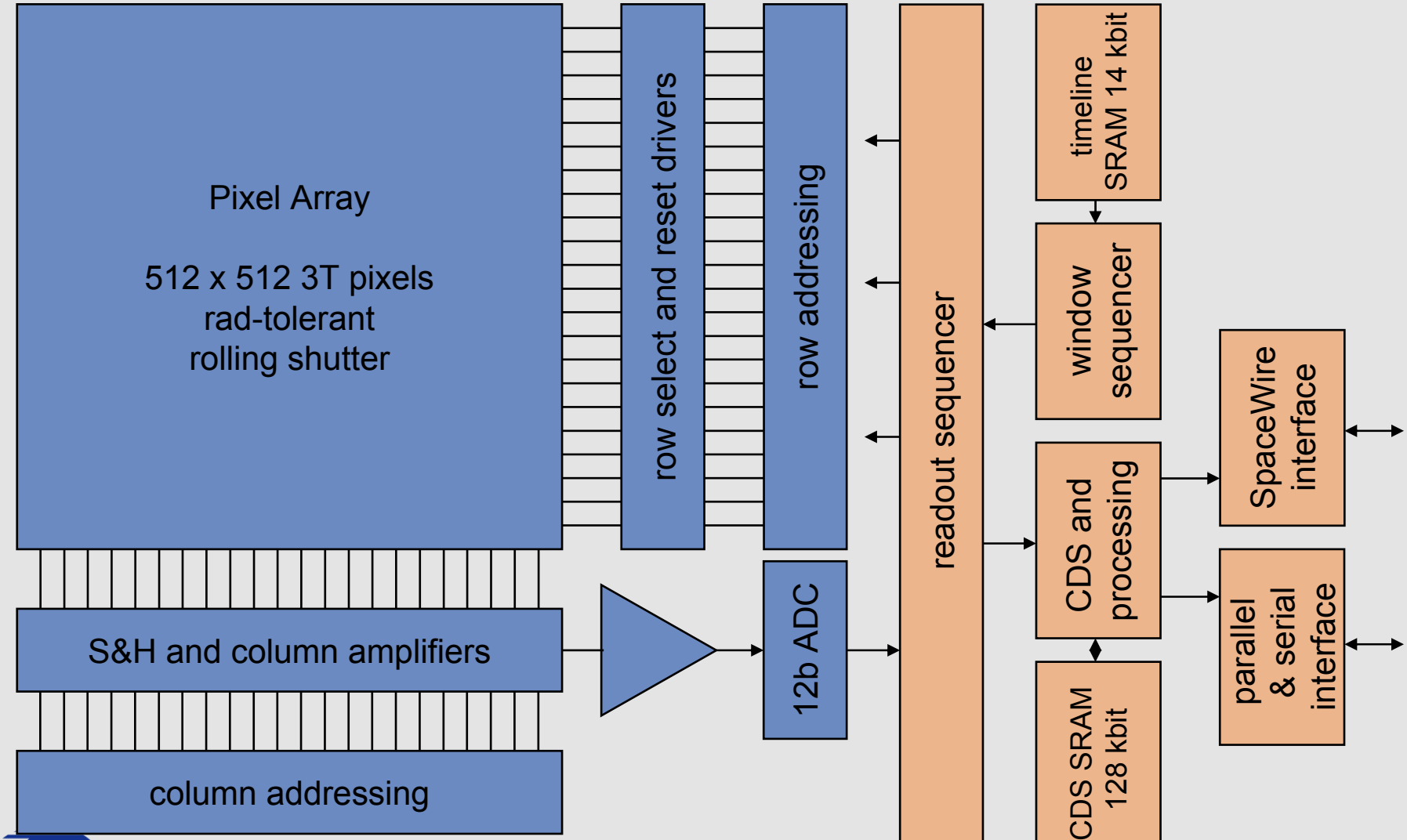
- HAS (High Accuracy Startracker) established analogue architecture
- LCMS (Low Cost and Mass Startracker) image sensor core is scaled HAS sensor
  - 1024 x 1024 → 512 x 512 pixels
  - 18 x 18 → 25 x 25 um pixel size
- HAS Silicon + FPGA used for LCMS logic pre-validation

CMOS process/fab choice

HAS: optimal performance → X-Fab .35

LCMS: minimal design risk → AMIs .35

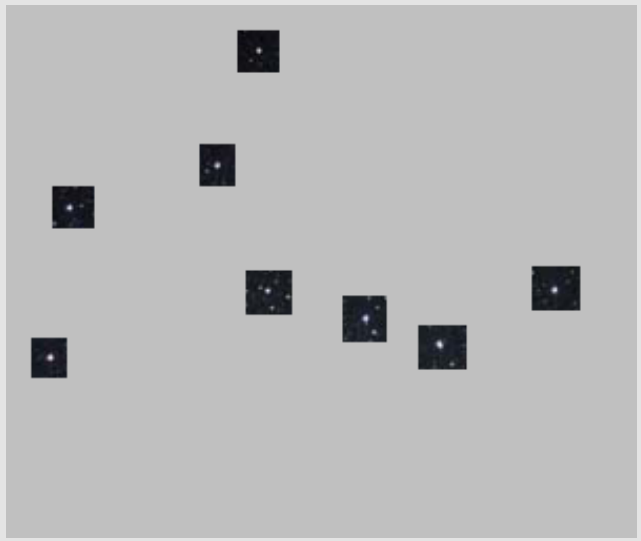
LCMS Block Diagram



LCMS Readout Sequencers

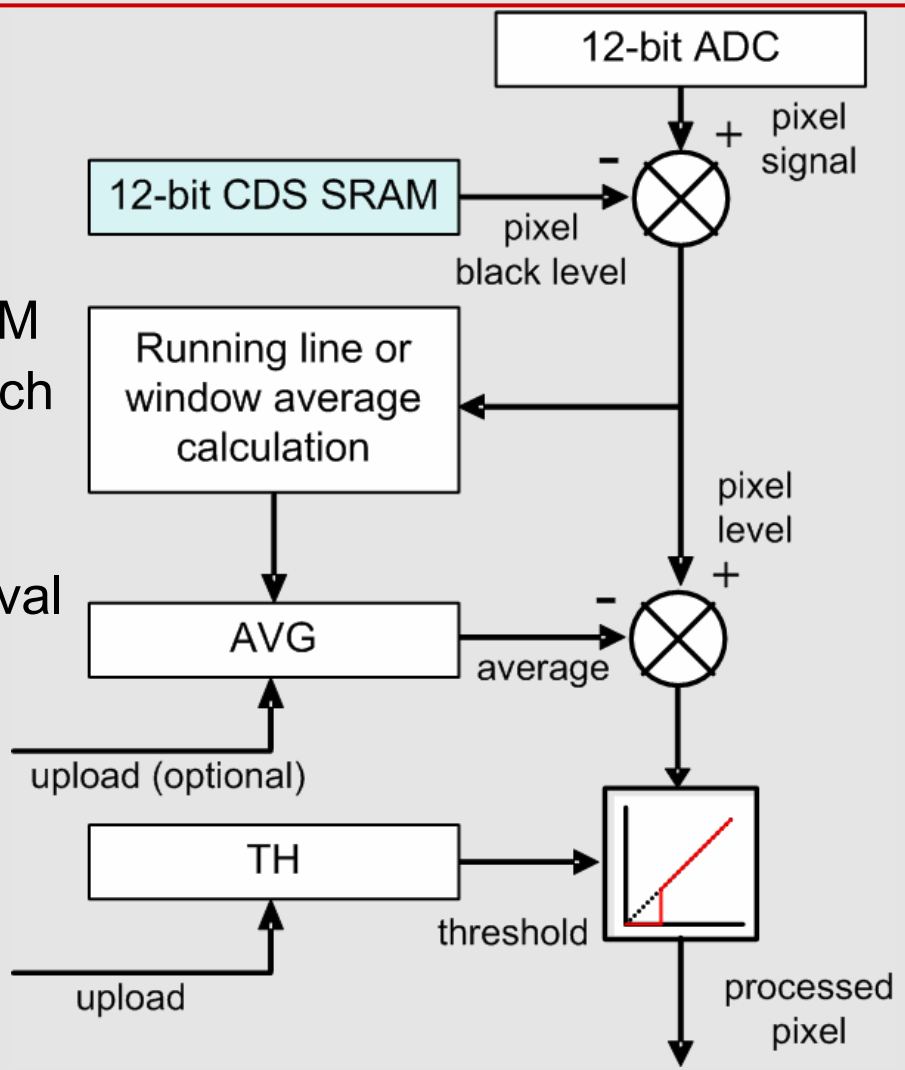
- Low-level sequencer
  - Controls analogue core
- High-level sequencer
  - Full frame readout with Rolling Shutter and Double Sampling
  - Windowed readout with Correlated Double Sampling

- Windowed readout timeline
  - programmed into on-chip SRAM memory
    - 8 kbits
    - 1023 program steps/ 100 ms ‘frame’
  - per window
    - position in FOV
    - PGA gain and offset
    - when to reset
    - when to read post-reset levels
    - when to read post-exposure levels
  - → very easy to set-up on-the-fly



LCMS CDS and Pixel Processing

- **Correlated Double Sampling**
  - digital domain
  - suppresses kTC noise and FPN
  - stores black / reset levels of 20 windows in 128 kbit on-chip SRAM
  - calculates (exposed-initial) for each pixel in output windows
- **Data processing**
  - background estimation and removal (technique depends on mode)
  - signal thresholding
- **Data output format**
  - contiguous, per window
  - no data re-ordering required



LCMS Interfaces

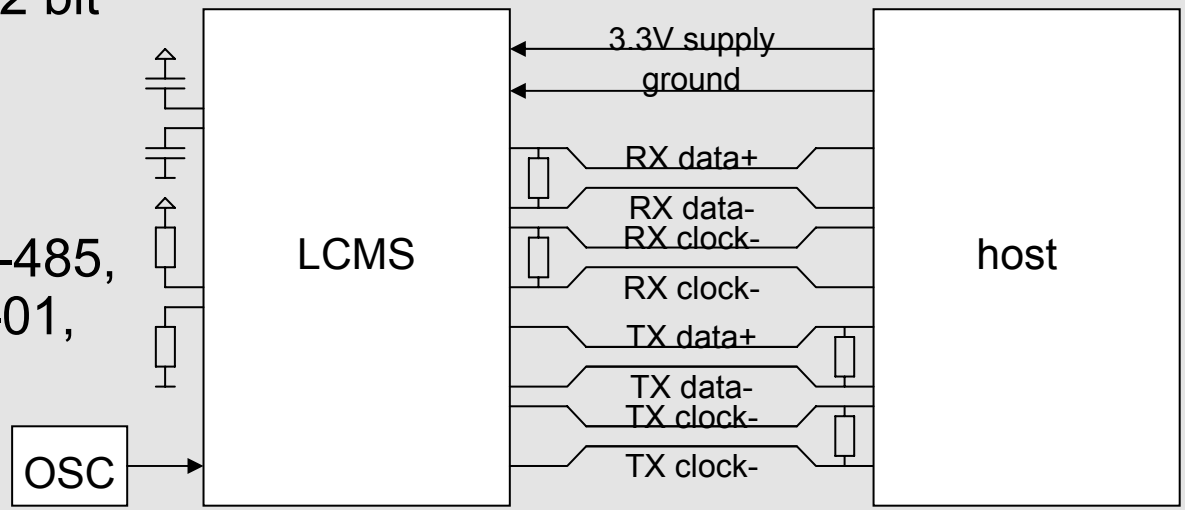
- SpaceWire
  - command and data
  - 5 full frames / s @ 12 bit / pixel
- Parallel
  - command and data
  - compatible IDT 72V2113–style FIFOs
  - 9 full frames / s @ 12 bit / pixel
- Serial
  - command only
  - various formats (RS-485, PacketWire, TTC-B-01, ...)

•Implementation:

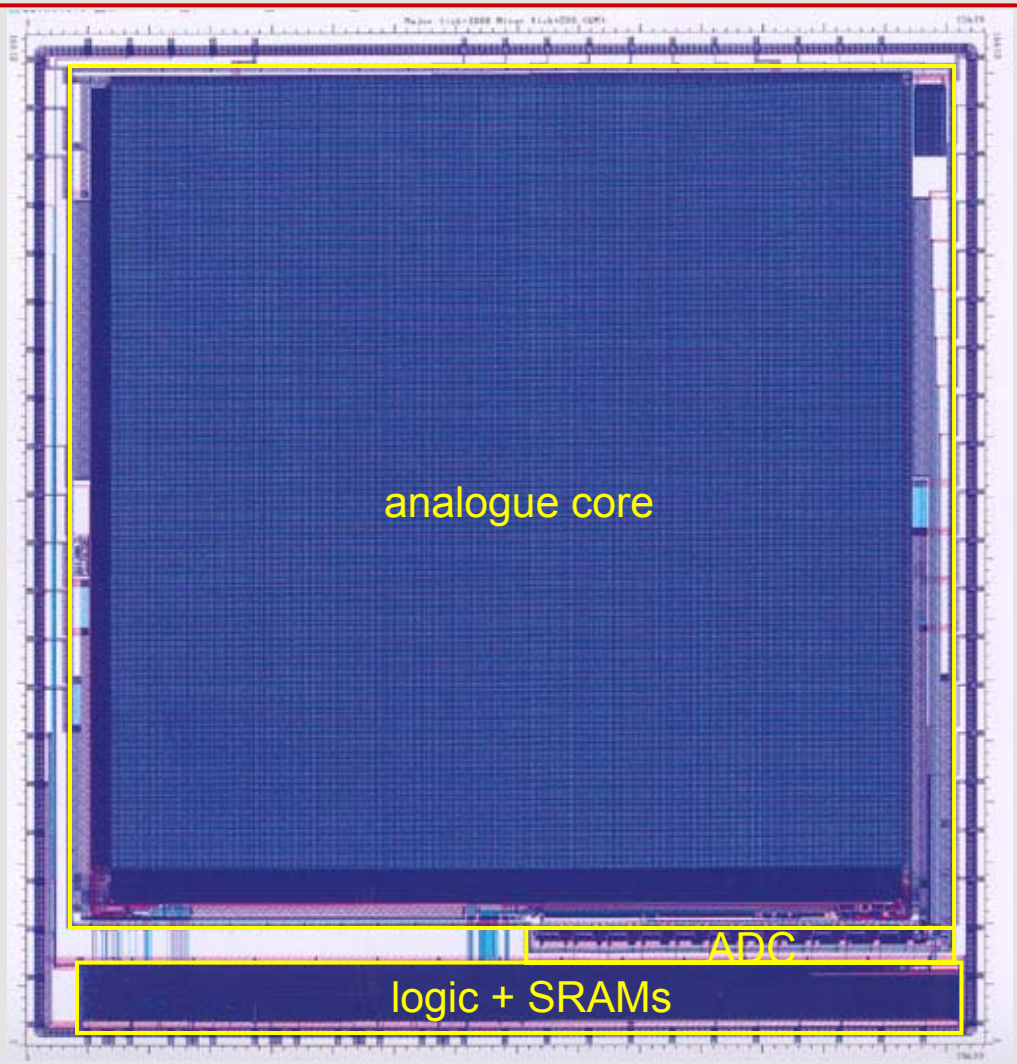
•3.3v power supply

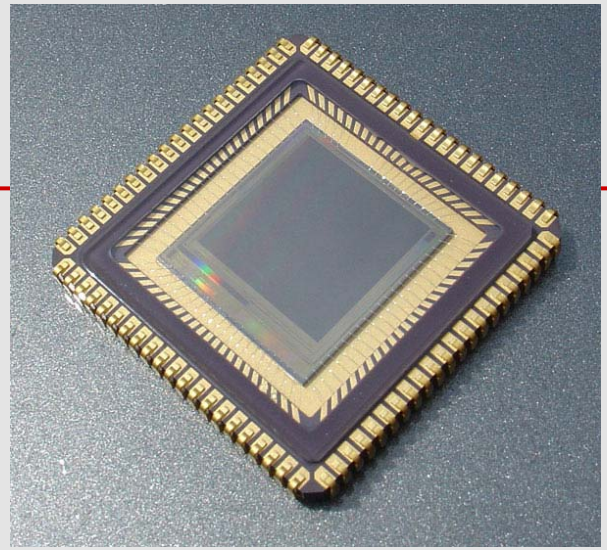
•20MHz oscillator

•Minimum number of external references – easily obtained by resistor network.



LCMS Physical





- Package
  - ceramic JLCC-84
- Bond options
  - 84 pin package ⇔ 94 pin design
  - LCMS-C: CMOS i/f options
  - LCMS-L: Spacewire only

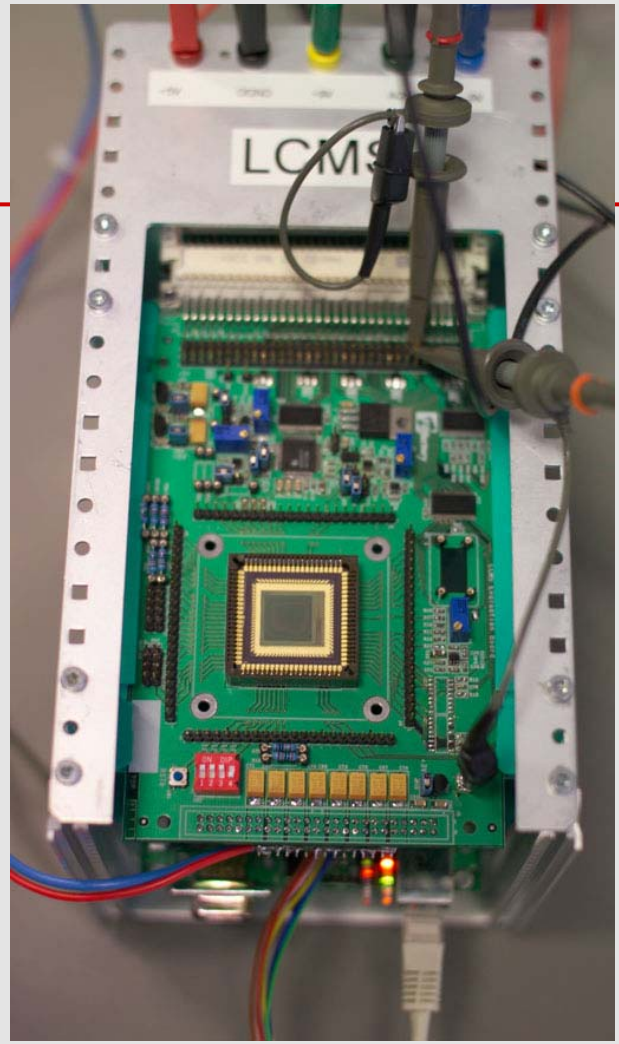
LCMS chip dimensions
-X: 15.5 mm
-Y: 16.2 mm
-Area: 251 sq.mm

Silicon Results

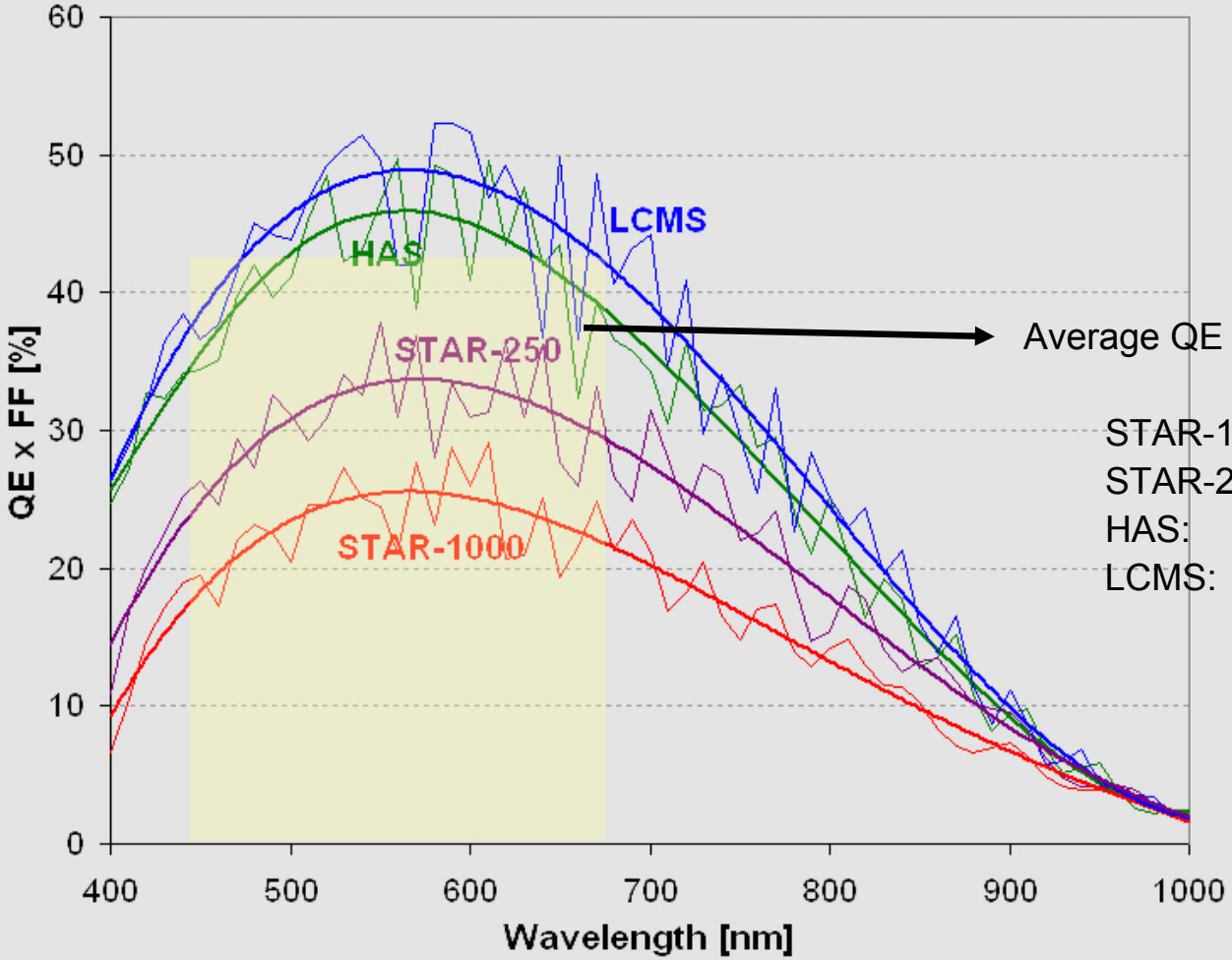
- Fully functional from first silicon

- Functional, performance and limited radiation testing performed
- No measurable additional noise effects.
- All functionality working as designed

parameter	result	Units	Remarks
Dark Current, 25C	1000	e-/s	after 21.5 krad
DCNU, 1sigma (dark current non uniformity)	100	%	after 21.5 krad
Read Noise, 1sigma	60	e-	after 21.5 krad
FPN, Full frame mode	85	e-	after 21.5 krad
FPN, windowed mode	19	e-	after 21.5 krad
PRNU (photon response non uniformity)	<1.4	%	
Full well capacity	85000	e-	
Fill Factor x Quantum Eff.	48	%	Peak at 600nm
Power, **full speed**, EOL	164	mW	CMOS mode
	226		LVDS mode



Spectral Response – FF x QE



Average QE x FF for [400 – 720 nm] range:

STAR-1000:	22 %
STAR-250:	29 %
HAS:	40 %
LCMS:	43 %

Future Work (1) – near and medium term

- LCMS evaluation by ESA and European STR builders
  - on-going
  - in-flight demo expected

- 'LCMS2'
  - follow-up project, in funding and detailed definition phase at ESA
  - extend LCMS concept with:
    - object detection and aglomeration
    - Basic object filtering and centroiding
    - Large object edge detection and curve fitting
    - On the fly full image compression
    - Real time FPA SEU suppression
    - smaller pixels – easier optics
    - Improved, 12 bit accuracy ADC
    - Even more simplified electrical interface (fewer pins, removal of external references, further power reductions…)
    - …
  - Maintenance of full user configurability of all functions and parameters.
  - Aiming at fully qualified radiation hard product
    - Current ESA baseline for second-generation APS-based AOCS units in the next decade.

Future Work (2) – long term possibilities

- ‘Sensor-on-a-chip’ feasibility study
  - ESA contract 5135/06/NL/JA
  - partners Galileo Avionica, Alcatel Alenia Space, BAe Systems
  - explore present and future limits of integration
    - Processor, NVM and RAM
    - DC-DC convertor, clock generation and all auxiliary functions
    - package miniaturisation and thermal self regulation
    - optics miniaturisation (MEMS, ...)
    - ultra-low-power
    - ultra-low-mass
    - wireless interfacing
    - ...
  - Identify uses, system level problems and key budgets
  - Determine development costs (Very High!!) and recurring costs (rather low)
  - Initial results indicate 20 - 50g, 0.1watt sensor may be feasible with some provisos (e.g. power supply voltage)

Limits of integration

- Integration on chip has many potential benefits **BUT** many difficult issues:
- Non-technical issues
  - Industrial issues… (many of them!)
  - IPR issues
  - Product flexibility
  - Non recurring development costs (exponential with complexity)
- Technical issues
  - Compatibility of required CMOS processes with image sensors (multiple metal layers, high voltage and wireless support -> poor dark current characteristics)
  - Radiation hardening and electrooptical characterisation of new CMOS processes
  - Clock, power and cross talk management
  - Fault and problem identification and resolution
  - Configurability management
  - Testing complexity !!! (Do not underestimate!)
  - Assembly and alignment issues

Conclusion

- LCMS provided a clear and successful demonstration of functional integration on image sensors.
  - Fully proven integration of:
    - readout & interface logic
    - pixel processing
    - memories
    - SpaceWire
    - LVDS IO
    - temperature sensor
  - Demonstration that integration can be done with no negative impact on noise, power, ...
  - Demonstration (by design and partial testing) that radiation issues can be handled.

- Further on chip integration provides the most promising path to AOCS sensor improvements in the future (e.g. lower mass, power and cost with higher reliability)