The new SpaceWire compliant SMCS332SpW / SMCS116SpW ASIC

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Outline

- **Introduction**

- **Motivation for the new SMCS**

- **SMCS332SpW   New Features / Functions**

- **SMCS116SpW   New Features / Functions**

- **Serial Transfer Universal Protocol (STUP)**

- **ASIC Facts**

- **Status**

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Introduction

SMCS   (Scalable Multi-channel Communication Sub-system)

- communication controller ASIC
- for space applications (radiation tolerant)

Tasks:

- hardware supported execution of major parts of the inter-processor protocol
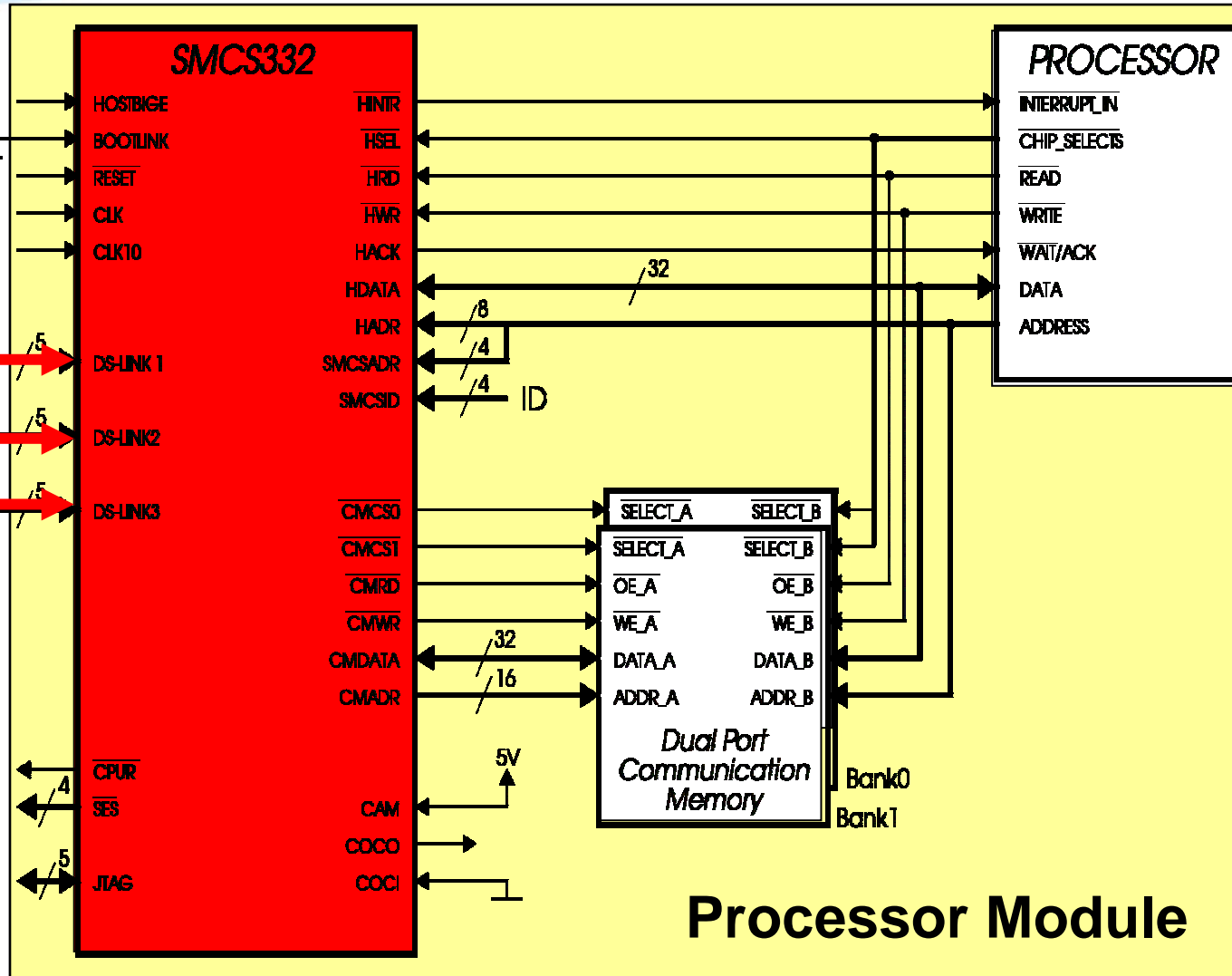- provide a fast interface to serial protocol

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Introduction – The current SMCS

Application of SMCS ASICS

IEEE 1355
or SpaceWire network

Memory 1

SMCS116

Sensor 1

SMCS 116

Sensor 2

SMCS 116

SMCS 332

SMCS 332

Processor

SMCS116

Memory 2
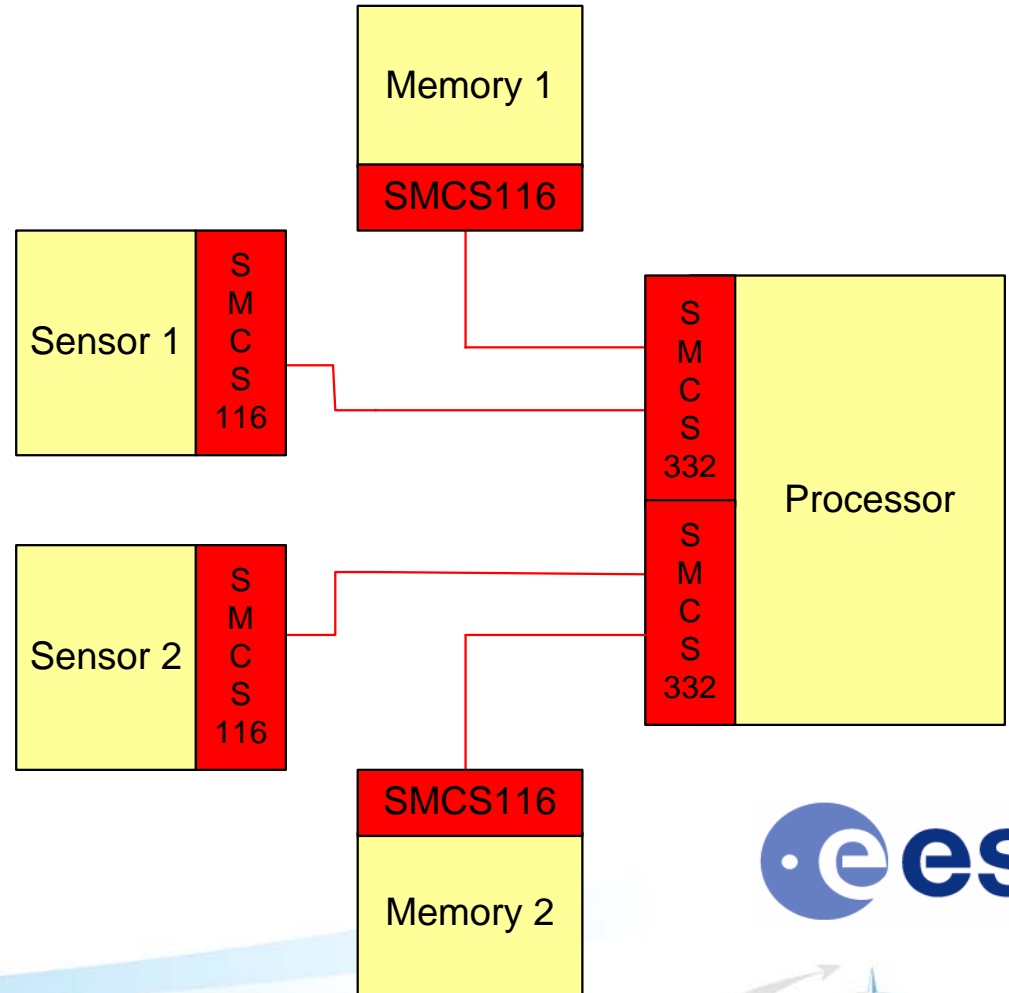
SMCS332 in typical environment

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SMCSlite Applications

SMCSlite connected to four banks of memory.
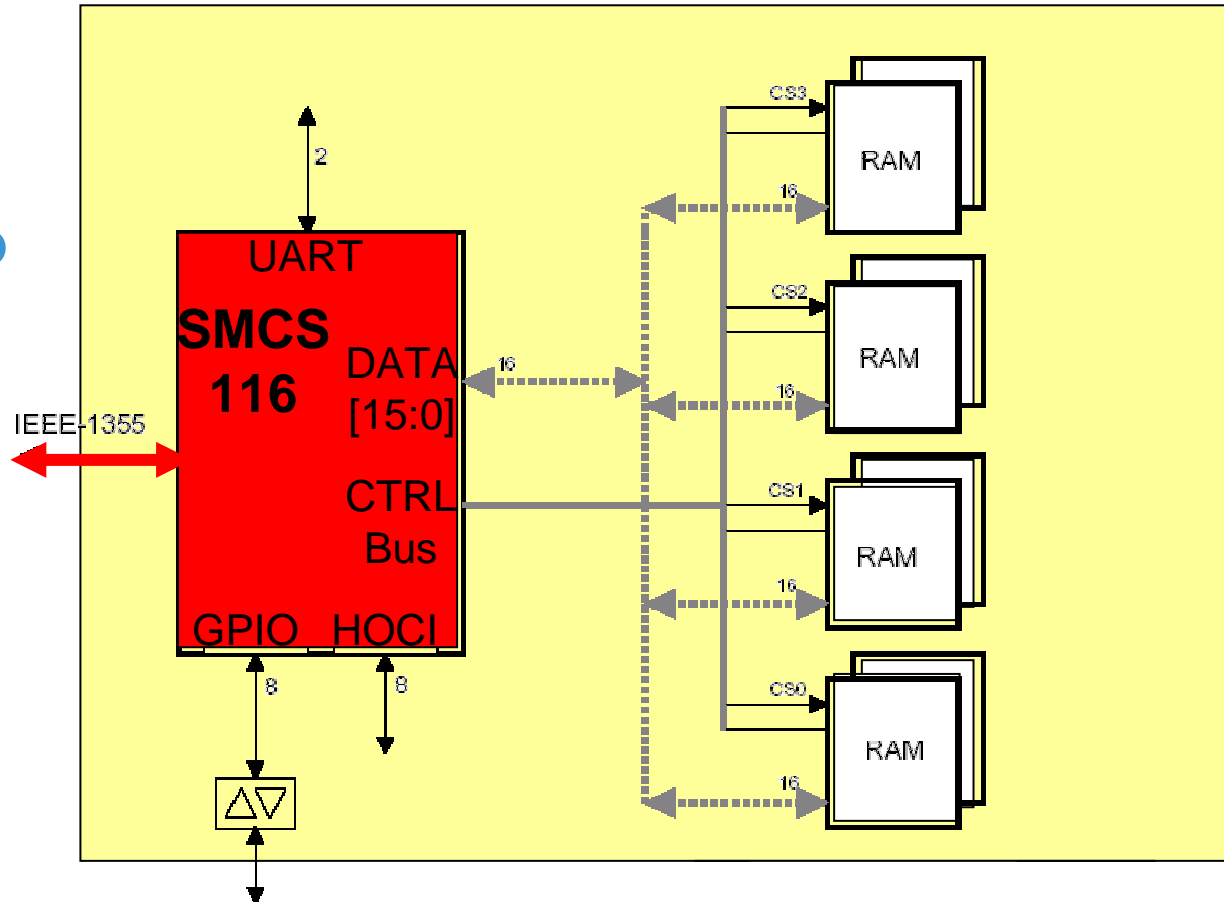
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SMCSlite Applications

SMCSlite as communication and system controller on an interface node consisting of an ADC and DAC.
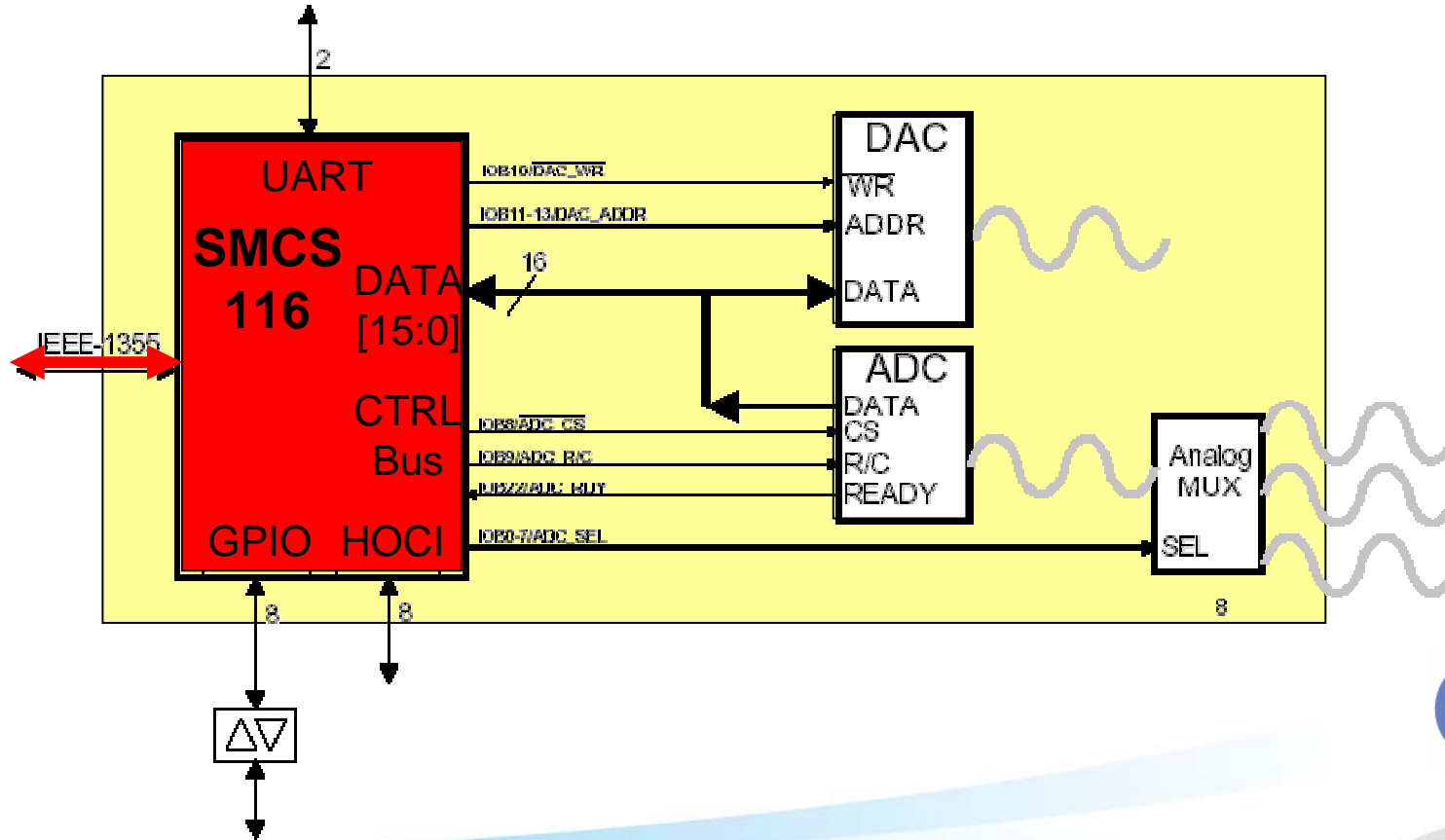
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Introduction - SMCS332

- **3 bi-directional link channels**
  each with DS macro cell,
  receive, transmit section,
  protocol processing unit

- **COMI:** Com Memory Interface
  performs autonomous accesses
  to the communication memory

- **HOCI:** Host Control Interface
  gives r/w access to config reg
  and to DS channels for the CPU

- **PRCI:** Protocol Command
          Interface
  collects commands from
  protocol units

- **JTAG:** Test Interface
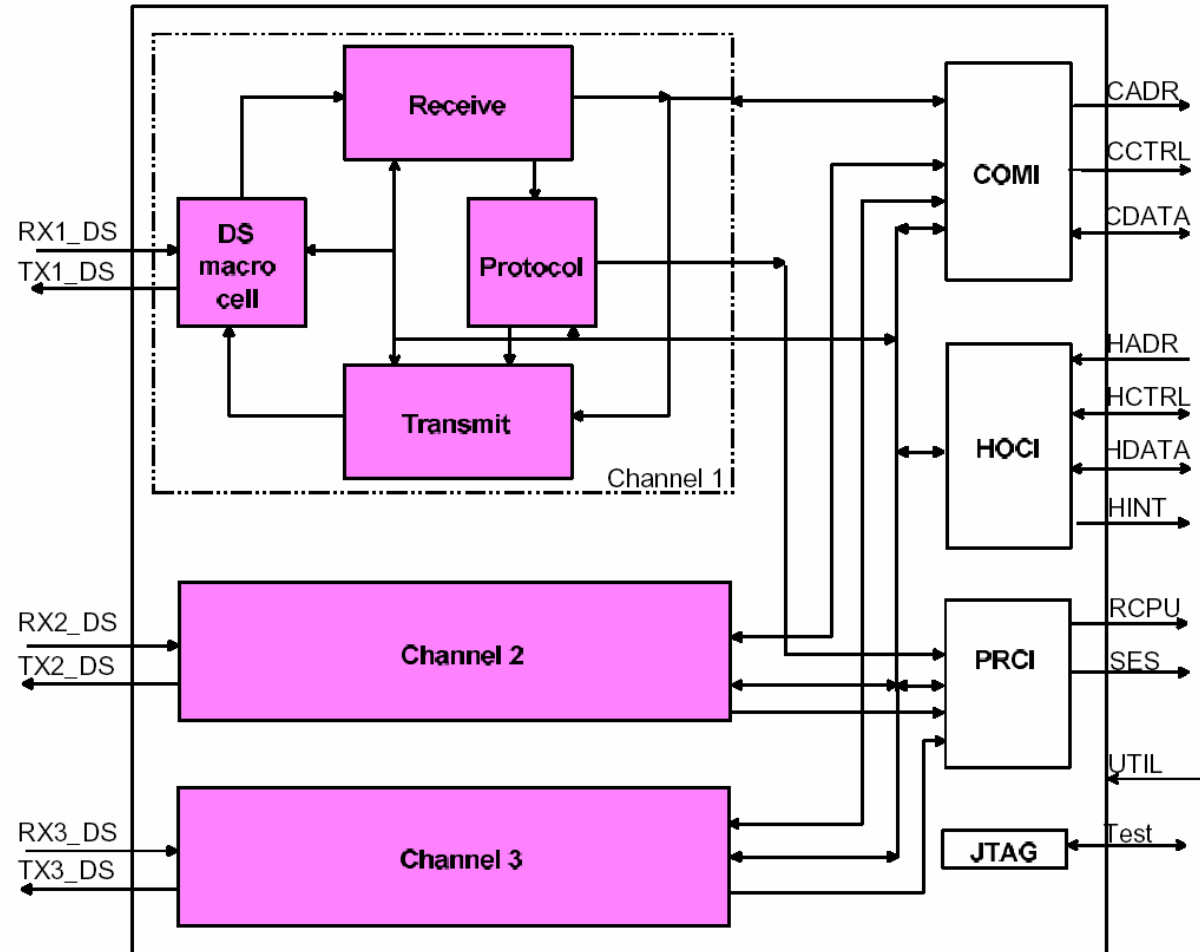
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Introduction SMCS116

Link Interface:

•Interface to serial IEEE-1355 link

•control by Link

Host Interface:

•parallel Interface for programming and controlling

ADC/DAC I/F:

•allows the read from ADC or write to DAC

RAM IF:

•4 banks (each 64K) of memory are addressable

FIFO I/F:

•small internal FIFO (passive mode)

•interface to external FIFO (active mode)

GIPO:

•General Purpose Interface, up to 24 I/Os

UART:

•2 independent UARTs

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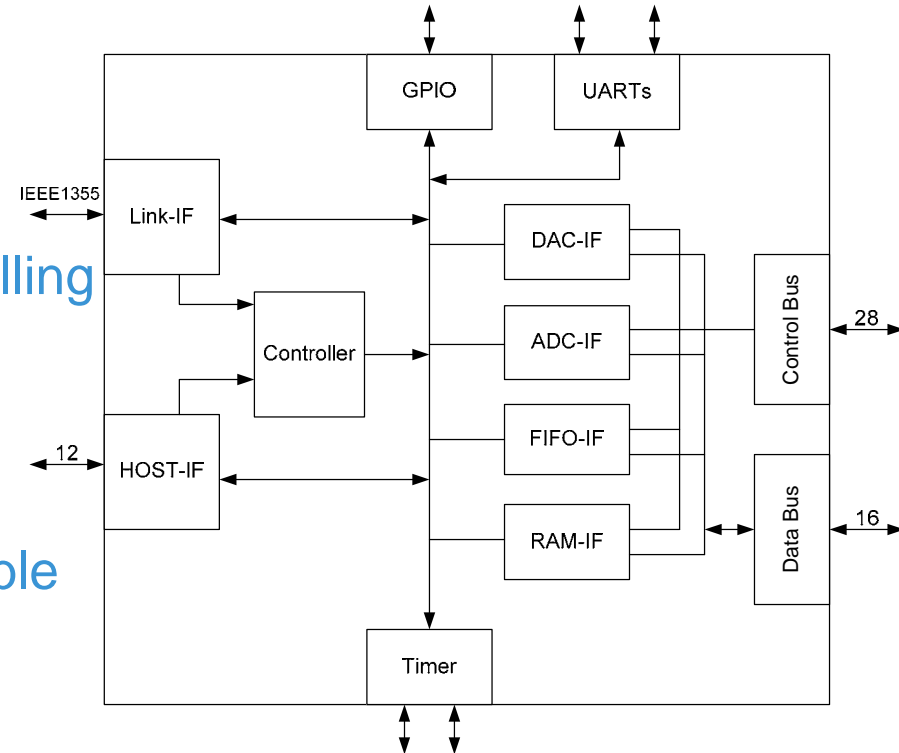
Motivation

Motivation for new SMCS SpW ASICs

- SMCS ASICs are often used communication controllers
- SpaceWire standard is becoming increasingly important
- ESA support

Requirements for the new SMCS SpW

- SpaceWire compliant (ECSS-E-50-12A, 24-Jan-2003)
- Pin compatible to existing SMCS332 / SMCS116
  - *not achieved completely*
- correct known anomalies of the existing SMCS ASICs
- Goal: Backward compatibility concerning software

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Advantages of SpaceWire

New Features due to the SpaceWire Interface:

- The new SpaceWire interface is resistant against simultaneous switching on the data and strobe inputs

- It is 'hot' plug able (no master-slave situation has to be arranged)

- The SpaceWire Interface transmits / receives the new time code characters

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SMCS332SpW - New Functions

- Time code
  - The SMCS332SpW can send Time Code characters
  - The SMCS332SpW can be used as Time Code master

- New header field control bit
  - more flexibility for packet generation

- Arbitrary packet length

- No restriction for the packet size for data reception/transmission over COMI

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SMCS116SpW - New Functions

- supports Serial Transfer Universal Protocol (STUP)

- enhanced 32-bit processor support
  - the protocol engine was modified that it tolerates and executes commands of any length
  - rest of a packet (read beyond 1 byte; write beyond 2 bytes) will be ignored

- Time code
  - The SMCS116SpW can send Time Code characters
  - The SMCS116SpW can be used as Time Code master

- FIFO, ADC and UART I/F improved

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Protocol handling

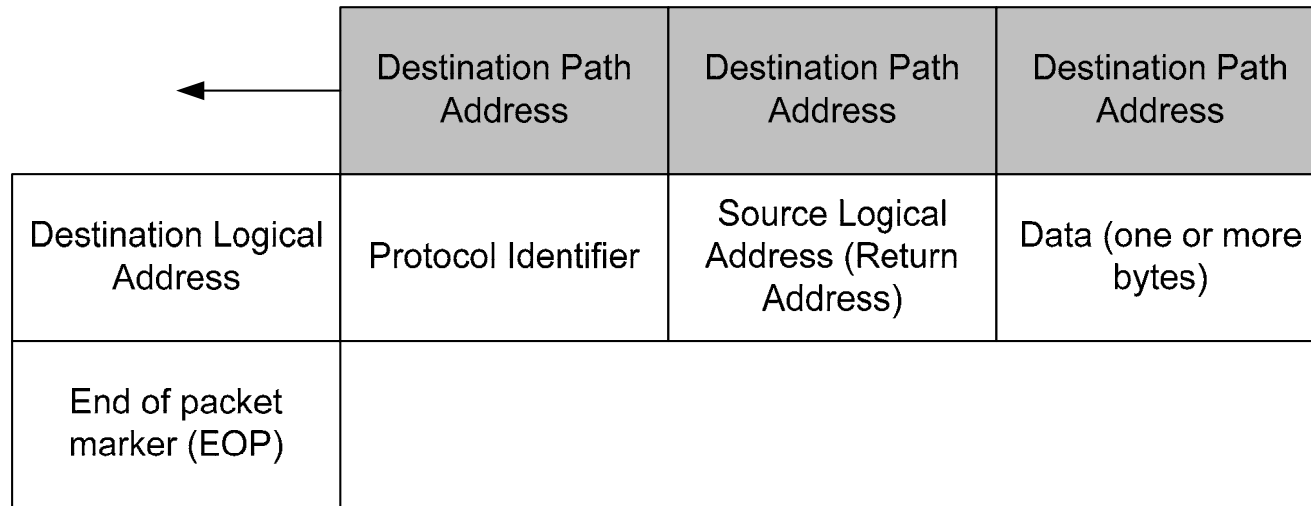- for SpaceWire a new protocol is defined

- SMCS332SpW
  - The SMCS332SpW directs all received data directly to the SW. Therefore, the SW has to handle the protocol and the SMCS332SpW is fully compliant to the new protocol.

- SMCS116SpW
  - The new SMCS116SpW is able to handle data transfers without protocol and is compliant to the new SpaceWire protocol by using the **STUP** protocol.

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Serial Transfer Universal Protocol

Protocol format

Destination Path Address	Destination Path Address	Destination Path Address
Destination Logical Address	Protocol Identifier	Source Logical Address (Return Address)	Data (one or more bytes)
End of packet marker (EOP)		

- **Destination Path Address bytes are optional**
- **This protocol structure can be used for all kinds of commands**

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STUP in SMCS116SpW

Command format for SMCS116SpW

Destination Logical Address	Protocol Identifier	Source Logical Address (Return Address)	Command/Address
Data (one or more bytes)	Checksum	Checksum	End of packet marker (EOP)

- Byte 4 defines the command and address (write or read).
- Two Checksum bytes are appended, if checksum generation is enabled
- Source Logical address will be used as return address for read replies

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ASIC Facts

SMCS332SpW

- **Radiation tolerant gate array technology from Atmel: MG2RT (0,5 µm)**
- **196 pins**
- **power consumption: 1,7 W**
- **3.3V version: 100MBit/s**
- **5 V version: 200MBit/s**

SMCS116SpW

- **Radiation tolerant gate array technology from Atmel: MG2RT (0,5 µm)**
- **100 pins**
- **power consumption: TBC**
- **3.3V version: 100MBit/s**
- **5 V version: 200MBit/s**

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ASIC Schedule

SMCS332SpW

- **Prototypes tested**
- **Prototype approval given**
- **ASIC available -> Atmel**

SMCS116SpW

- **Prototypes testing ongoing**
- **Prototype approval planned for end of March 07**
- **ASIC available in ~ Q3/07**

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