Reconfigurable Communication Experiment using a small Japanese Test Satellite

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Agenda

- Background and Motivation
- Objectives of the mission
- Reconfigurable Communication Equipment
- Configuration of onboard software defined radio
- (Heavy Ion test results of Virtex II pro)

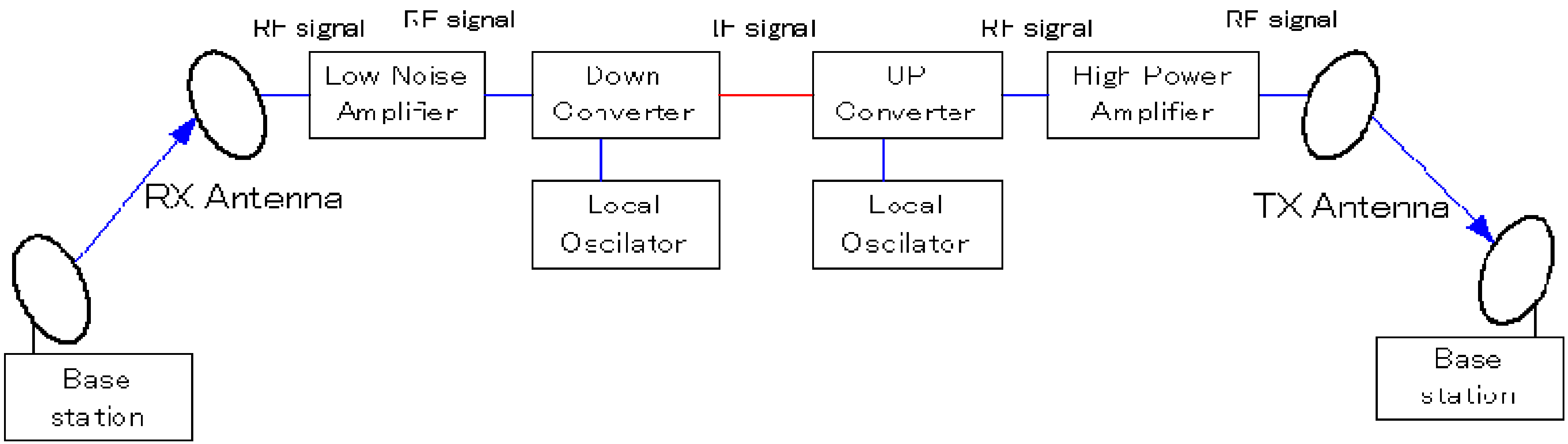
Background and Motivation

For next-generation satellite communications:

- Bandwidth expansion expected (HIGH data rate: more than 1.5 Mbps)
- Circuit switch -> Packet Switch

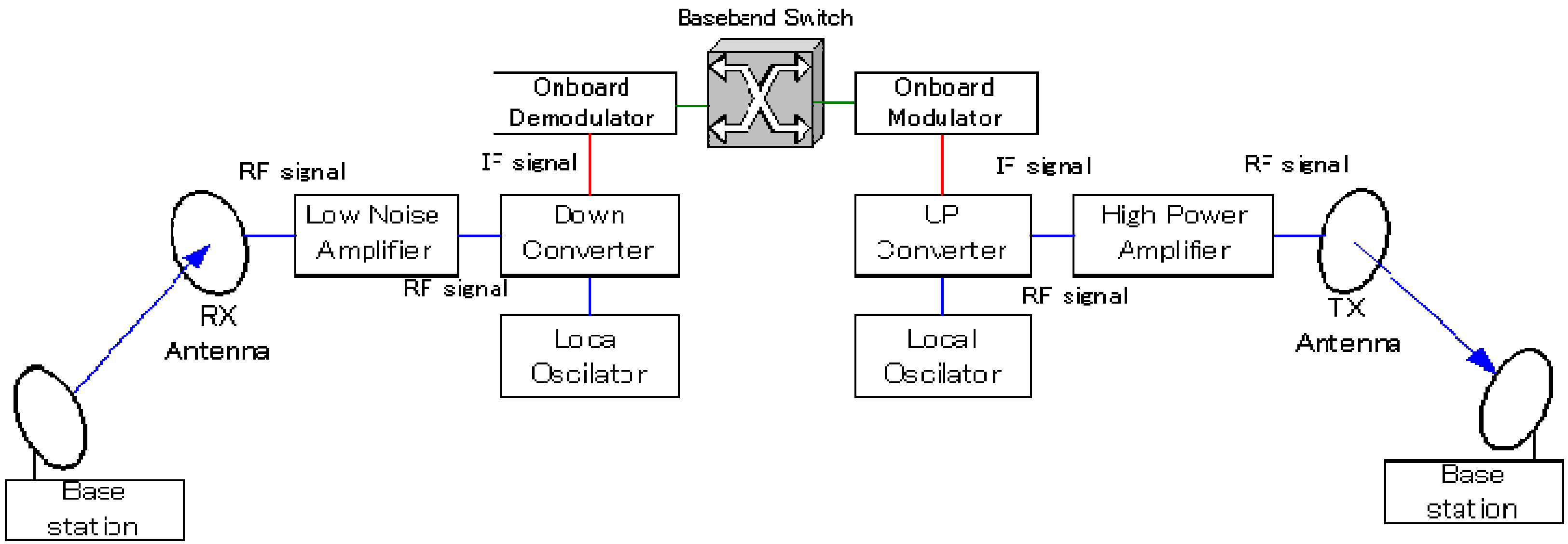
Regenerative relay + Onboard switching

Bent-pipe relay system



- Bent-pipe, through repeater, or frequency conversion (dumb hub)
- Most commercial communication satellite systems have this kind of repeater
- All signals received at the satellite are amplified and sent back to base station
- Supports Point-to-Point link

Regenerative Relay + Onboard Switching



- Full mesh network (Multi points-to-Multi points).
- 3-dB power gain
- Boost the total system bandwidth by the statistical multiplexing effect by using the onboard baseband switch
- Flexible link design
- Already been tested and demonstrated with experimental satellites
- Still few commercial satellites with this type of transponder

Issues (1)

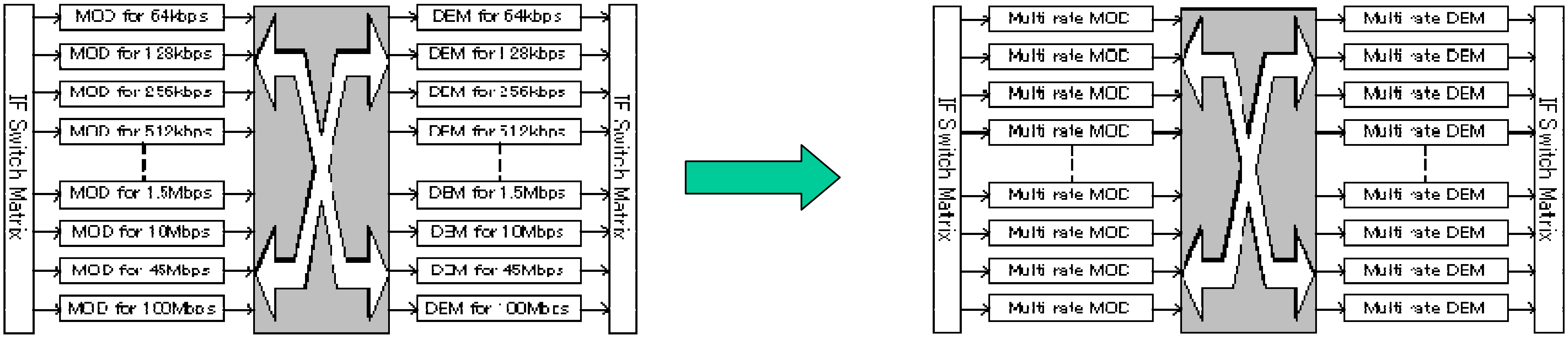
Recent communication satellite system: 10-20-year lifetime

- Can not come back from Geostational orbit
- Can not upgrade communication system installed in satellites
- Flexible link design, but system not flexible

Please imagine 20 years before communication system!

Acoustic coupler+RS232C+HDLC? (300 bps)

Issues (2)



Traditional Technology

- Many fixed-rate MODEMs
- Huge redundant system
- Test procedure complicated
- Heavy payload

Reconfigurable Techonology

- Many multi-rate MODEMs
- Simple redundant system
- Test procedure very simple
- Payload not so heavy

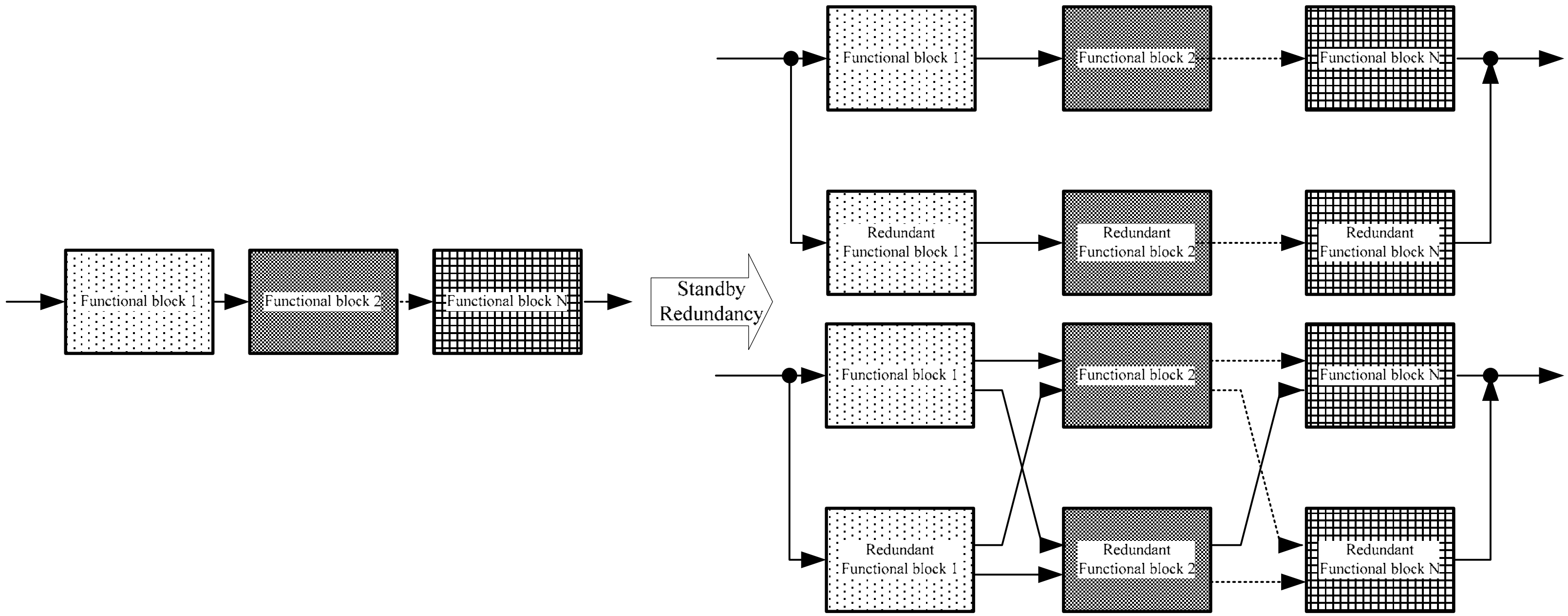
Objectives

1. Technological demonstration of onboard software-defined radio
   - Versatile onboard modulator and demodulator (MODEM) with SDR technique
   - application proof of highly functional onboard transponder for next-generation communication satellite
   - Adaptable to latest communications technology with flexible link design and high data rate

Objectives (Cont')

2. Gracefully degradable equipment with functional redundant technique
   - Reliability enhancement of onboard MODEM with software-defined radio flexibility
   - Paradigm shift from dual or triple modular redundant system with exclusive equipment to functional redundant system with versatile equipment
   - Introducing a soft fault decision process (multilevel, not "hard decision") for extending mission equipment lifetime (autonomous fault decision and resource evaluation)
   - Reducing redundancy by assigning a light load to partially "out of order" equipment with taking account of a required computational complexity disequilibrium in an onboard MODEM

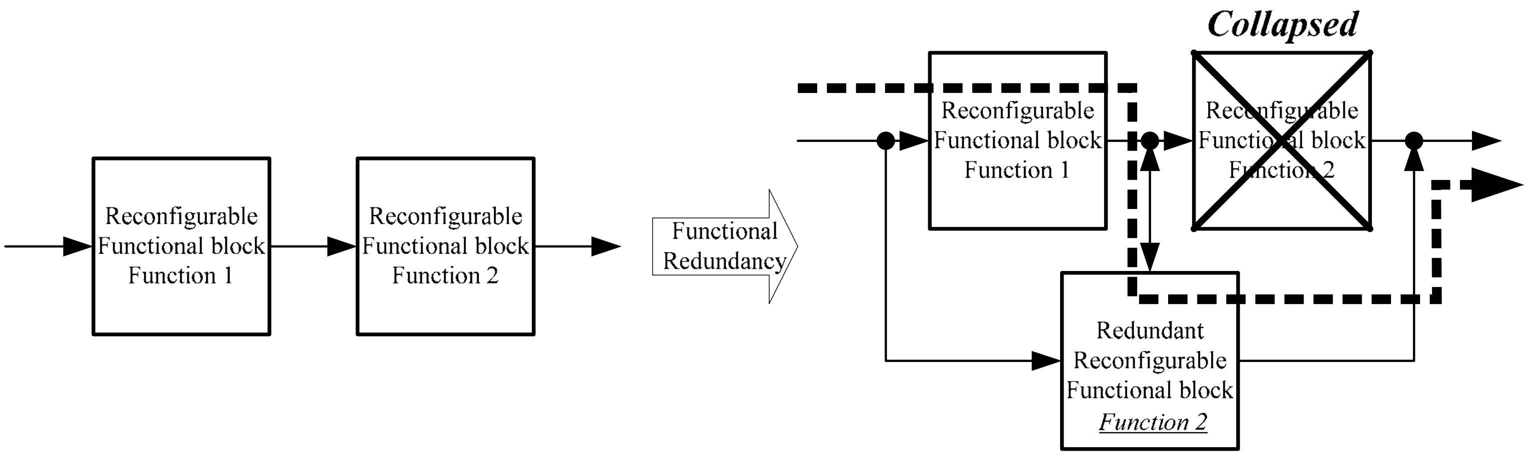
Failure rate of Stand-by redundancy system



$$P_{SR1} = \left[1-(1-P)^N\right]^2 = 1-2(1-P)^N + (1-P)^{2N} \cong \boxed{N^2P^2}$$

$$P_{SR2} = 1-(1-P^2)^N \cong \boxed{NP^2}$$

Failure rate of Functional Redundancy



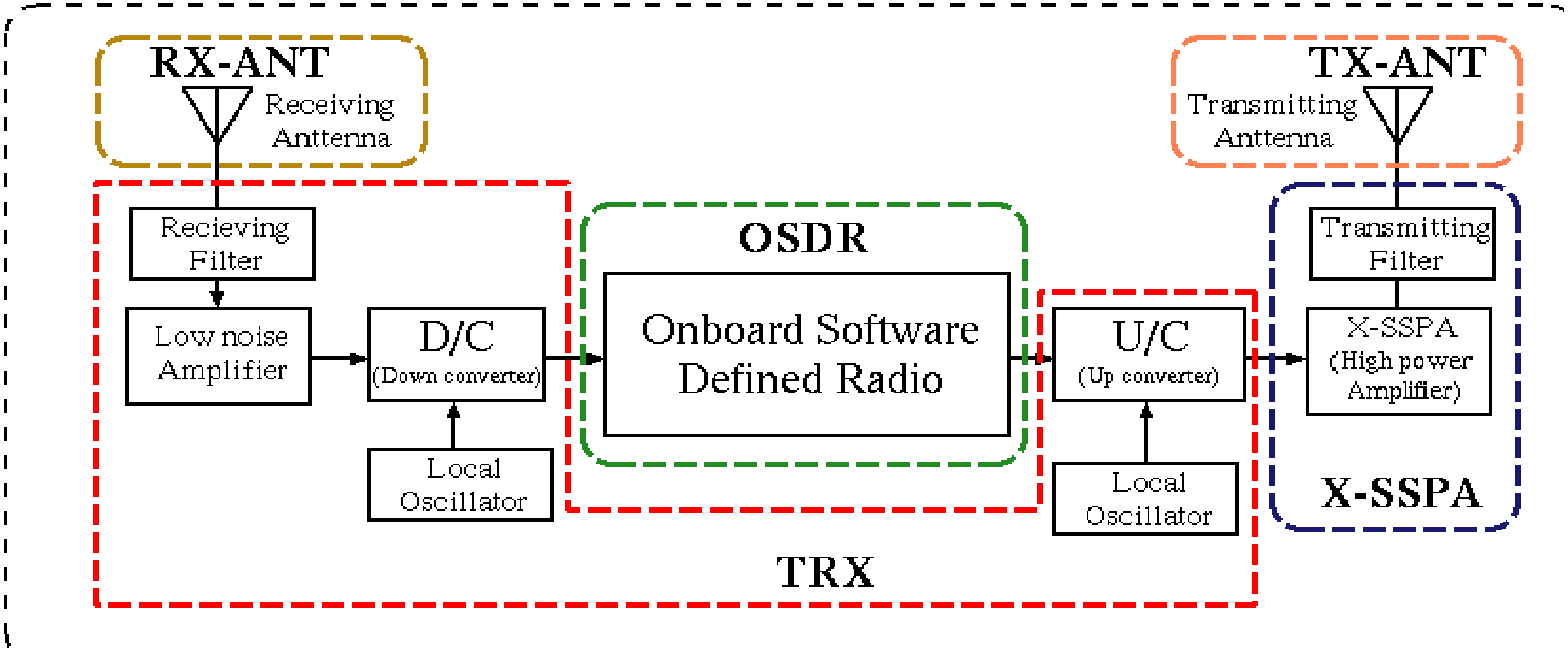
$$P_{FRL} = 1 - \sum_{k=0}^{L} {}_{N+L}C_{N+L-k} P^{k} (1-P)^{N+L-k} \cong {}_{N+L}C_{L+1} P^{L+1}$$

- N+L functional redundancy system
- Case P=1e-7, N=2
  - 2.0e-14 with stand by redundancy (4 units)
  - 3.0e-14 with functional redundancy (3units)
  - 4.0e-21 with functional redundancy (4units, two for redundancy)

Objectives (Cont’)

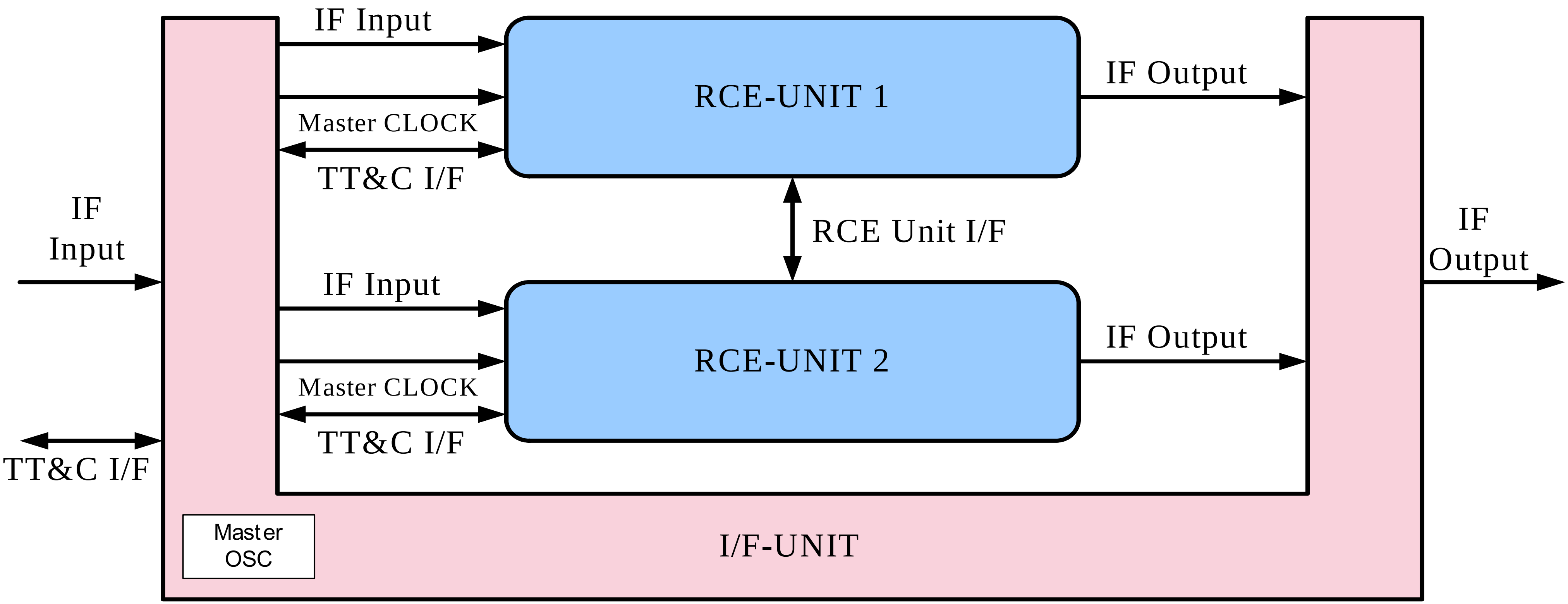
3. Test bed in Orbit
   – The architecture and the information of the OSDR will be opened
   – ***“All you can reconfigure it !”***

Reconfigurable Communication Equipment



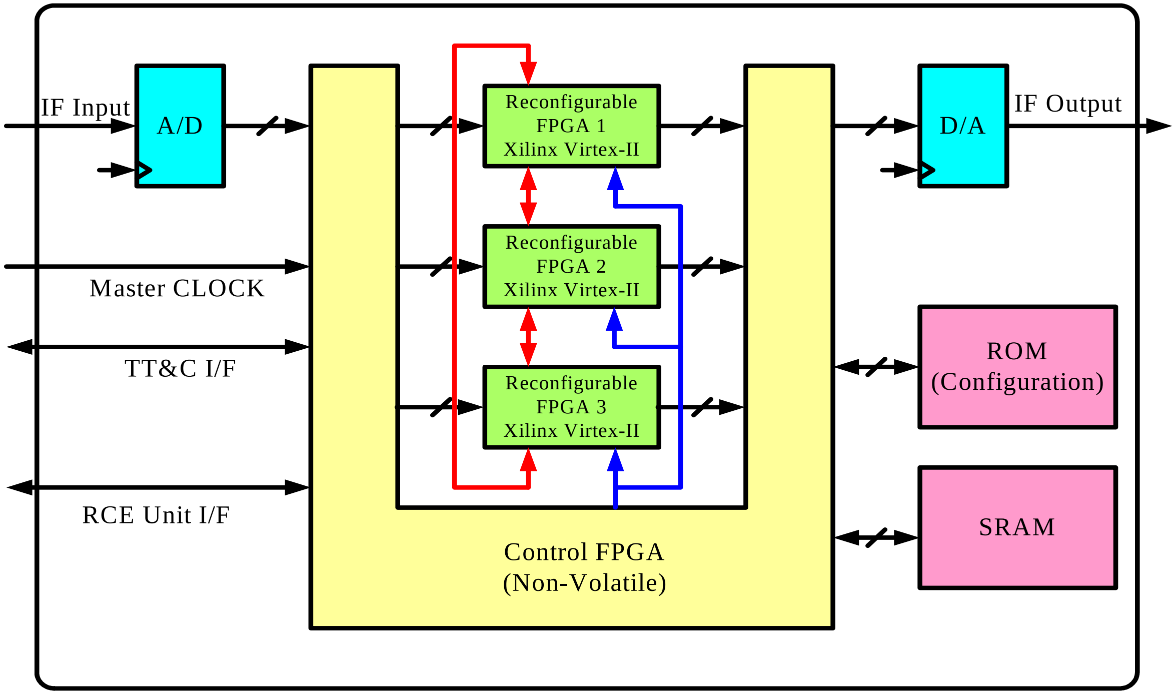
- Onboard software-defined radio (OSDR), IF components, RF components, and two antennas for reception and transmission
- Weight: 16 kg (TBD); Power consumption: 80 W (TBD)
- Frequency X 8480.000 MHz S:2054.500 MHz
- OSDR EFM manufacturing => March 2007

OSDR EFM Overview



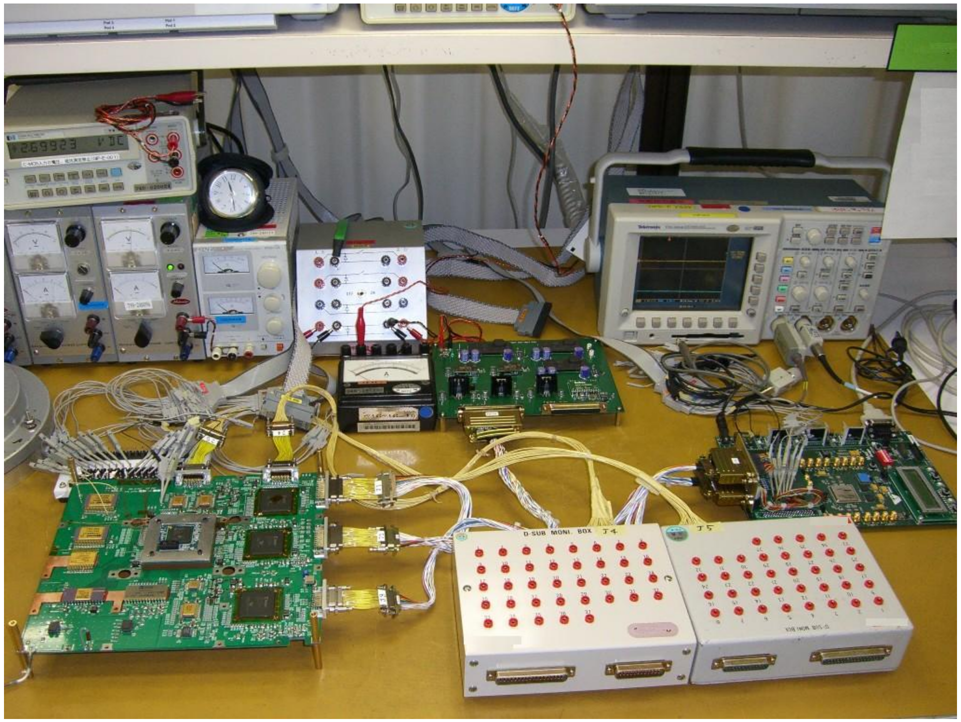
- Two identical RCE units and an InterFace (I/F) unit

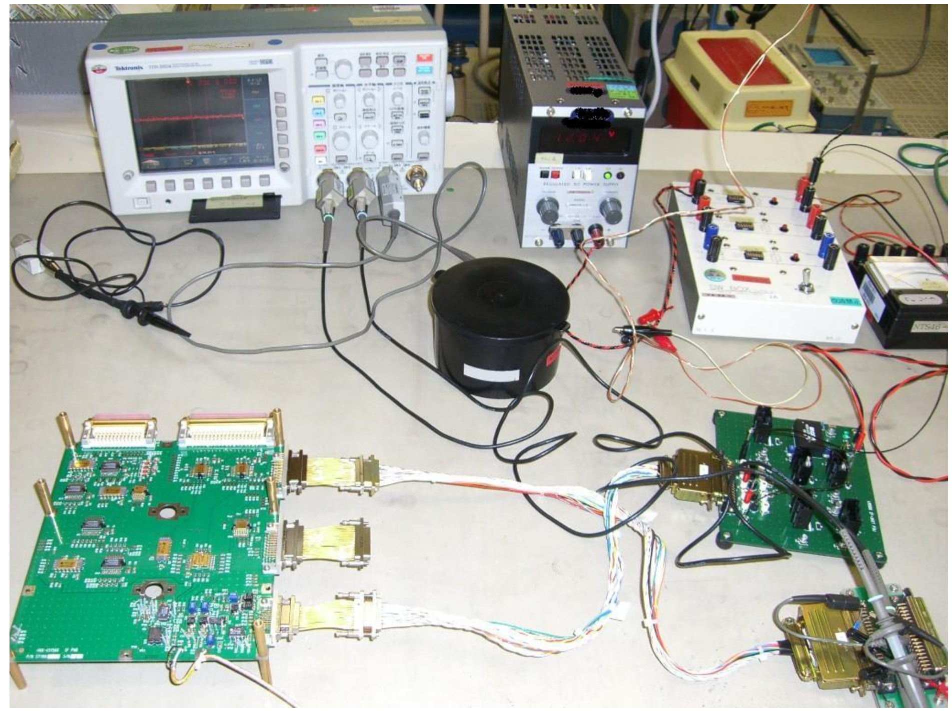
RCE unit



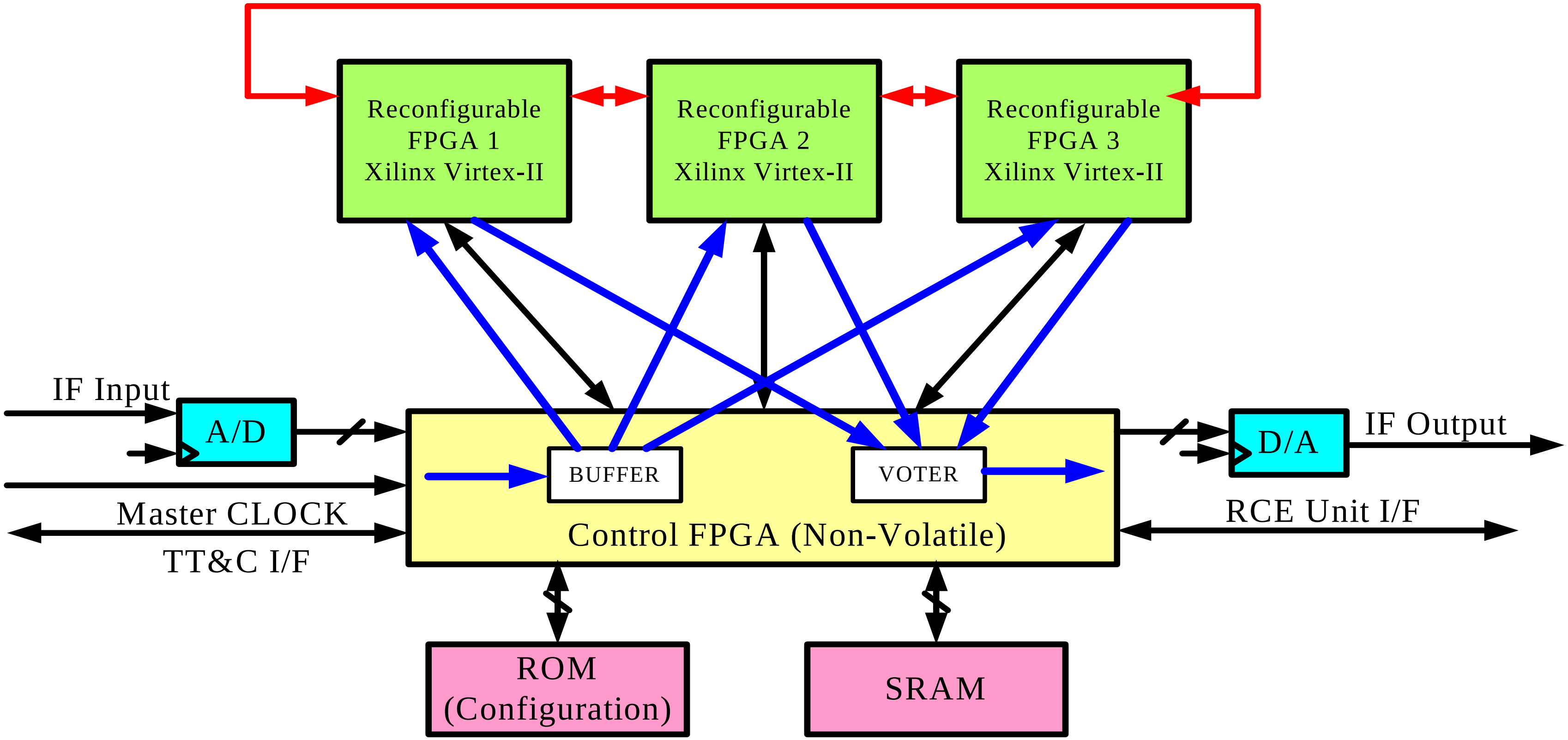
- Combination Smart but fragile device (S-RAM FPGA) and Sledgehammer but dumb device (Non-volatile FPGA)
- Three S-RAM FPGAs for reconfiguration (Virtex II XC2V1000) and
- All the inputs and outputs of the FPGAs are connected to Control FPGA and the others
- Three operation modes

OSDR inside



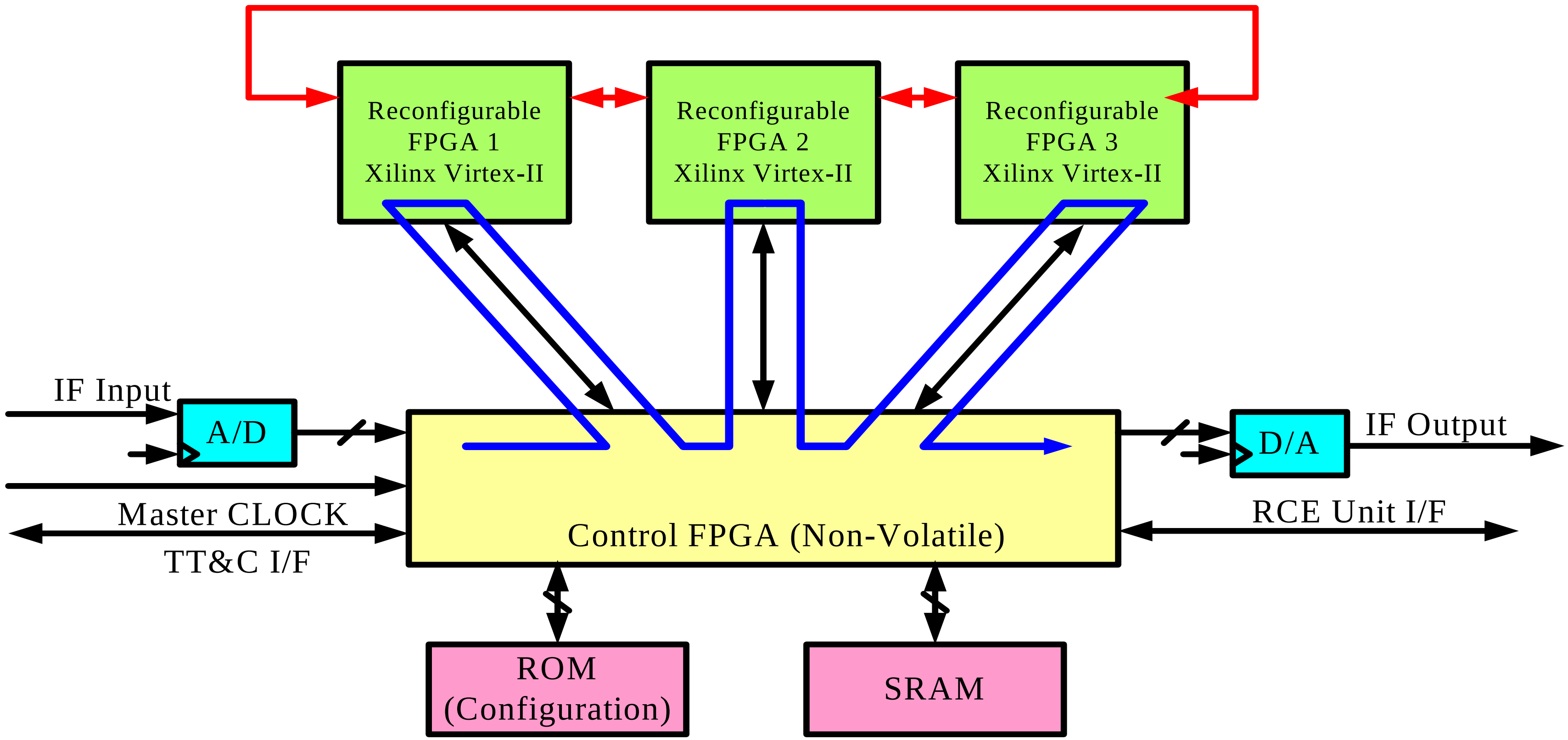


Triple modular redundancy mode

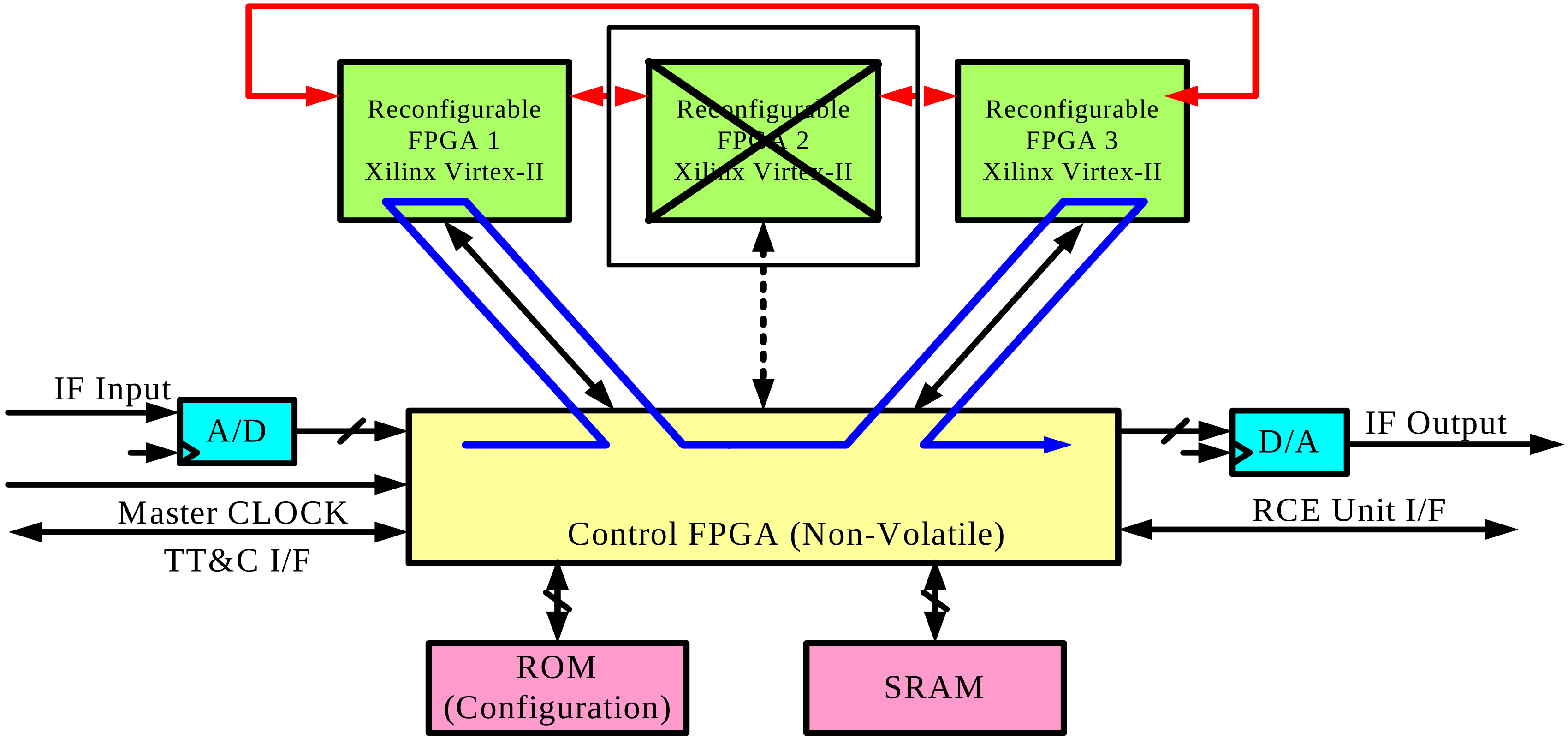


- TMR voter implemented on controller FPGA

Daisy chain mode



Degenerate mode



- Modulation and encoding require lower computational complexity than demodulation and decoding, respectively.
- A bank including a failure FPGA is assigned a modulation/encoding function.

SEU mitigation

SEU -> Data upset AND Circuit upset

- SEU must be detected for preventing “Bus-Fight” (I/O part)
- Bit assignment of Configuration stream is unknown (need reverse engineering)

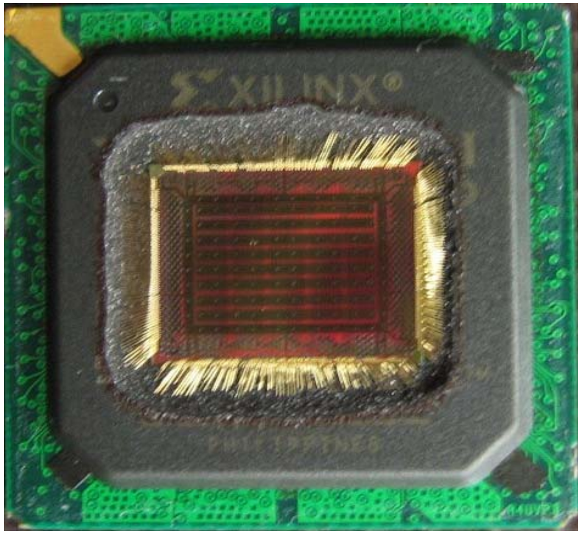
Read back inspection:

- Config data, Read back data, and Mask data are required -> three times more.

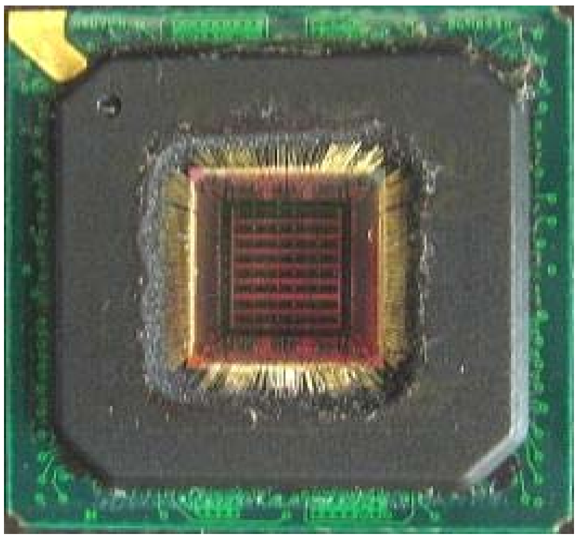
Our strategy:

- Read back the configuration data and compare it’s CRC and original one.
- Read back CRC <> Original CRC => Rebooting the device

Radiation test of Virtex II Pro

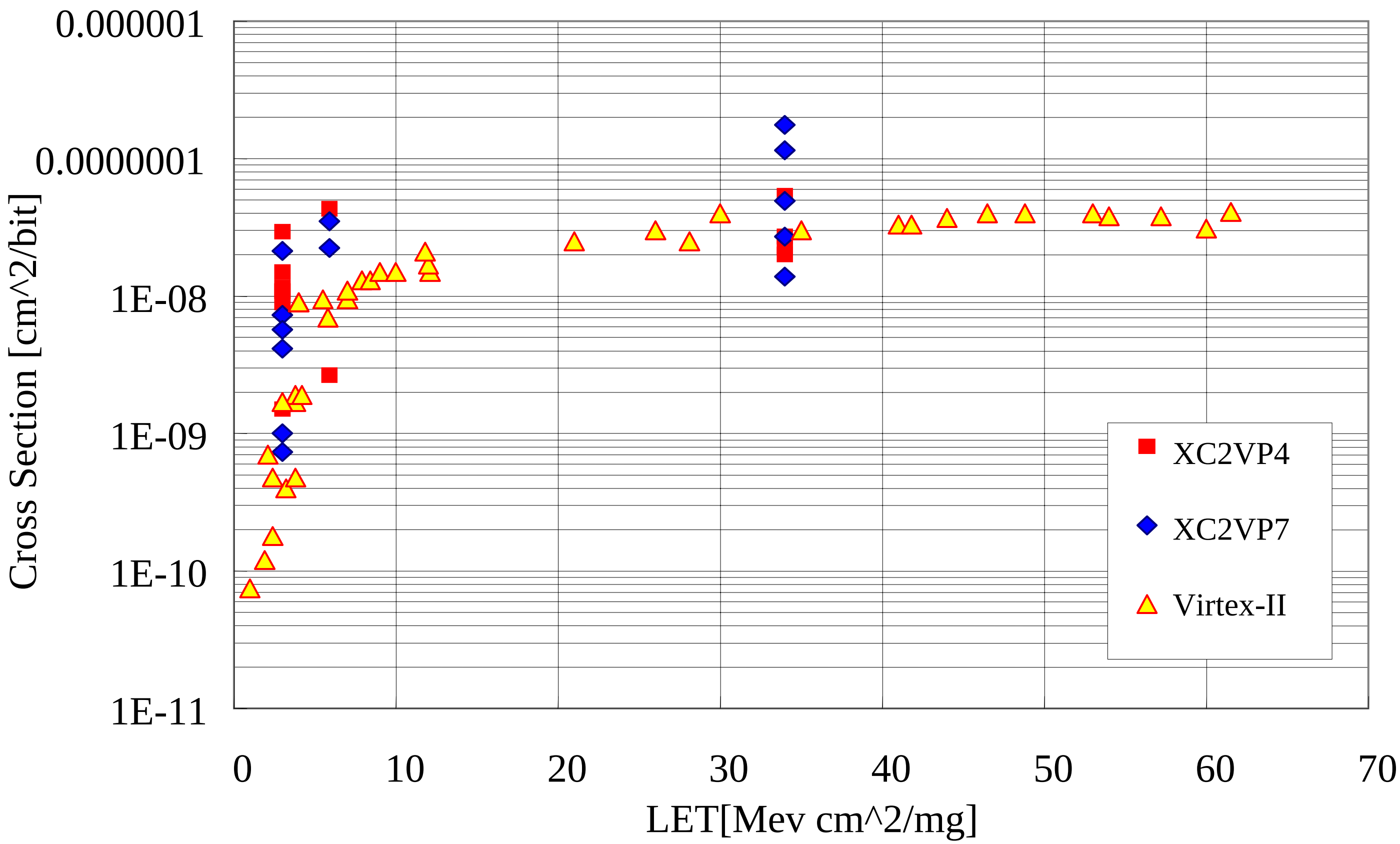


- Virtex II pro (XC2VP7-5FG456 and XC2VP4)
- Test carried out in November 2003 and February 2004 at TIARA in Takasaki, Japan
- Heavy Ions (N, Ne, and Kr)



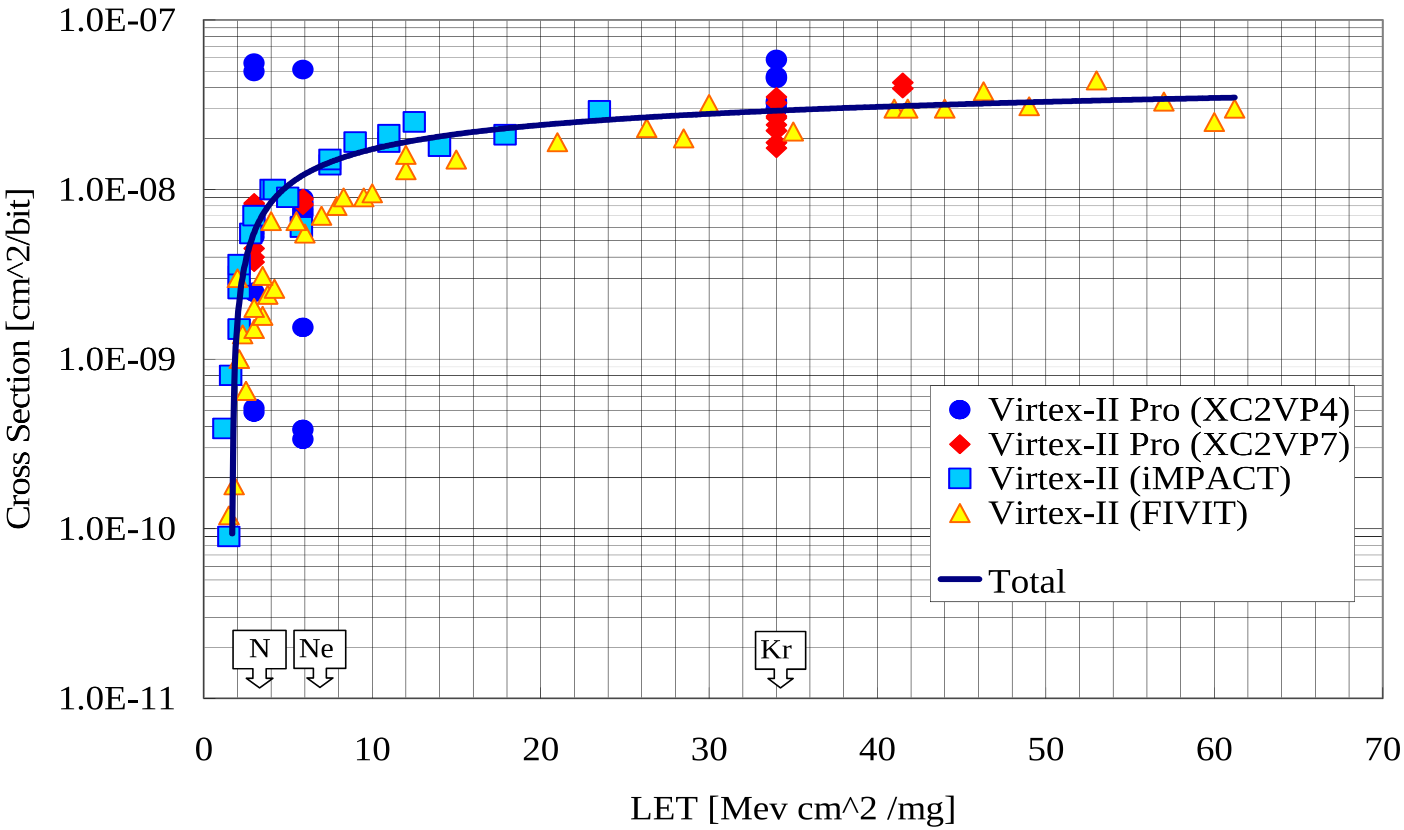
Radiation test result (1)

Block select RAM region



Radiation test result (2)

Configuration Memory region



Mean Time Between Failure Analysis (CREME 96)

	XC2VP4		XC2VP7		XC2VP100 (Simulated)	
	Solar MAX (Sec.)	**Flare Peak (1 week) (Sec.)**	**Solar MAX (Sec.)**	**Flare Peak (1 week) (Sec.)**	**Solar MAX (Sec.)**	**Flare Peak (1 week) (Sec.)**
Conf. Memory	2.64E+05	5.29E+02	1.77E+05	3.55E+02	2.32E+04	4.64E+01
DCM	4.14E+08	8.09E+05	4.14E+08	8.09E+05	1.38E+08	2. 70E+05
Block RAM	2.02E+06	3.95E+03	1.28E+06	2.51E+03	1.27E+05	2.49E+02
Multipliers	7.89E+07	1.89E+05	5.02E+07	1.21E+05	4.98E+06	1.19E+04
SYSTEM	2.3267E+05	4.6495E+02	1.5501E+05	3.0972E+02	1.95E+04	3.90E+01

- System MTBF -> Harmonic Mean of all functional blocks
  - Assumption 1: All the SEUs can be detected.
  - Assumption 2: All the gates are used.
  - Assumption 3: All the SEUs must be repaired as soon as quickly

Mean Time To Repair (MTTR)

	XC2VP4	XC2VP7	XC2VP100
Configuration data (bit)	3,006,560	4,485,472	34,292,832
MTTR (s) (10Mbyte/s)	0.037582	0.056068	0.42866
MTTR (s) (50Mbyte/s)	0.007516	0.011214	0.085732

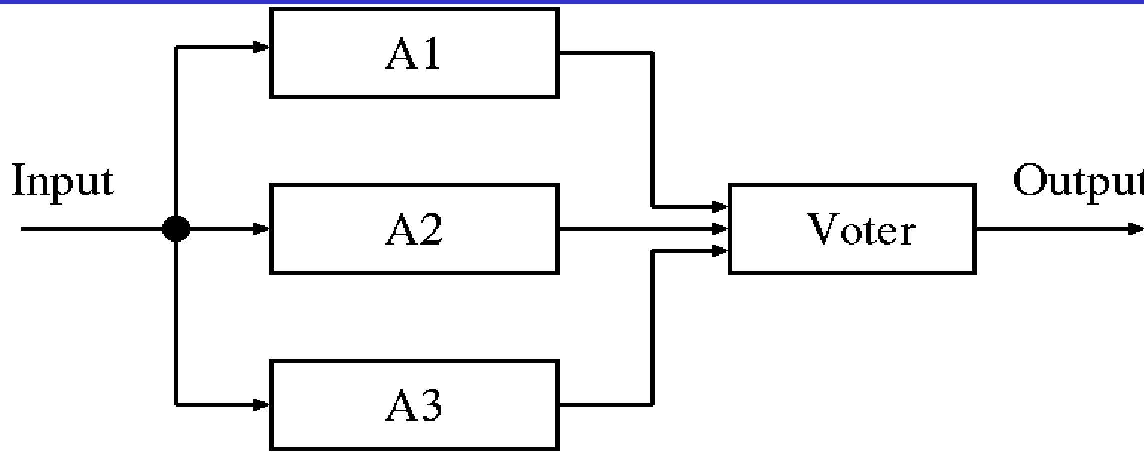
- REBOOT == Repair
  - The effects of SEU are volatile.
- By loading the correct configuration data, the operation mode will go to the normal mode.
  - Rebooting time -> Repair time
- If the SEU can be considered as **A Failure,** the MTTR is roughly proportional to the size.
- The maximum data rate for loading is fixed : 50M byte/Sec. for XC2VP series.
  - The larger gate size or configuration size, the longer MTTR becomes necessary.

Nonavailability Analysis

	XC2VP4		XC2VP7		XC2VP100 (Simulated)	
	Solar MAX	**Flare Peak**	**Solar MAX**	**Flare Peak**	**Solar MAX**	**Flare Peak**
10 Mbyte/s	1.6153E-07	8.0824E-05	3.6172E-07	1.8099E-04	2.1974E-05	1.0885E-02
50 Mbyte/s	3.2306E-08	1.6166E-05	7.2344E-08	3.6204E-05	4.3949E-06	2.1961E-03
100 Mbyte/s	1.6153E-08	8.0830E-06	3.6172E-08	1.8102E-05	2.1974E-06	1.0992E-03
200 Mbyte/s	8.0764E-09	4.0415E-06	1.8086E-08	9.0513E-06	1.0987E-06	5.4992E-04
400 Mbyte/s	4.0382E-09	2.0208E-06	9.0430E-09	4.5257E-06	5.4936E-07	2.7504E-04

- MTBF is **inversely proportional** to the die area and MTTR is **proportional**. -> Large FPGA has disadvantage.
- Large size FPGA does not meet the criteria 10e-6
  - Much larger down load rate will be needed (50 M Byte/S is too slow)
  - How to mitigate? –partitioned small FPGAs

Triple Module Redundancy



- One out of Three system failure is acceptable.
  - Loose regulation
  - Acceptable when the MTBF is quite large compared with MTTR

	XC2VP4		XC2VP7		XC2VP100 (Simulated)	
	Solar MAX	**Flare Peak**	**Solar MAX**	**Flare Peak**	**Solar MAX**	**Flare Peak**
10Mbyte/s	7.83E-14	1.96E-08	3.93E-13	9.83E-08	1.45E-09	3.53E-04
50Mbyte/s	3.13E-15	7.84E-10	1.57E-14	3.93E-09	5.79E-11	1.44E-05

Thank you very much

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