Multi-DSP/Micro-Processor Architecture (MDPA)

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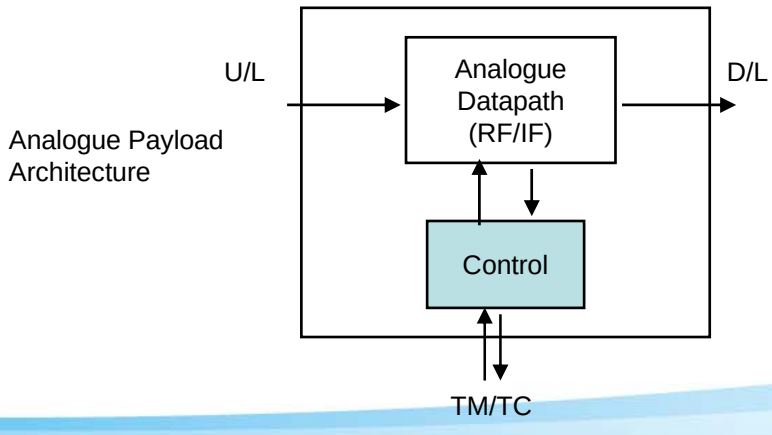
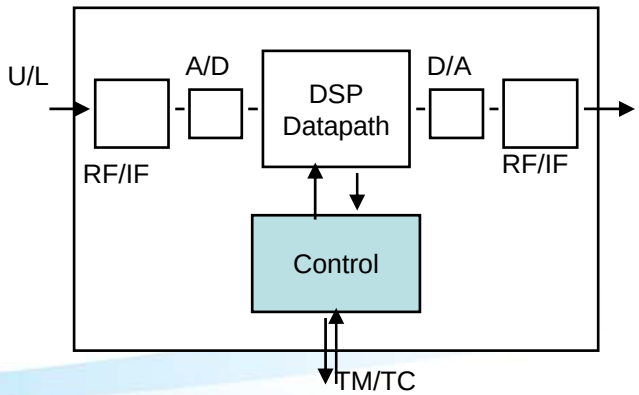
MDPA for New Generation Processor (NGP)

- Payload Control Processor MDPA (Multi-DSP/ µProcessor Architecture) features:
  - High Control Processing Performance (70MIPS@4W)
  - Scalable to multiprocessor system via SpaceWire with routing capability
  - Spacecraft interface via Milbus or SpaceWire
  - Payload interface via MilBus, SpaceWire or CAN bus
  - DVB-S regeneration function for high speed TM/TC with Network Control Center (600Kbps each direction)
  - Stand-alone Unit with own redundant power converter or integrated within platform or payload electronics

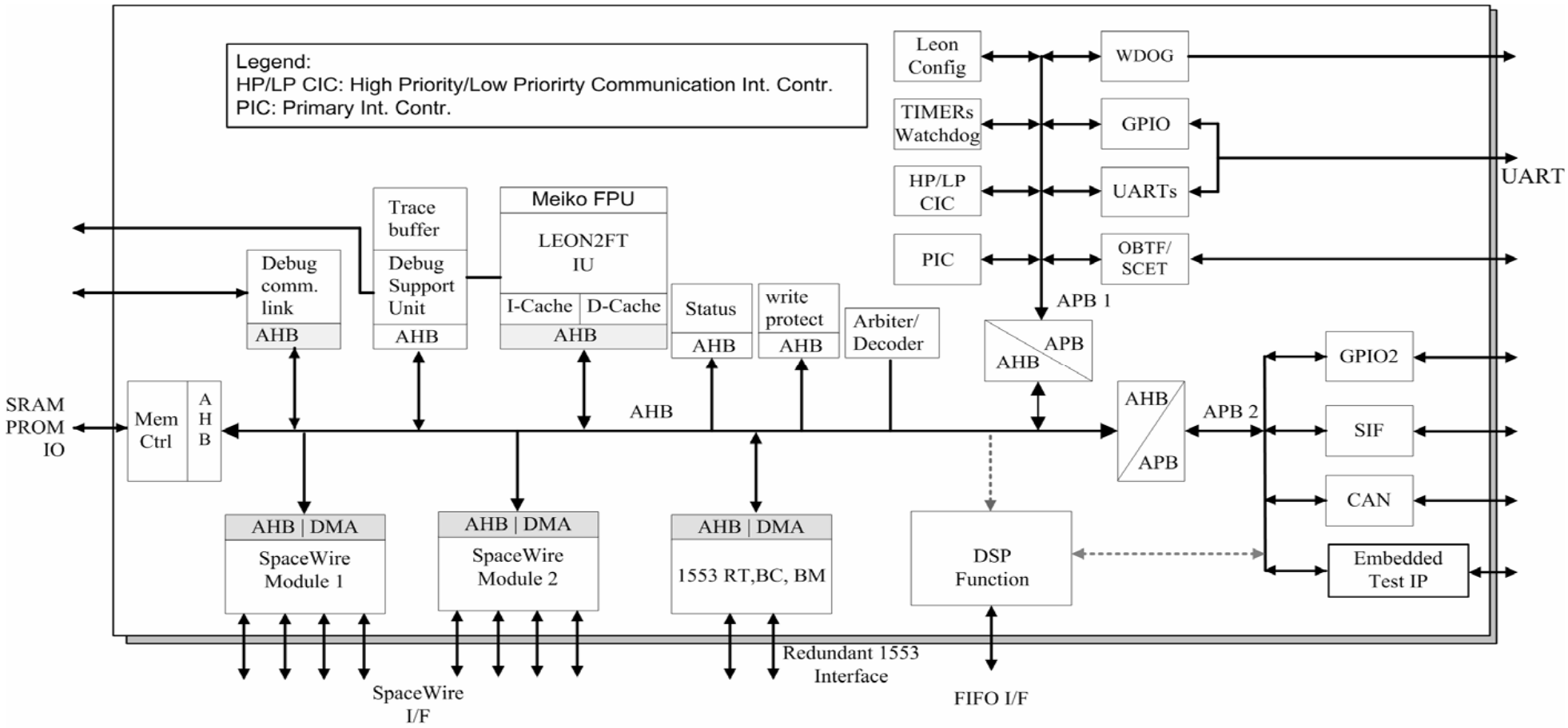


Analogue Payload Architecture



Digital Processing Payload Architecture

MDPA ASIC Blockdiagram



MDPA ASIC SoC architecture

- The MDPA architecture uses the AMBA Bus.
  - All high speed devices (in terms of latency or transfer rate) are connected to the AHB Bus. The AHB bus has several advantages:
  - high transfer rates (2,5Gbits/s @ 80MHz)
  - low latency
  - Guaranteed latencies due to round robin arbitration.
  - No Bus contention
    During System Architecture it was taken care that bus contention will not be possible. No Bus member, except the 1553 IP, is allowed to block the AHB Bus via the Amba LOCK mechanism for a single read-modify-write transaction.
    No Bus master can block the bus through long bursts.
  - accepted and widely used industry standard

MDPA ASIC SoC elements

- Basic Elements of MDPA SoC
  - LEON2-FT processor
  - Hardwired DSP algorithms
  - General Purpose Clock
  - UARTs
  - SpaceWire
  - Service Interface (SIF)
  - MIL-STD-1553B Interface Controller
  - CANbus
  - Time distribution services
    - Real Time Clock (RTC)
    - Spacecraft Elapsed Time (SCET)
    - AOCS Cycle Time (ACT)
- Additional processing features
  - Floating Point Unit (FPU)
  - Watchdog
  - Non maskable interrupt (NMI)
  - Reset register
  - Software reset
  - GPIO extension
  - SRAM bank swap
  - SRAM Chip Selects

Leon2FT Configuration (Cache)

- 32kb instruction cache with 4way associative cache
  - Guarantees high cache hit rate
- 16kb data cache with 2way associative cache
  - MDPA is usually a controller
  - Number crunching is not a application for the CPU
- 32byte cache line size for instruction access
  - Fastest possible access to SRAM
  - Code resides sequentially in RAM
- 16 byte cache line size for data access
  - Is only used to administrate the cache
  - Data is read in word/dwords (4/8 byte) at a time

Leon2FT configuration (FT)

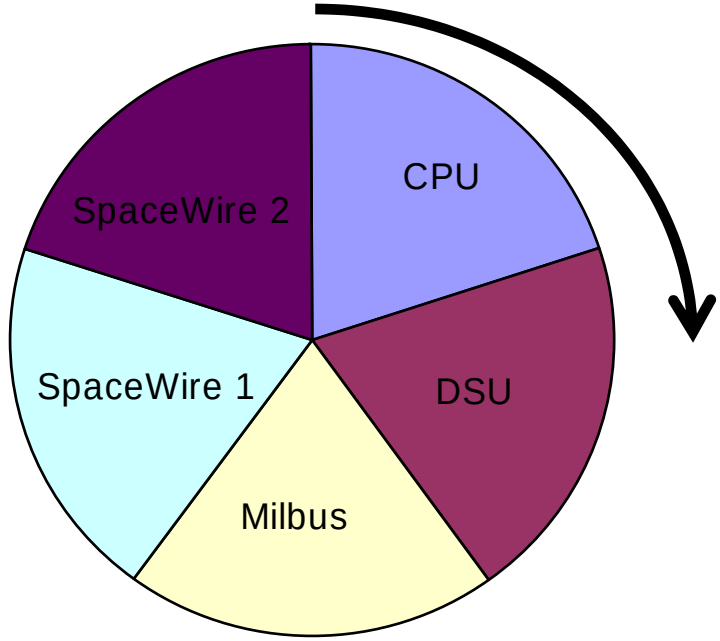
- EDAC protected SRAM
- EDAC protected SPARC register block
- Parity protected cache
- SEU hard FF (using ATC18RHA technology)
- Some registers that can generate resets or non maskable interrupts support triple voting

Leon2FT Configuration

- Multiplier
  - Fastest one is design goal (1-cycle)
  - If critical path is in multiplier unit a 4-cycle multiplier will be used
  - Multipliers are important for calculation jump addresses
- 1024 trace lines
  - Up to 1024 cycles can be analyzed without influencing the system
- Meiko FPU
  - Cheaper and smaller than the Gaisler FPU
  - Only has to be licensed if the FPGA/ASICs are sold
  - Big heritage in older Sun CPUs
  - Important is the floating point capability. Performance is not an issue

AHB Arbiter

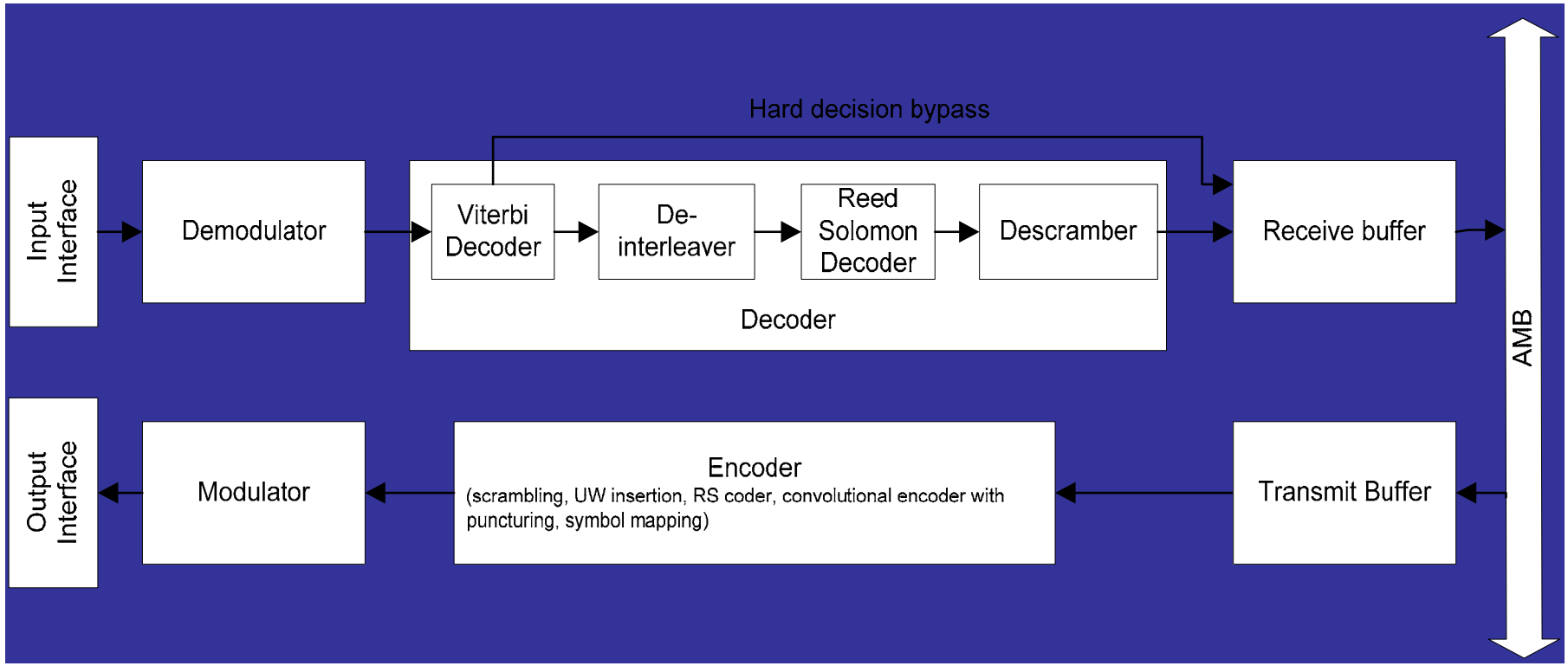
- Leon2FT is delivered with a hard encoded priority arbiter.
- A system with a priority encoded arbitration can be locked if two master continuously access the bus
- Round Robin arbiter offers the best solution
- Other solution would be to minimize the number of AHB masters



SpaceWire Modules

- Two modules with 4 SpW interfaces
- Modules were used without routing capabilities in older projects
- Routing capabilities with logical and path addressing is currently implemented
- Every Module has its own DMA. So they can independently access the memory space
- Internal interrupt controllers ease connection to system

DSP Block



Embedded Test IP

- Customer furnished item from Astrium UK
- APB Interface was added to enable CPU interaction
- Enables following test scenarios:
  - Go/Nogo tests without BSCAN Equipment
  - Remote tests in harmful environment
  - Complete system tests via boundary scan
  - Test are either controlled by external equipment
  - Or by CPU

SpW Service Interface (SIF)

- Already used for debugging purposes in older projects
- Fast and easy way to upload new software
- Software can dump status information with lowest possible system influence
- Therefore can also be used in FM
- adds debugging capabilities where the Leon2FT DSU functionality ends

Milbus Interface

- IP Core from Astrium SAS
- Can be either BC, RT or BM

CANBus Interface

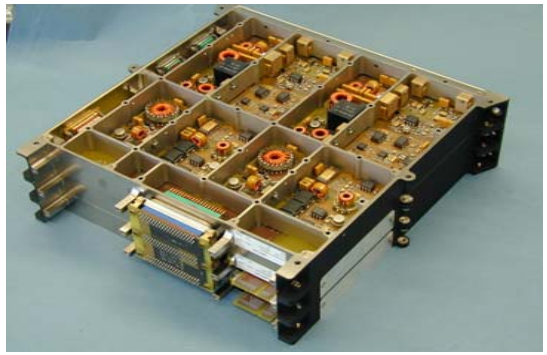
- Hurricane 5.1 IP Core from ESA
- APB wrapper from Hurricane 4.6 was enhanced

MDPA Development Plan

- Predevelopment
  - MDPA chip functional model (VHDL) and validation (DSP-IP and SpaceWire outstanding)
- Kick-off to PDR (Dec 2006 - Sept 2007)
- PDR to CDR (Sept 2007 -May 2008)
- CDR to FR (May 2008-Nov 2008)

MDPA Project Output

- Outputs:
  - MDPA ASIC
  - MDPA controller module
  - Standalone box (non-redundant) including DC/DC converter
  - Test and Verification Software
  - Unit Tester



Example of a standalone box with a redundant processor module and a DC/DC converter (without side covers)