FFTC – Fast Fourier Transform Co-processor

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Introduction

FFTC Project consists of two parts

- FFTC ASIC
- FTAB (FFTC Accelerator Board)

Target Applications

- SAR Image Processing
- Radar Altimeter Processing
- Fourier Transform spectrometer data processing
- Data compression (e.g. wavelet)
Background

PowerFFT

- PowerFFT is proprietary of Eonic
- PowerFFT is commercially available
- PowerFFT IP is licensed by ESA from Eonic

The concept of the PowerFFT is the basis for the FFTC device development.
FFTC Functional Requirements

- **Input/Output complex data format**
  - Parallel I and Q: 8 to 16 bits integer; 8 to 16 bits sign-inverted integer, 32 bits IEEE floating point; 32 bits integer
  - Sequential I and Q: 32 bits IEEE floating point; 32 bits integer

- **Complex data filtering or windowing**

- **Fast Forward / Inverse Fourier Transforms based operations**
  - FFT / IFFT
  - Convolve / correlate 2 vectors in frequency domain
  - Convolve / correlate a vector with vector in frequency domain
  - Multiply / conjugate multiply 2 vectors and FFT / IFFT result

- **Perform square law detection**

- **Output complex or real data**

- **Complex multiply**
**FFTC Device Requirements**

- Initialise itself
- Load its internal registers
- Perform a function in cyclic mode
- Select FFT length from 16 to 1024 points
- Perform 1024 points complex FFT in less than 50 microseconds (goal 10 microseconds)
- Perform 256 taps FIR on block of 64 k samples
- Perform gain and offset correction
- Batch repeat mode for short FFT lengths
- Integrated EDAC for on-chip and off-chip memories
FFTC Design Requirements

- FFTC contains 4 radix 2 processors working as butterfly engines
  - FFTC provides MAC (Multiply/Accumulate) functionality
  - FFTC includes internal RAM
  - FFTC will be manufactured in a space qualifiable ASIC technology
- FTAB includes address generators
- FTAB includes a sequencer and control logic
**FFTC Architecture**

- **FFTC Control**
- **MAC Core**
- **FFT Core**
- **Crossbar Switch**
- **Input Converter**
- **Output Converter**

Primary data input

Primary data output

4 additional memory ports
FFT Core
- vector length 16, 32, ... to 1024 points

MAC Core
- Vector multiplication of two vectors
- Vector addition of two vectors
- Gain / offset operation
- Conjugate one vector and add to second vector
- Square law detection of a vector
### FFTC Architecture (cont.)

**Control**
- Data converters, processing core, cross-bar switch etc. are set through FFTC control instructions
- Device is programmed using high level instructions
- Very Long Instruction Word (VLIW): one instruction sufficient for FFT up to 1024 points
- Cycled operations possible

**Memory Ports**
- External memory banks provided for longer FFTs or multi-dimensional data sets
- Are controlled and synchronized by external memory controller
- Can be used as data buffers
ASIC Facts

FFTC ASIC will be realised in ATC18RHA technology from ATMEL in the frame of a MPW run

- Core supply voltage: 1.8 V
- I/O supply voltage: 3.3V
- estimated gate count: ~4 Mio
- Package: MCGA625
- Memory ports: 4
FFTCC Demonstration System

- **FTAB - FFTC Accelerator Board**
  - Serve as a demonstrator for the FFTC device
  - it can be used as a building block for high performance on-board signal processing units
  - it can be connected to a SpaceWire network, allowing scaling of processing performance for application requirements

- **FFTCC demonstration system is based on**
  - FFTC Accelerator Board
  - Host (test) computer (PC)
  - SpaceWire PCI interface board
FFTC Accelerator Board (FTAB)

FFTC

Buffer Memory 1

Buffer Memory 2

Buffer Memory 3

Buffer Memory 4

Controller and Address Generator

SpaceWire Interface Chip

Data

Control
FTAB Support software

- Host computer controls the FTAB via SpaceWire
- Communication between Host and FTAB via SpaceWire
- Perform FFTC and FTAB configuration
- Send commands for FFTC via SpaceWire
- Data transfer to and from FFTC via SpaceWire
- Communication is based on RMAP
Status

- Start of the FFTC project in April 2007
- Requirement Review in June 2007
- Architectural Design Review in September 2007
- Logic Review in December 2007
- Design Review in July 2008
- Prototypes in October 2008
- Project end in January 2009