Monolithic Galileo/GPS Front-End ASIC

8-March-2007

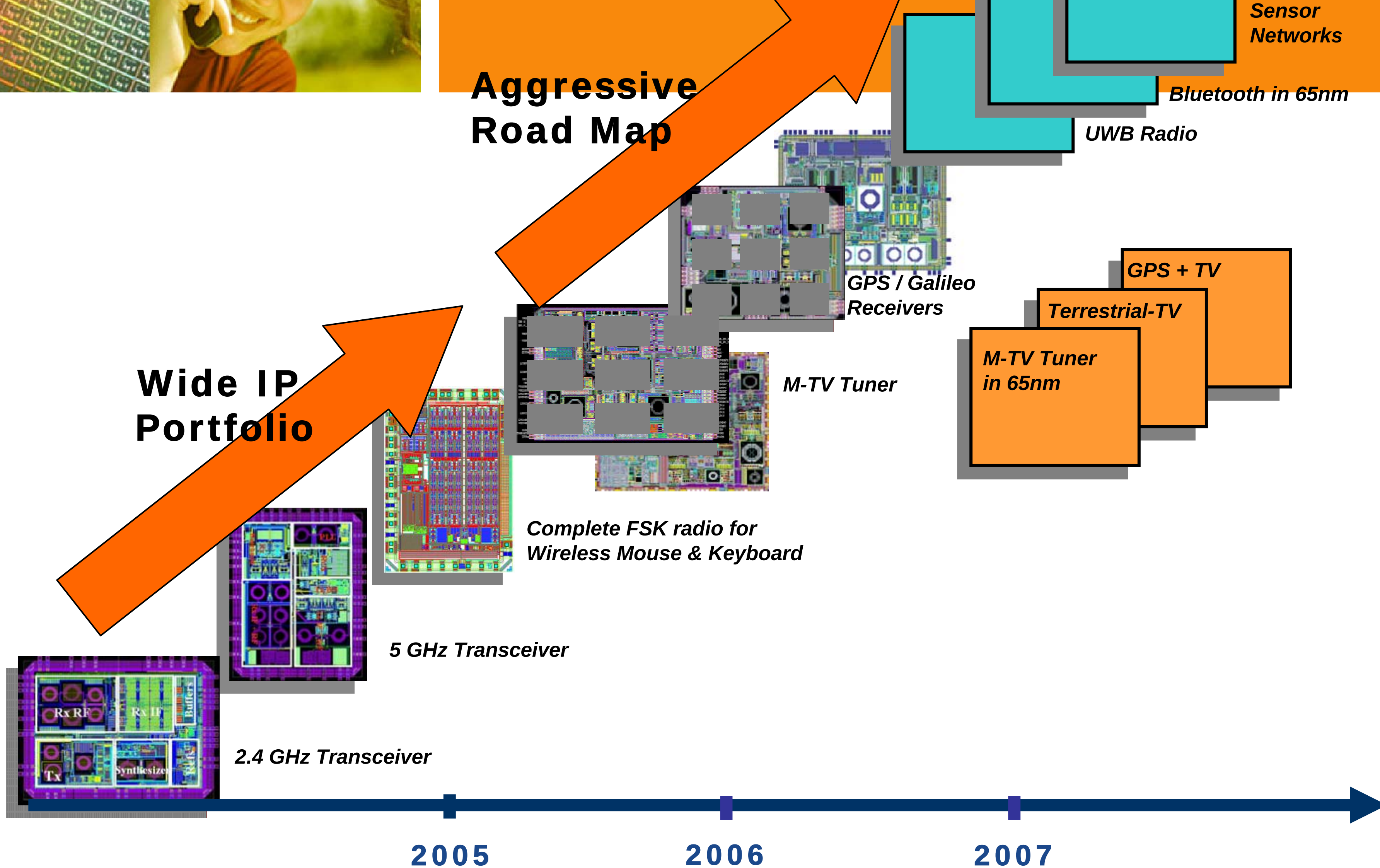
Contents

- Introduction to Chipidea
- Chip specifications
- Schematics overview
- Layout & Packaging
- Test Setup
- Characterization Tests
- Future – Receiver Tests
- Future – Radiation Tests
- Future – Next Spin

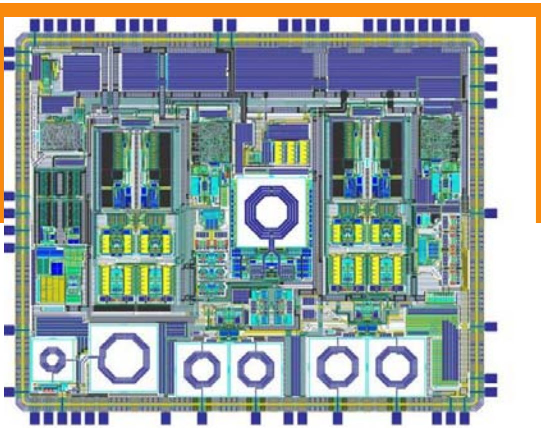
Chipidea, Your Partner for RF Solutions

- **Complete system solution far beyond the RF chip**
  - Baseband converters that can be located either in the RF chip or Baseband SoC
  - Optimum partitioning of filters between analog and digital
  - Support functions such as supply regulation, clock generation, etc.
  - Advanced Digital Interfaces, such as 3GDigRF
- **Proven RF design competence**
  - From complete FSK radios for ISM HF bands to UWB RF front-ends
  - RF Transceivers in 2.4 GHz band and in 5 GHz band
  - For GPS receivers supporting Galileo
  - For Mobile TV covering all the bands (from VHF to L-Band) and standards (DVB-H, T-DMB, ISDB-T)
- **Working in close collaboration with Customers**
  - Incorporating exclusive differentiating features for better competitiveness
  - Adapting the interfaces to suit specific application

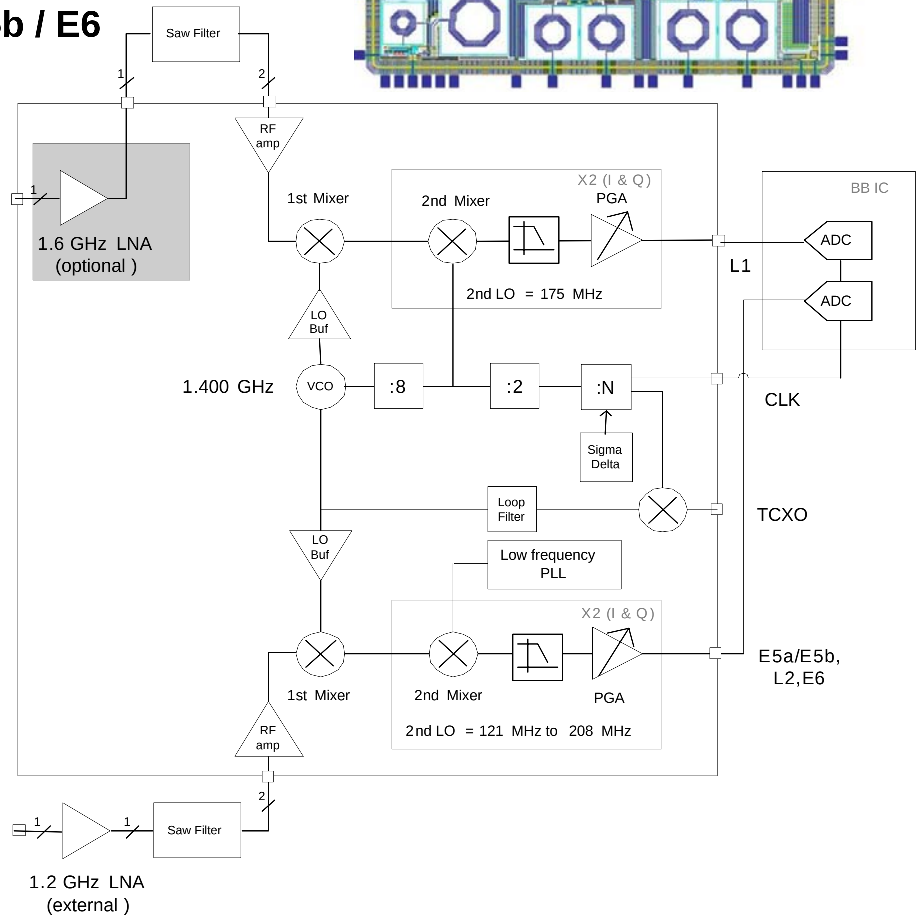
RF Road Map



Aggressive Road Map
Wide IP Portfolio
Sensor Networks
Bluetooth in 65nm
UWB Radio
GPS / Galileo Receivers
GPS + TV
Terrestrial-TV
M-TV Tuner in 65nm
M-TV Tuner
Complete FSK radio for Wireless Mouse & Keyboard
5 GHz Transceiver
2.4 GHz Transceiver
Rx RF
Rx IF
Buffers
Tx
Synthesizer
2005
2006
2007

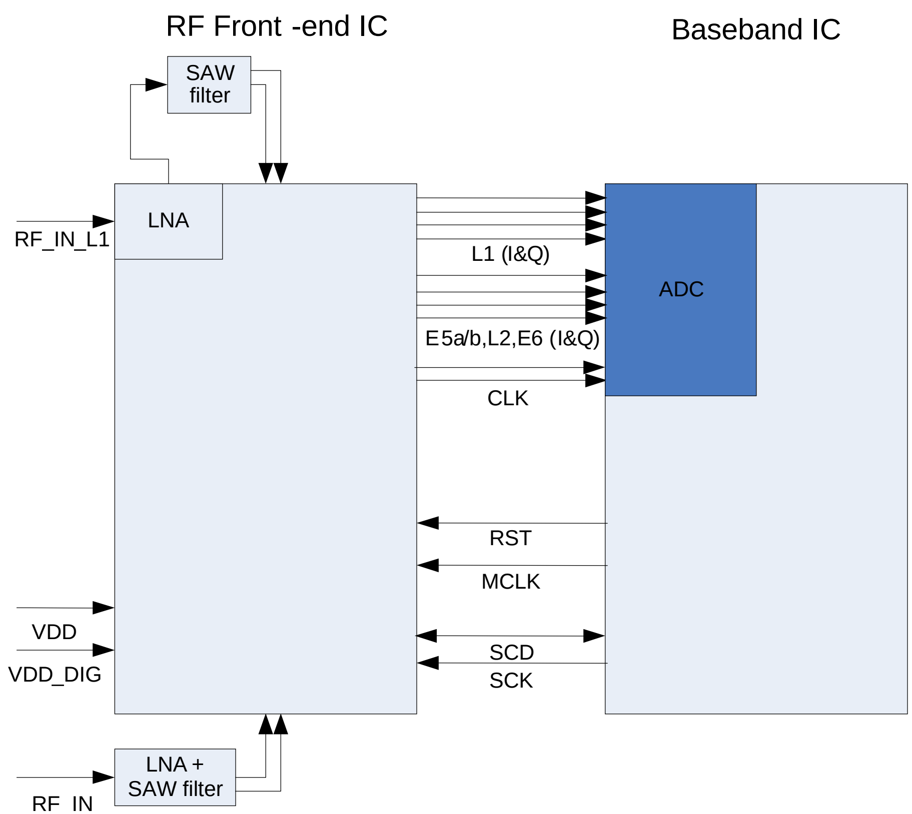


- Targets Galileo & GPS Positioning Systems
- Multiple Band Reception E1 / L1 / L2 / E5a / E5b / E6
- Simultaneous reception of:
  - L1 plus L2,
  - L1 plus E6,
  - L1 plus E5a or L1 or E5b,
  - L1 plus joint reception of E5a+E5b
- Low BOM – “On-chip” Filtering with only external LNA and RF Filters
- Zero IF with DC cancellation and Automatic Gain Control
- Fully Integrated PLL
- Onboard Crystal Oscillator
- 1.8 V Single Supply
- Current consumption: 25mA
- Chip Area: ~6.2 mm2
- First Silicon available



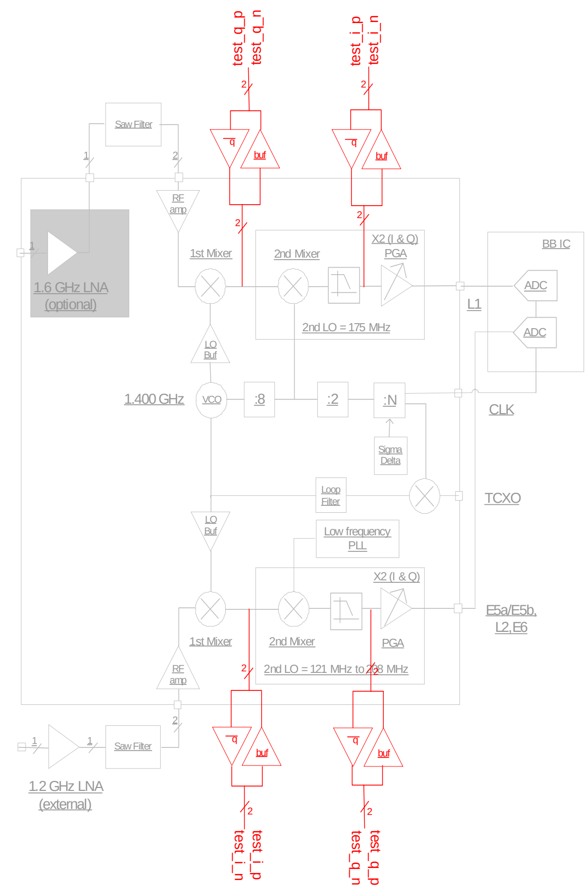
Application Diagram

- Communication with baseband IC, control, configuration, testing



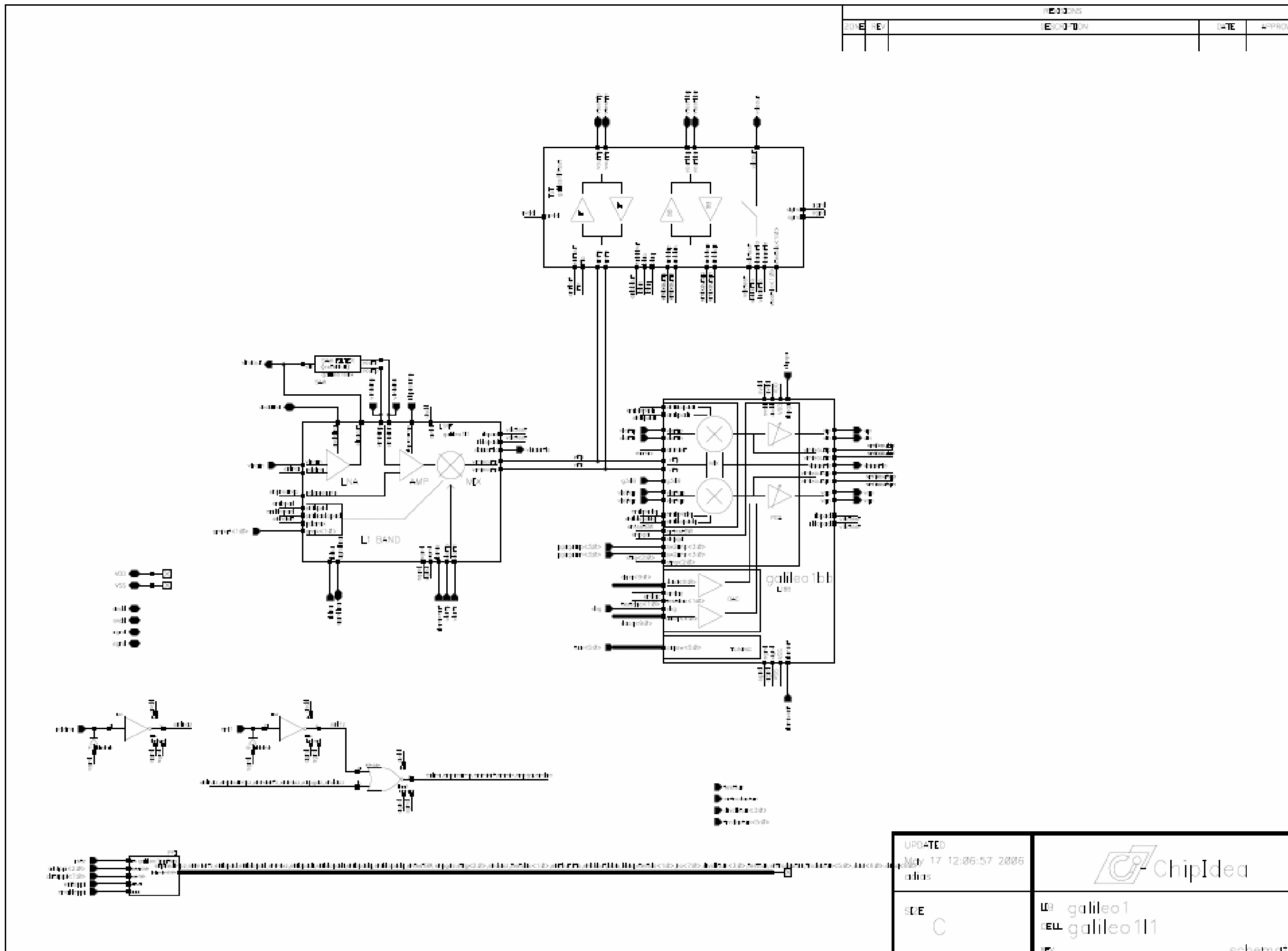
Testability

- Bi-directional buffers are strategically placed in critical node of the receiver.
- Four test pins are used for debug.
- The IF signal can be monitored or applied externally into the circuit for debug or characterization.
- The Baseband PGA input signal can be monitored or applied externally into the circuit for debug or characterization.
- Critical DC voltage of several blocks can be measured or forced using the four test pins.
- VDC_TEST: Dedicated test pin for Sigma Delta. Can output DC voltages of DUT, eg, Mixer CM, VCOs control Voltage, etc.



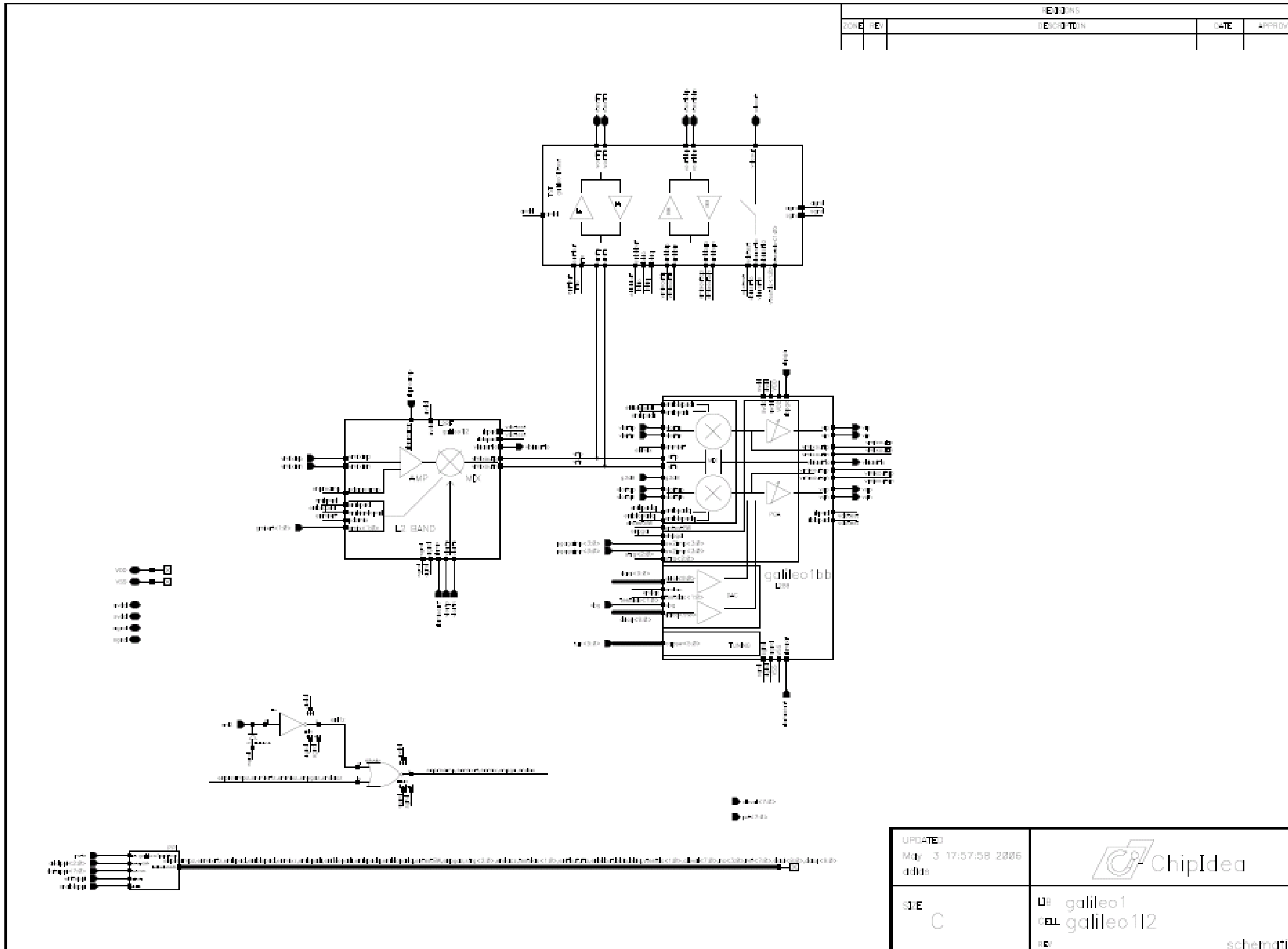
L1 receiver

- LNA (opt)
- Preamp
- 1st mixer (175MHz)
- 2nd mixer (zero-IF)
- PGA
- IQ offset DACs



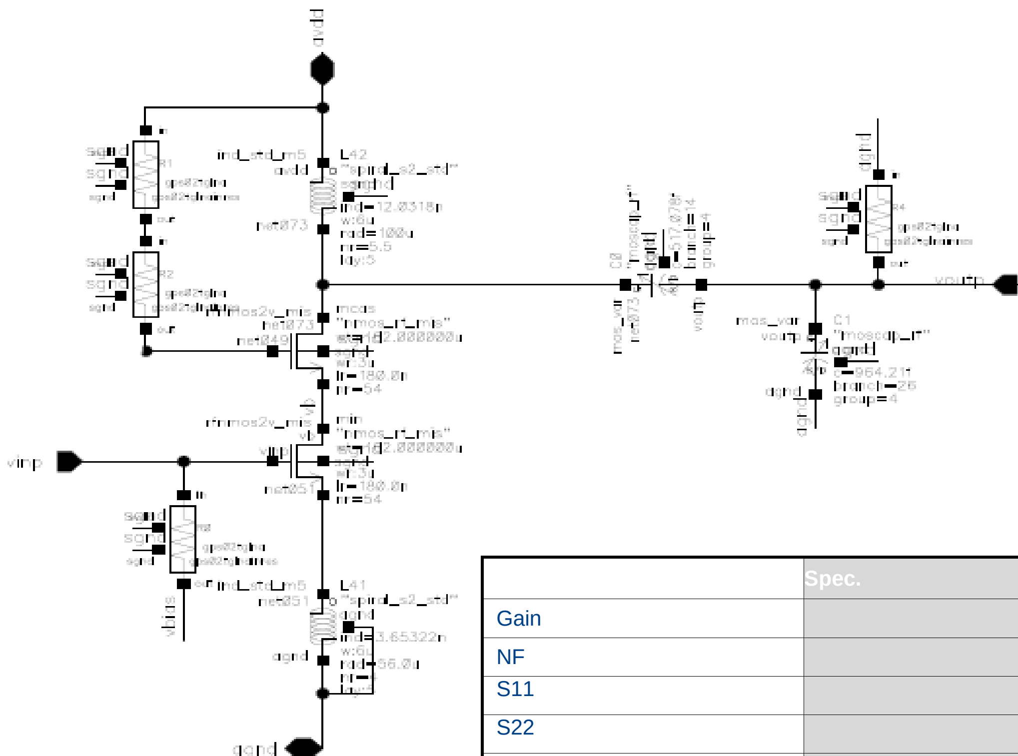
E5a / b L2 E6 receiver

- Preamp
- 1st mixer (121MHz to 208MHz)
- 2nd mixer (zero-IF)
- PGA
- IQ offset DACs



LNA for GALILEO / GPS application

LNA for GALILEO/GPS application (1.6GHz)



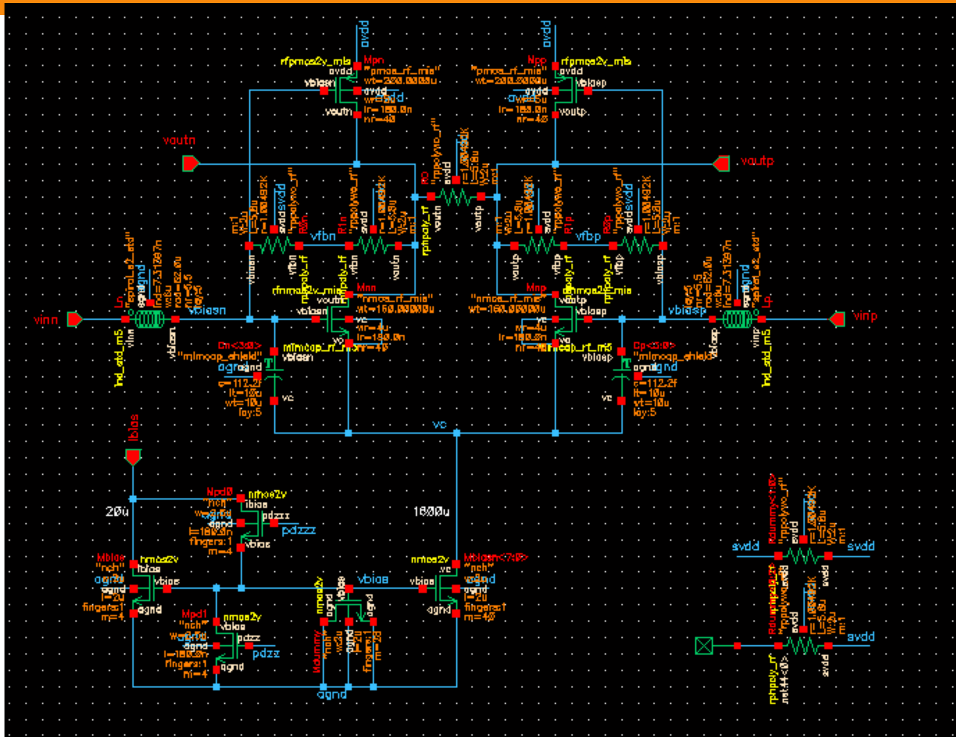
- Single ended
- L degenerated architecture
- External Inductor

	Spec.				
Gain	15	13	15.6	17.8	dB
NF	< 2 max	1.1	1.3	1.6	dB
S11	< -10 min	-16.7	-13.4	-10.9	dB
S22	< -10 min	-23.5	-15.9	-12.3	dB
IP3	> 0	-	1.2	-	dBm

RF Preamp L1

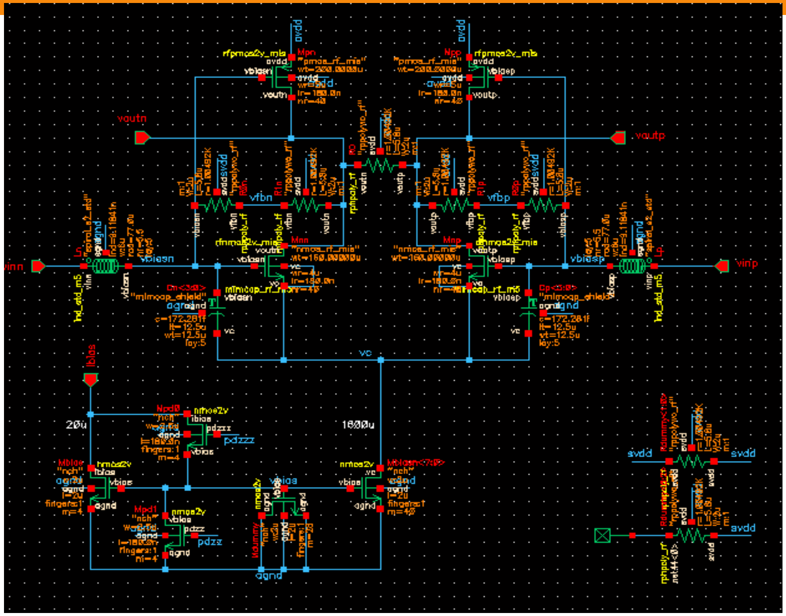
RF Preamp L1 (1.6GHz)

- Differential input
- Requires no external components



		Spec.				
G1575	Gain for 1575MHz frequency	> 12	12.94	14.97	16.86	dB
NF1575	Noise figure for 1575MHz frequency	< 5	1.86	2.59	3.44	dB
S11_1575	Input matching coefficient for 1575MHz frequency	< -12	-16.89	-25.3	-39.89	dB
IIP3	Input referred 3rd order interception point	> -20	0.85	2.51	3.93	dBm

RF Preamp L2 / E5 / E6

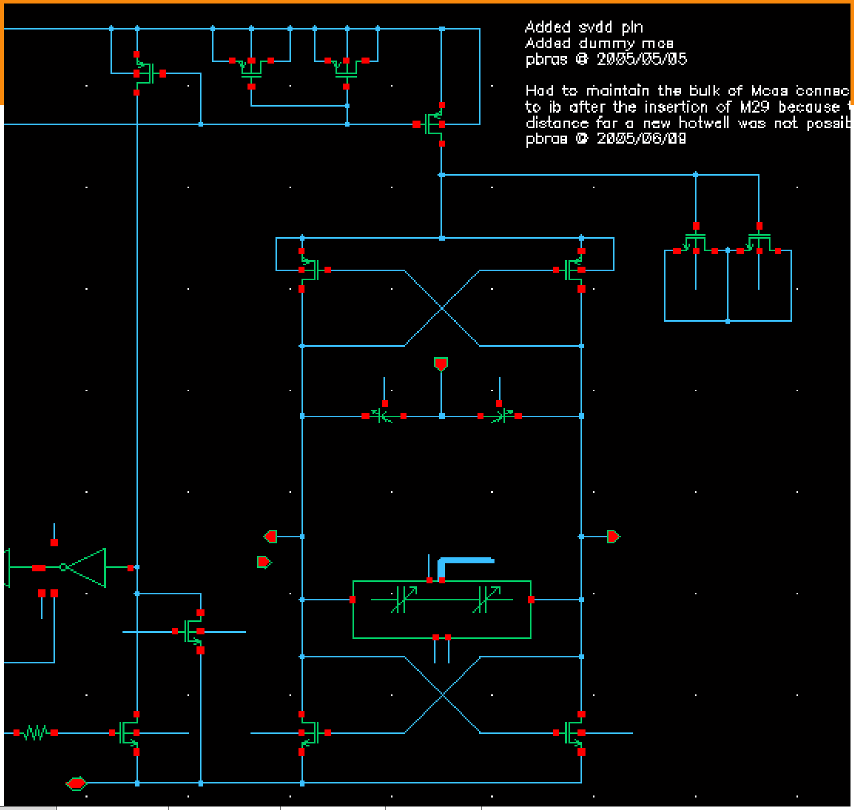


RF Preamp L2/E5/E6

- •Differential input
- •Requires no external components
- •Designed form 1.1GHz to 1.3GHz

		Spec.				
G1150	Gain for 1150MHz frequency	> 14	14.12	16.82	19.42	dB
G1300	Gain for 1300MHz frequency	> 14	14.06	16.33	18.39	dB
NF1150	Noise figure for 1150MHz frequency	< 4	1.91	2.67	3.56	dB
NF1130	Noise figure for 1300MHz frequency	< 4	1.87	2.63	3.58	dB
S11_1150	Input matching coefficient for 1150MHz frequency	< -9	-27.45	-16.36	-10.97	dB
S11_1130	Input matching coefficient for 1300MHz frequency	< -9	-48.53	-25.12	-16.8	dB
IIP3	Input referred 3rd order interception point	> -30	0.257	1.91	3.34	dBm

CHIPIDEA®



1.4GHz VCO

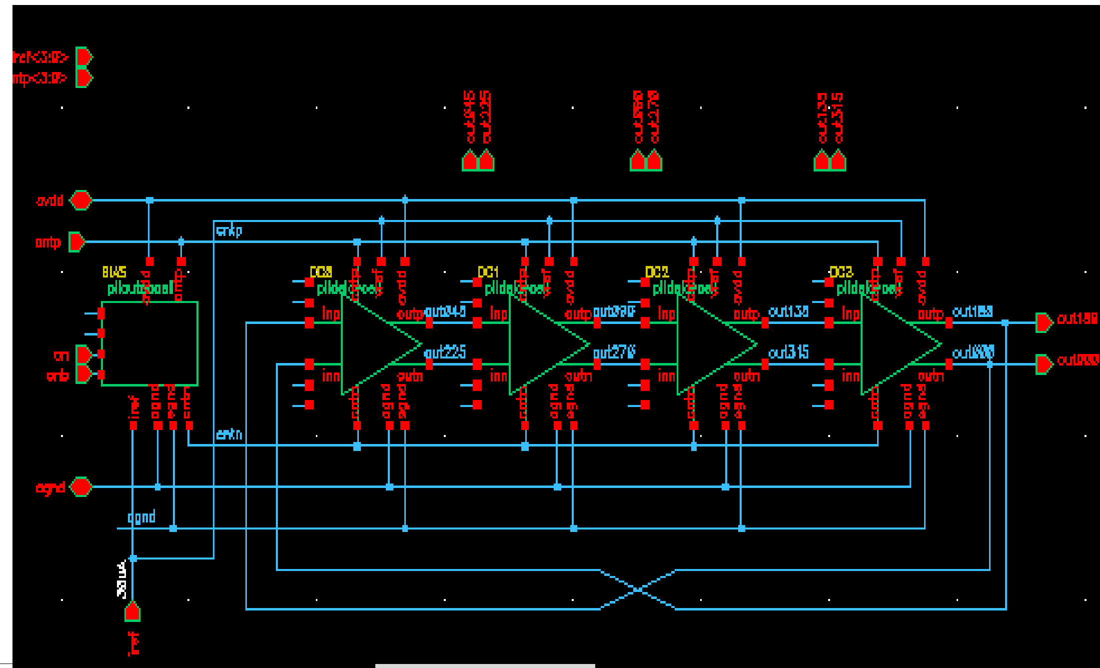
- Programmable capacitors to increase tuning range
- Integrated LC
- Low Phase noise

		Spec.				
VCO_Idc	VCO current consumption	>-2.5e-3	-2.25e-3	-2.11e-3	-1.99e-3	A
VCO_Vpk	VCO output amplitude peak	>0.7	660e-3	877e-3	1.173	V
VCO_dF	VCO gain dF/dV	>50	33.33	373.3	201.8	MHz/V
PhaseNoise	VCO phase noise @ 1K	<-70	-57.55	-55.83	-45.03	dBc/Hz
PhaseNoise	VCO phase noise @ 10K	<-70	-84.96	-83.82	-73.56	dBc/Hz
PhaseNoise	VCO phase noise @ 100K	<-75	-108.1	-108	-100.9	dBc/Hz
PhaseNoise	VCO phase noise @ 1M	<-95	-129	-129	-124.1	dBc/Hz
PhaseNoise	VCO phase noise @ 5M	<-108	-141.3	-141.3	-136.4	dBc/Hz

120MHz-225MHz VCO

120MHz-225MHz

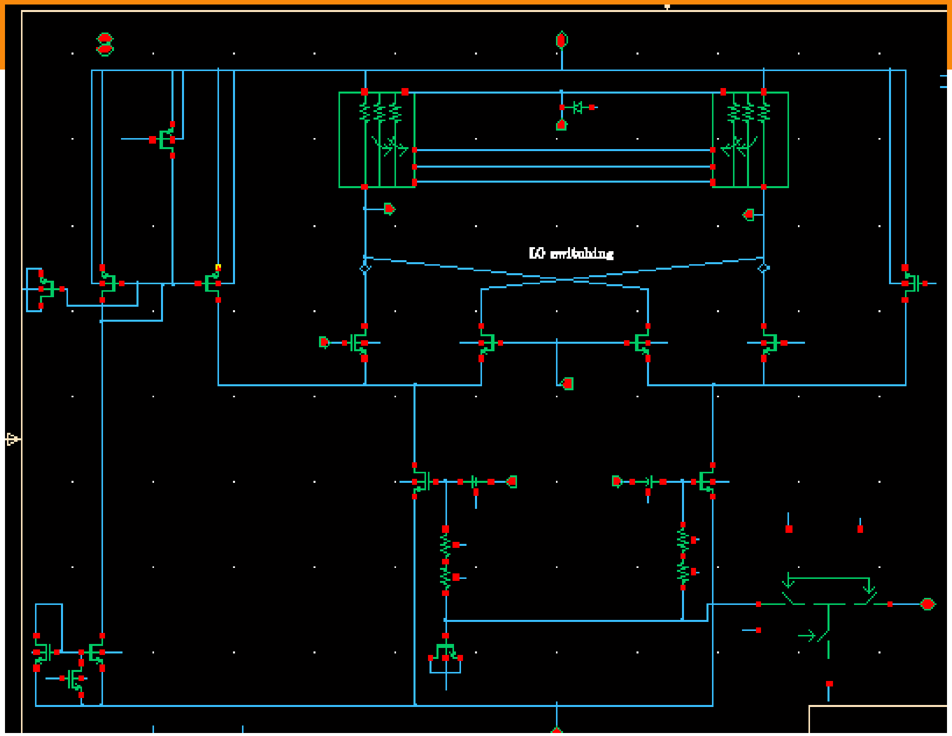
- Four stages ring oscillator
- I & Q phases available



		Spec.				
irmsavdd	VCO consumption	<0.0015	286e-6	306e-6	1.54e-3	A
voutdiff	VCO output amplitude	>0.6	645e-3	829e-3	1.223	Vpp
Kvco	VCO sensitivity	<100e6	-1.27e6	22.9e6	235e6	Hz
PhaseNoise	VCO phase noise @ 100KHz	<-75	-91.12	-88.21	-84.01	dBc/Hz
PhaseNoise	VCO phase noise @ 1MHz	<-95	-112.8	-110	-105.6	dBc/Hz
PhaseNoise	VCO phase noise @ 5MHz	<-108	-129.1	-126.3	-121.8	dBc/Hz
Ioff	Current consumption power down	>-0.1e-6	-687.80e-9	-9.36e-9	-1.67e-9	A

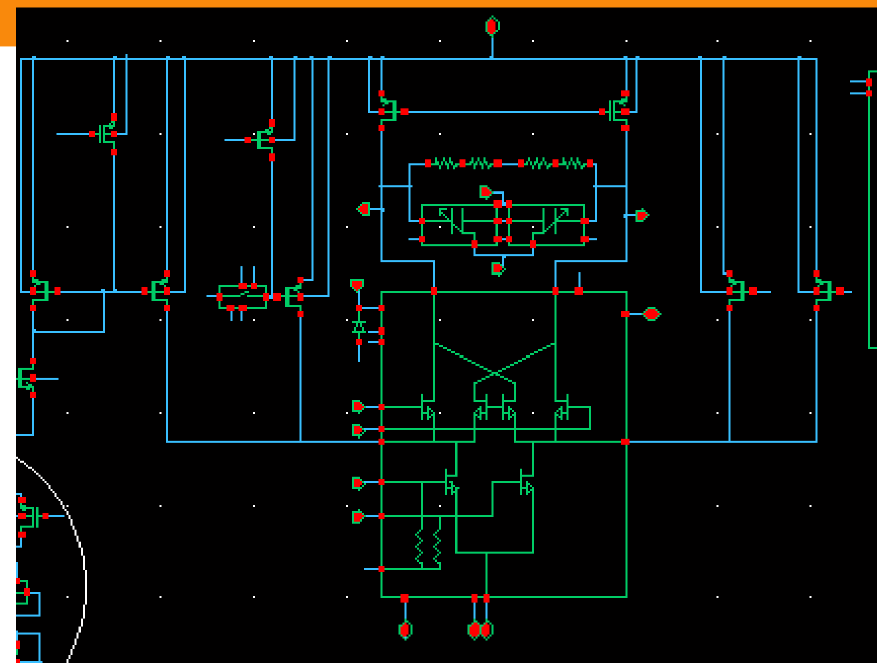
1st Mixer

- **1st Mixer**



		Spec.				
Gc	Conversion Gain	13	8.39	13	17.79	dB
NF	Noise Figure- DSB	18	15.8	17.9	20.1	dB
IIP3	Input 3rd order interception point	-18	-2.76	-0.85	-4.52	dBm
IIP2	Input 2nd order interception point	-	-	-30	-	dBm
Iavddon	Current drawn from avdd in normal operation mode	1.5	1.45	1.51	1.59	mA
Iavddpd	Current drawn from avdd in power-down mode	-	0.1	0.19	0.44	uA

2nd Mixer



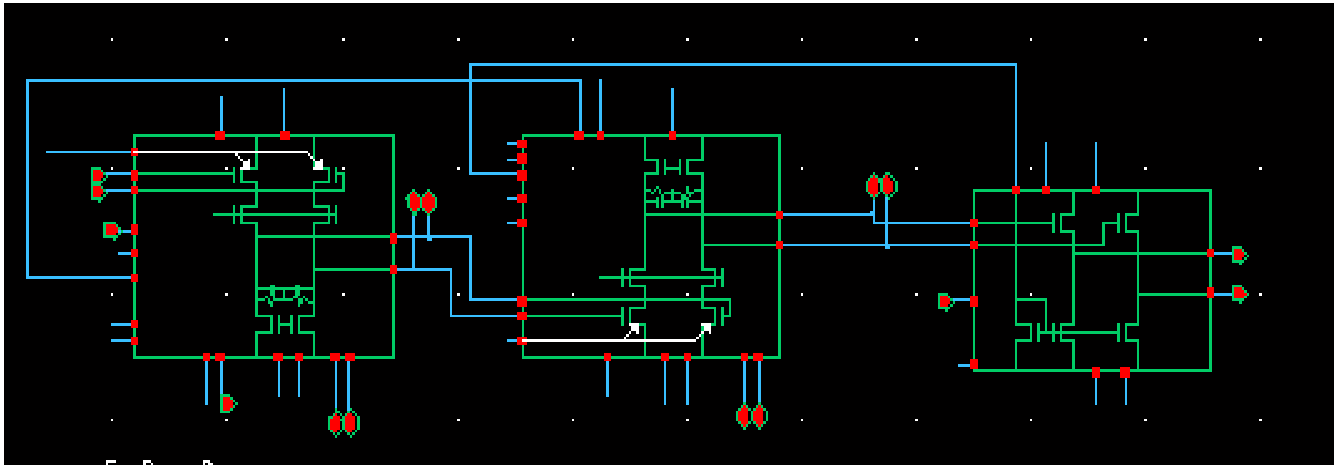
2nd Mixer

- Gilbert Cell
- I & Q for image rejection
- Integrated Filter

		Spec.				
Gc	Conversion Gain	21.5	16.03	19.5	22.86	dB
NF	Noise Figure- DSB	19.5	16.95	18.92	20.71	dB
IIP3	Input 3rd order interception point	-4	-10	-2.97	3.3	dBm
IIP2	Input 2nd order interception point	-		-40		dBm
Iavddon	Current drawn from avdd in normal operation mode	1.5	0.82	0.85	0.89	mA
Iavddpd	Current drawn from avdd in power-down mode	-	0.06	0.14	0.37	uA

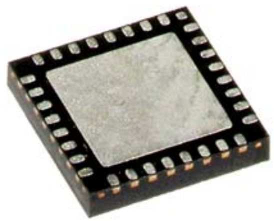
PGA

PGA



		Spec.				
Gmin	minimum Voltage Gain	3	-4.66	2.74	11.20	dB
Gmax	maximum Voltage Gain	51	42.70	49.80	57.30	dB
Gstep	Gain Step	=6		6		dB
NF	Noise Figure @ 10MHz (Max. Gain)	<40	20.08	20.85	21.53	dB
IIM3	IIM3 with maximum gain to allow no distortion at output	TBD	-	-61.73	-	dBV
Iavddon	Current drawn from avdd in normal operation mode (w/out Buffer)	< 1	-	0.52	-	mA

Layout



1. Die

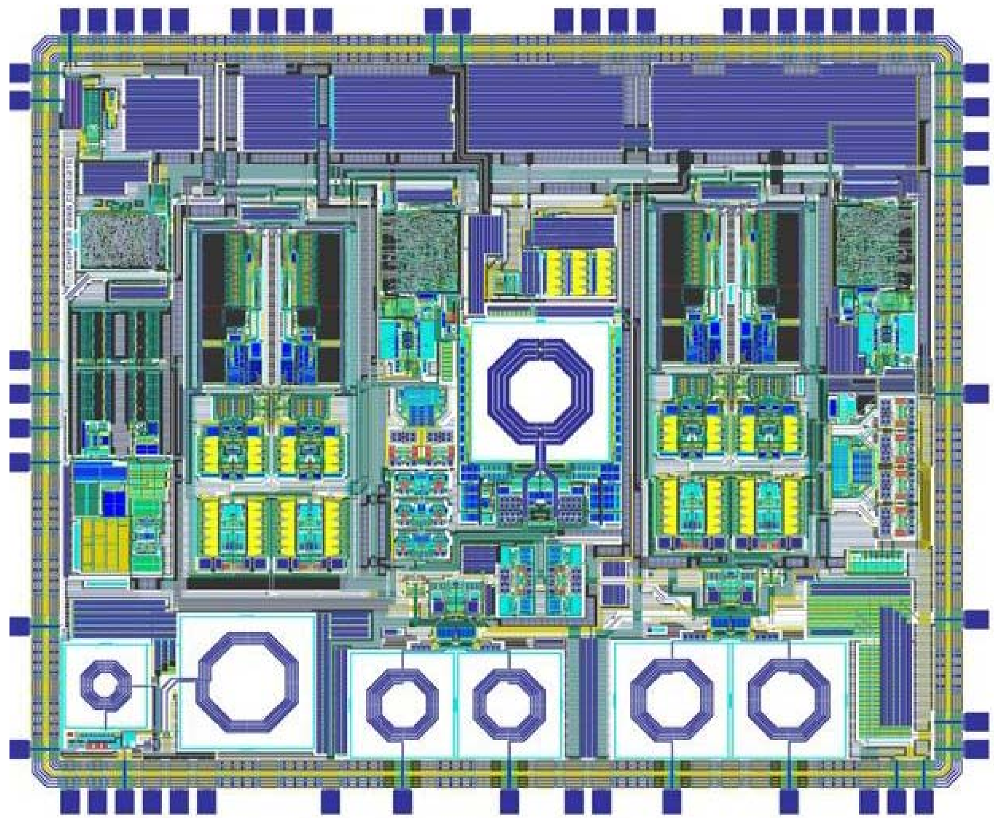
Dimensions in millimeters

Die external dimensions: l , w , t	3000 x 2500x 0.9
Minimum Bond Pad opening area: l , w	53 x 66 [um]
Minimum Bond Pad pitch	80 [um]

2. Package

Dimensions in millimeters

Type	QFN
Number of Pins	32
Pin Pitch	0.5mm
Body: l , w	5mm x 5mm
Body Material	Plastic, RoHS Compliant



Test Overview

- **Test Development**
- **Test Setup Review**
- **Characterization Tests**
  - Power Consumption
  - LNA
  - L1, L2 Complete Chain
  - Phase Noise
  - Sigma-Delta Spurs
  - LPF
  - Channel Isolation
  - IQ Mismatch
- **Summary**

Test Development

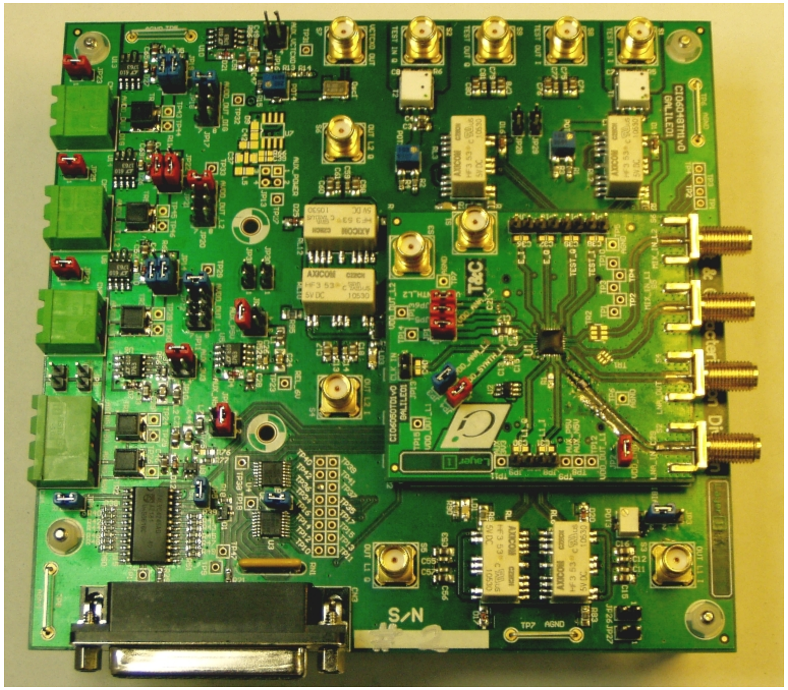
Packaging

- QFN32 for high RF performance

Hardware

- MotherBoard
- DaughterBoards
- De-embedding Boards

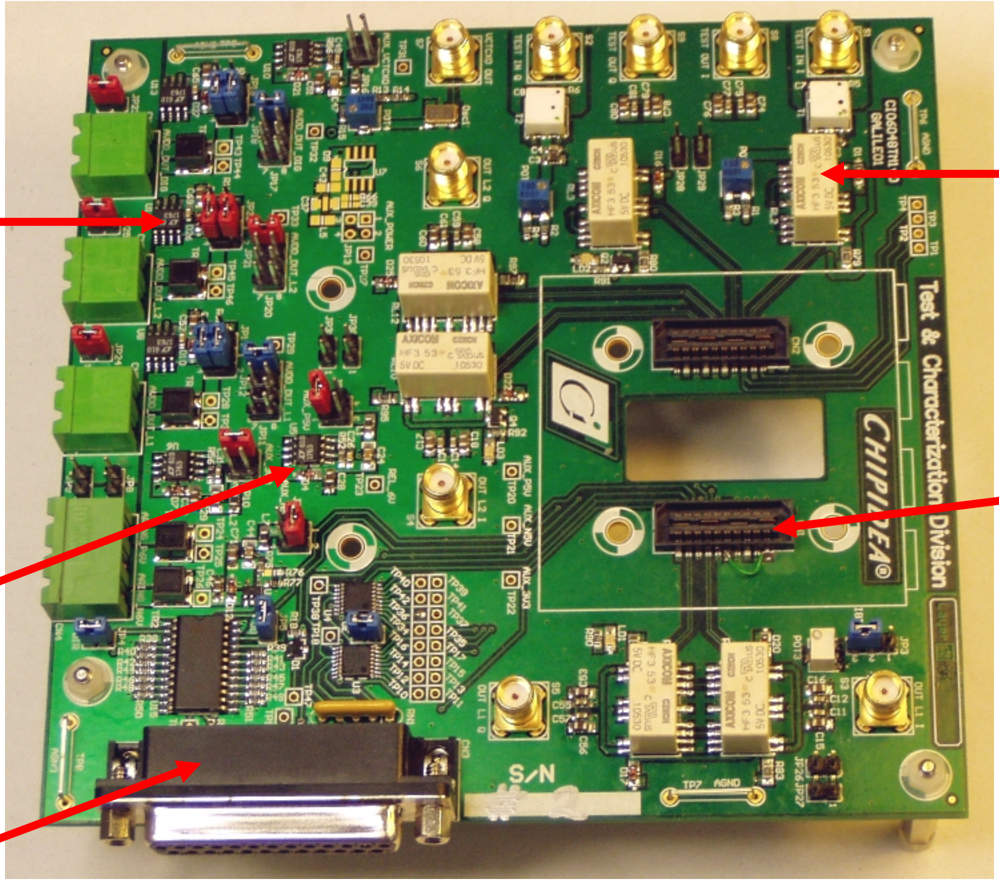
  (SAW Filter, Balun, PCB traces)



Software

- Flexible software Control (I2C)

Motherboard



Programmable power supplies and DUT biasing

Buffers for base-band Interface

I2C – PC communication

Relays for signal switching

DB Interface

Daughterboards

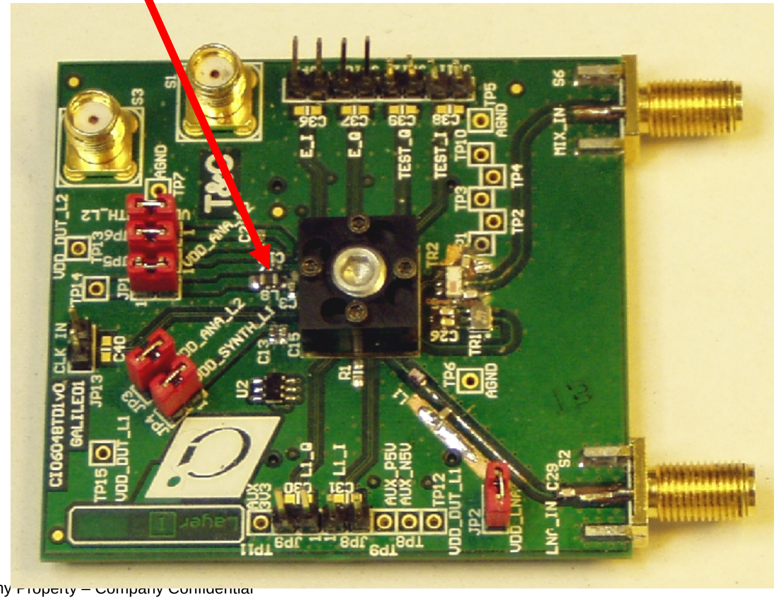
Two Types:

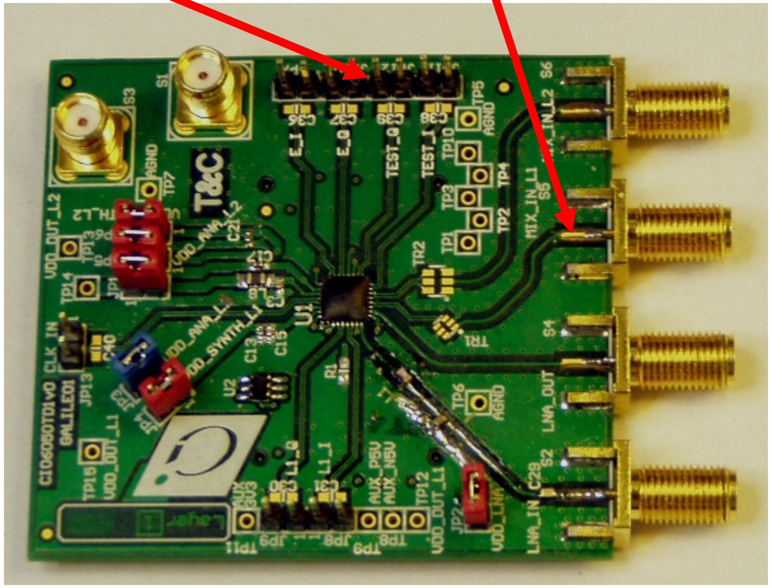
- Type I: with RF QFN socket and SAW filter
- Type II: for direct DUT soldering and LNA charactertization

RF signal routing

Test buffers access

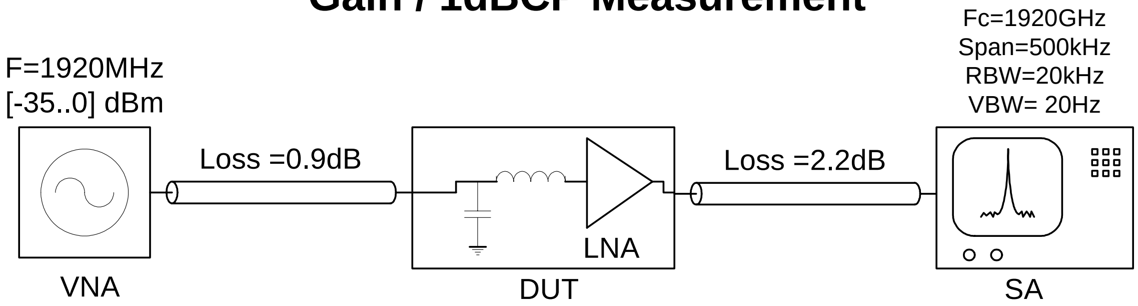
Power supply decoupling



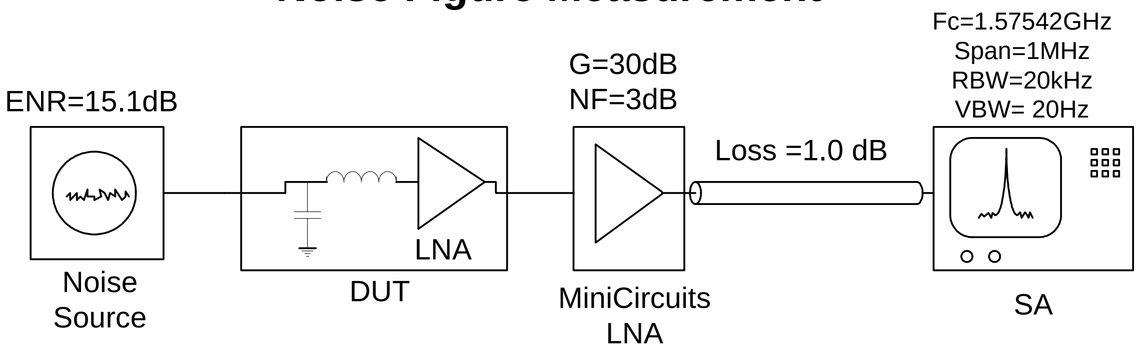


Test Setup: NF, 1dBCP

Gain / 1dBCP Measurement

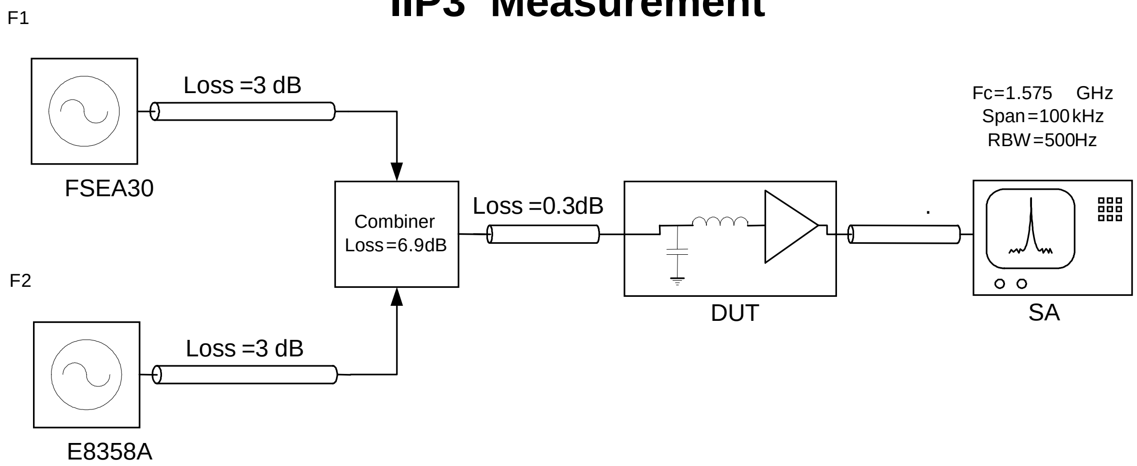


Noise Figure Measurement

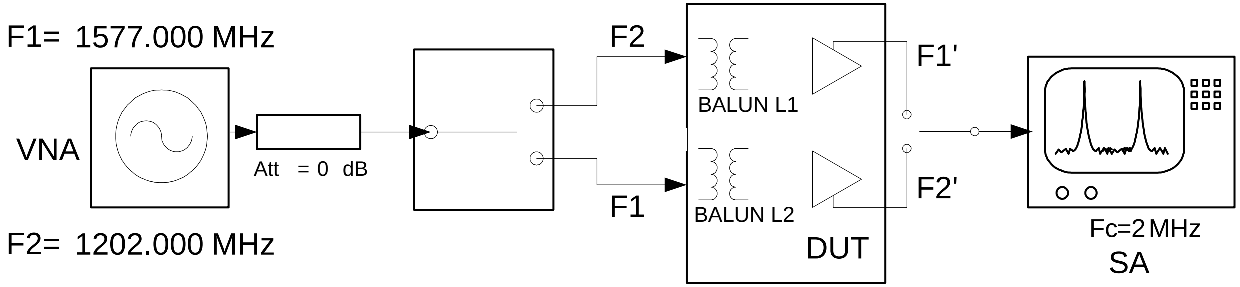


Test Setup: IIP3

IIP3 Measurement



Isolation between channels



F1' = F1 down converted to Bbi,q
F2' = F2 down converted to Bbi,q

Test – Power Consumption

Setup:

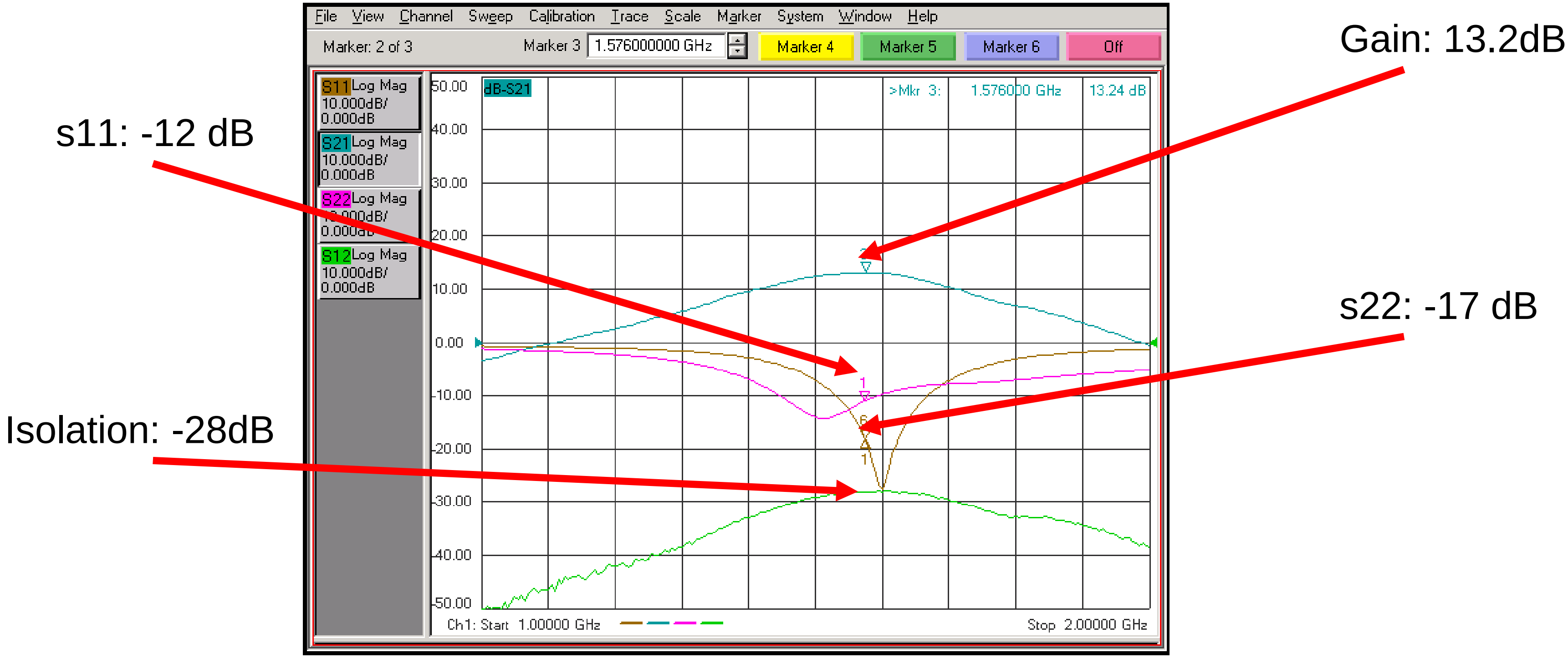
- Using standard lab Power Supplies and intercepting individual power domains of DUT

FIB # 3 / 1.8V	PGAs set to G=12dB				
POWER CONSUMPTION (mA)				Powerdown	
Domain	Measured	MAX. Spec		Domain	Measured
VDD_LNA	3.42	4		VDD_LNA	14 nA
VDD_ANA_L1	14.57	23		VDD_ANA_L1	120 nA
VDD_SINTH_L1	0.515	1.5		VDD_SINTH_L1	22 nA
VDD_ANA_L2	9.84	16		VDD_ANA_L2	10 nA
VDD_SINTH_L2	0.427	1.5		VDD_SINTH_L2	1 nA
VDD_DIGITAL	2.54	4		VDD_DIGITAL	240 nA
TOTAL	31.312	50		TOTAL	<400 nA

LNA – s-Parameters

Setup:

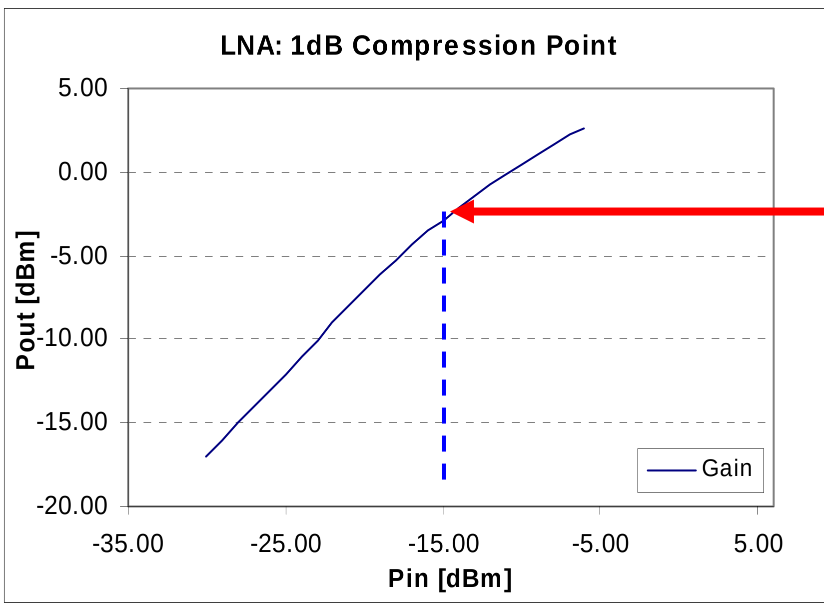
- Calibrated VNA, after LNA input impedance matched (5.6nH Series, 3p3 Shunt)



LNA – Linearity and Noise

Setup:

- LNA input impedance matched (5.6nH Series, 3p3 Shunt)

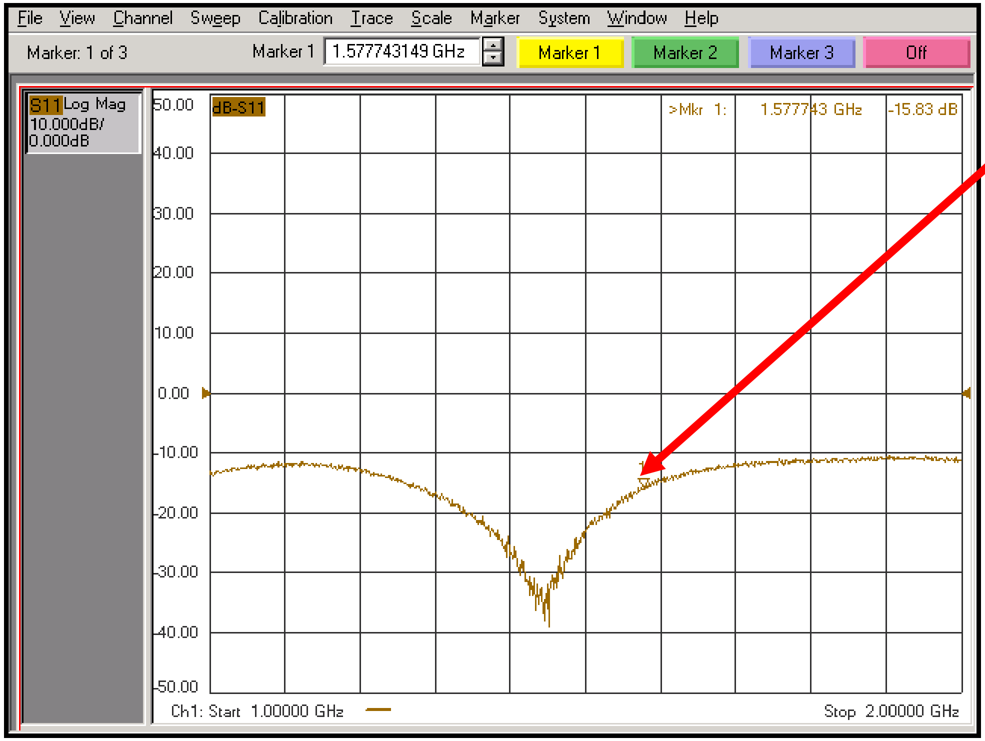


1dBCP: -15dBm

→ **NF=2.5dB (typ)**

LNA: IIP3	
Condition	**IIP3 (dBm)**
Out of Band (f1=1.675GHz, f2=1.775GHz)	4
	5.5
In Band (f1=1.575GHz, f2=1.576GHz)	1.4
	1.4

L1, L2 RF_AMP Input Impedance



S11 OK!

L1 - Complete Chain (RF_AMP to PGA)

Setup:

- G(RF_AMP) = 15dB
- G(RF_MIXER) = 4dB
- G(IF_MIXER) = 20dB
- G(PGA-p, PGA-n): (24,0) or (0,24)dB
- SD=0

Results:

✓ Gain = 52 dB, step OK!

✓ 1dBCP= -52.5dBm

✓ IIP3 = -18.3dBm

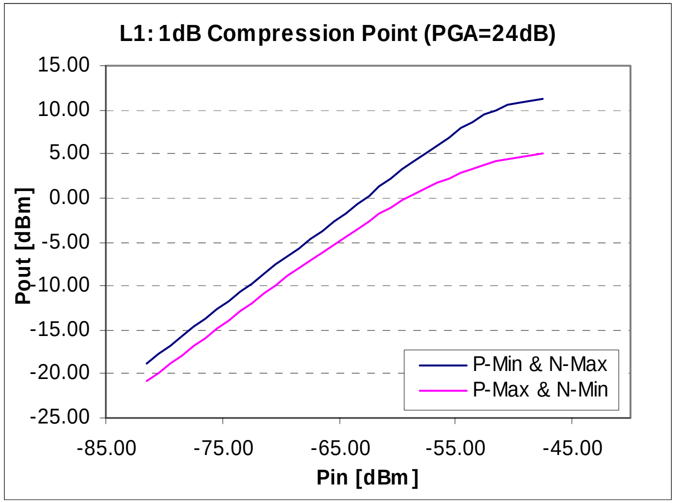
(-35dBm referred to LNA input, spec=-40dBm)

✘ NF = 6.5dB (spec: 5.35dB)

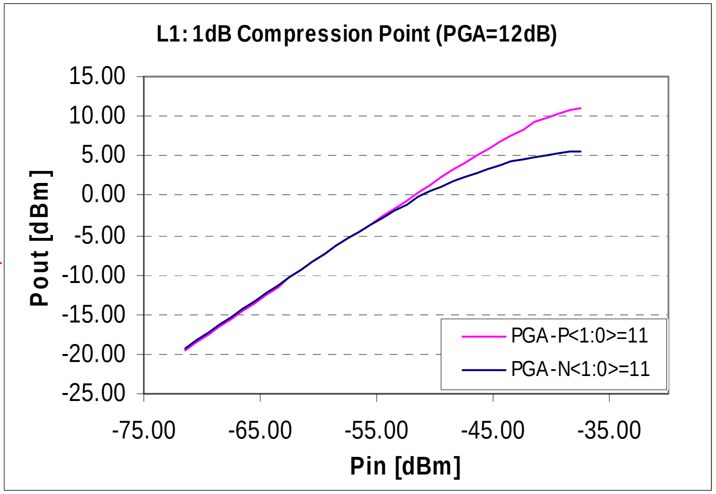
IIP3 Setup:

- f1=1.69 GHz, f2=1.81 GHz
- Pin=-37.5 dBm
- PGA-p=12dB

L1 – Complete chain



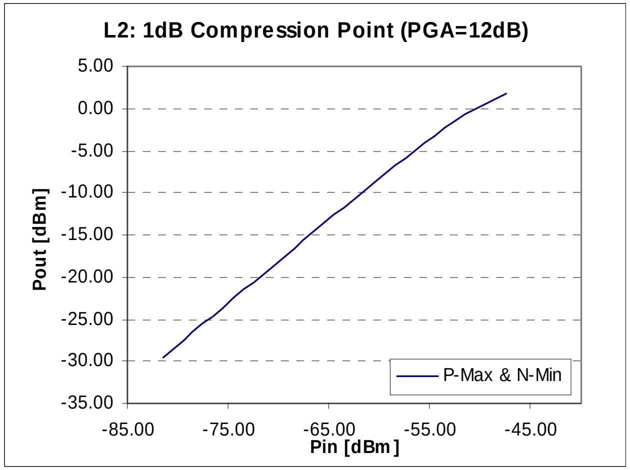
GPGA reduced to 12dB



L2 - Complete Chain

Setup:

- G(RF_AMP) = 15dB
- G(RF_MIXER) = 4dB
- G(IF_MIXER) = 20dB
- G(PGA-p, PGA-n): (24,0) or (0,24)dB
- SD=0



Results:

✓ Gain = 51.8 dB (should be 51dB), step OK!

✓ 1dBCP= -52.5dBm

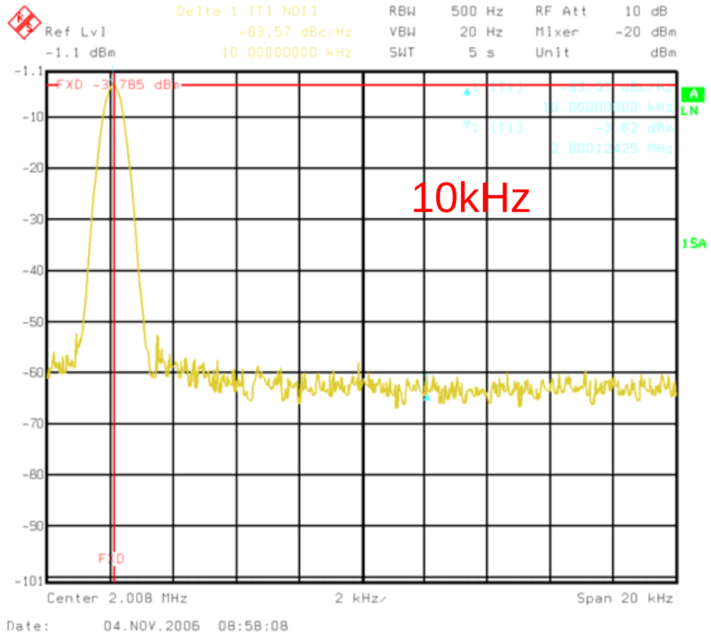
✓ IIP3 = -19.6dBm ←

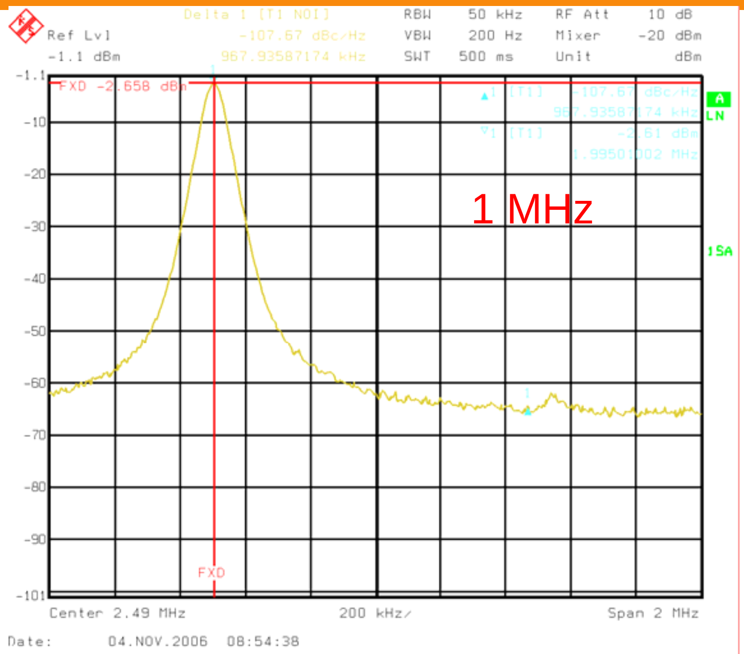
✘ NF = 7.5dB (spec: 5.35dB)

IIP3 Setup:

- f1=1.31 GHz, f2=1.43 GHz
- Pin=-50.0 dBm
- PGA-p=12dB

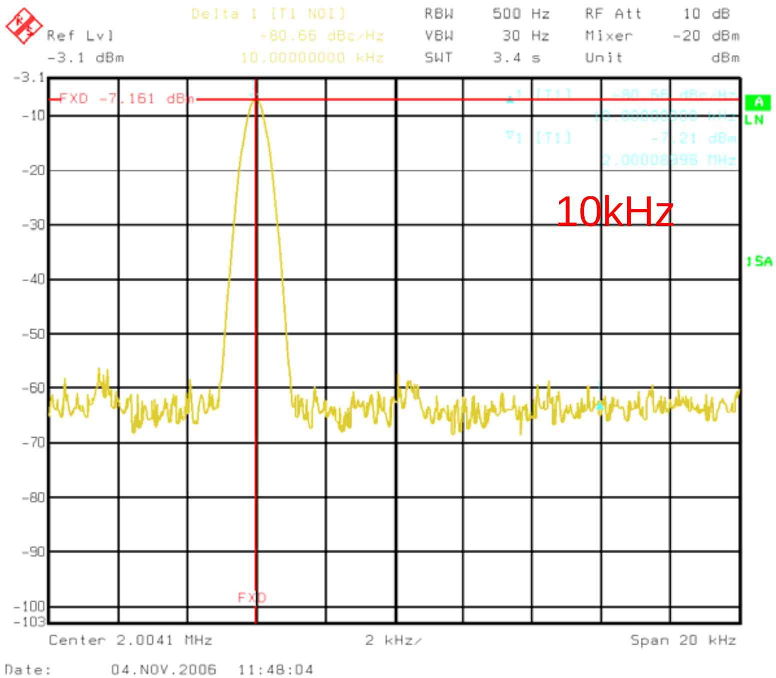
L1 – Phase Noise at Base-band (SD=0)

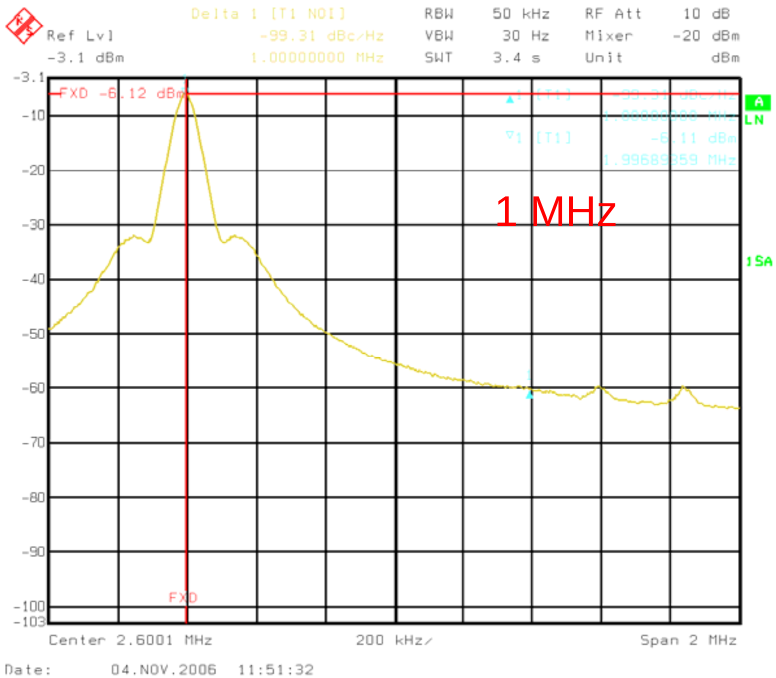




L1 – COMPLETE CHAIN				
Pin @ RF-AMP [dBm]	PGA GAIN	OFFSET	PHASE-NOISE [dBc/Hz]	SPECIFICATION
-51.5	0dB	1 kHz	-77.6	na
-51.5	0dB	10 kHz	-83.2	-70
-51.5	0dB	57 kHz	-75	na
-51.5	0dB	100 kHz	-84.4	-75
-51.5	0dB	1MHz	-107.3	-95

L2 – Phase Noise at Base-band (SD=0)

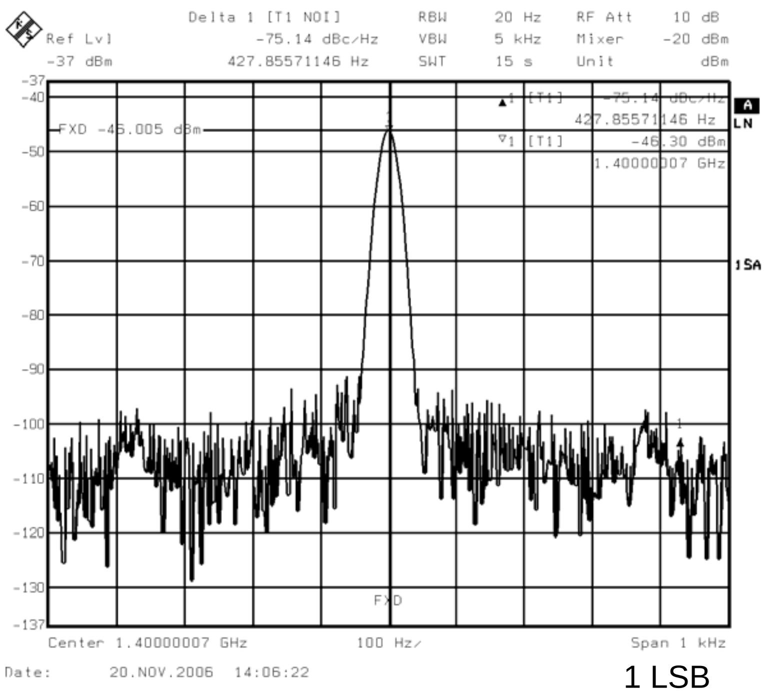


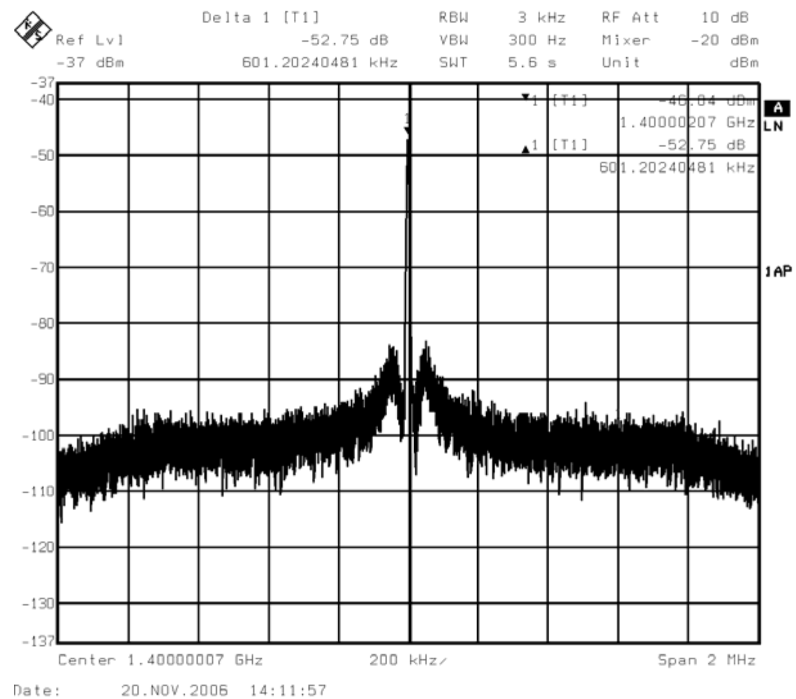


L2: COMPLETE CHAIN				
Pin @ RF-AMP [dBm]	PGA GAIN	OFFSET	PHASE-NOISE [dBc/Hz]	SPECIFICATION
-54	24dB	1KHz	-79.5	na
-54	24dB	10KHz	-81.5	-70
-54	24dB	100KHz	-81	-75
-54	24dB	1MHz	-98.4	-95

SIGMA-DELTA Spurs L2 (Both PLLs)

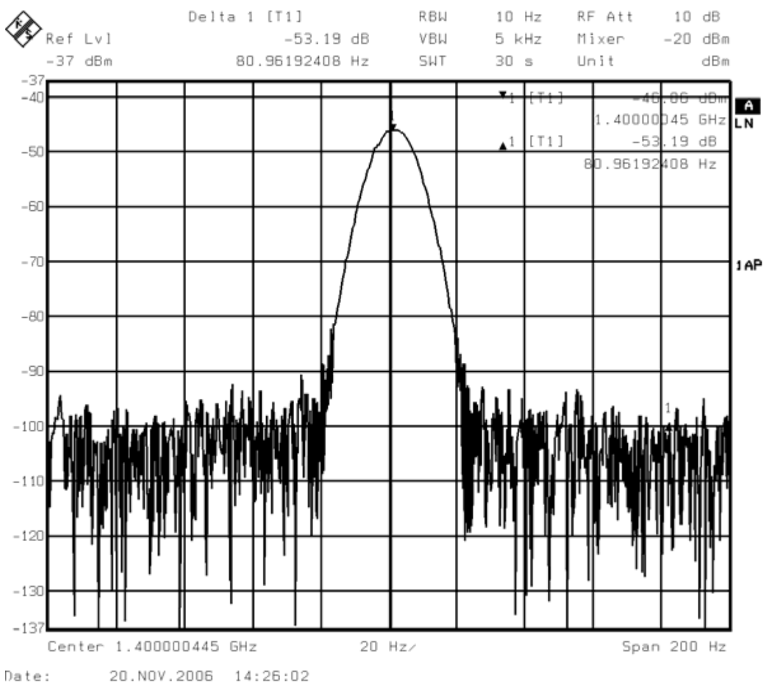
Downconversion measurement from RF_AMP input to PGA Output

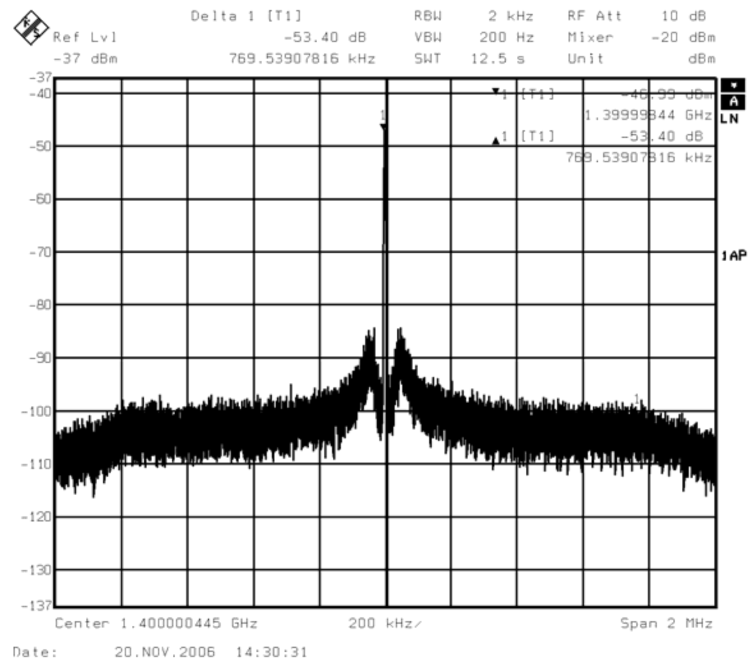




1 LSB
ΣΔ Offset = 2^16
CLCK=24.778761 MHz
Fine tuning 1LSB, step=189 Hz
fLO1=1400 MHz, FLO2=200MHz
MPLL1=7, MPLL2=8

SIGMA-DELTA L2 Spurs Both PLLS (2)

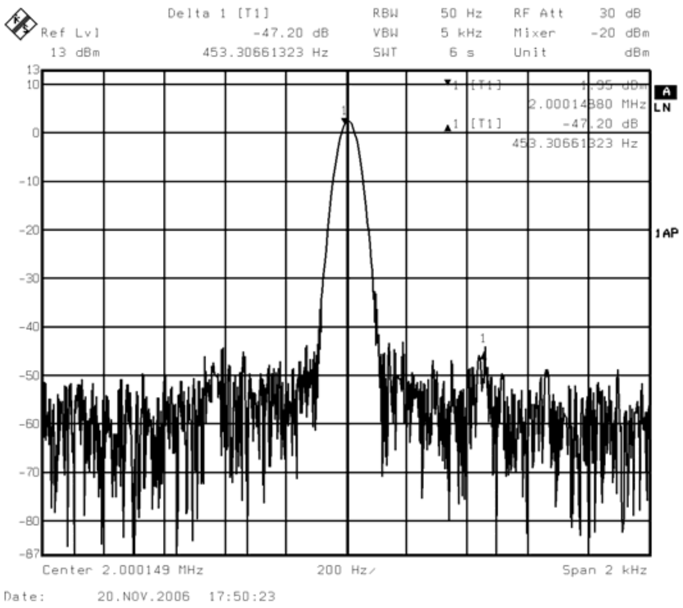


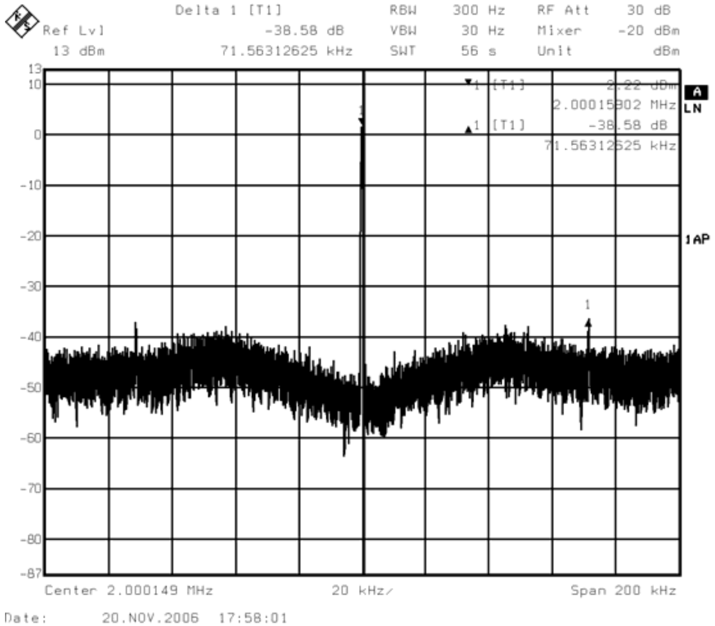


3 LSB
ΣΔ Offset = 2^16
CLCK=24.778761 MHz
Fine tuning 3LSB, step=189Hz
fLO1=1400 MHz, FLO2=200MHz
MPLL1=7, MPLL2=8

SIGMA-DELTA Spurs L2 (PLL2 alone)

Downconversion measurement from RF_AMP input to PGA Output





4 LSB

ΣΔ Offset = 2^16+2^13+2^10+2^7+2^4+2

CLCK=24.778761 MHz

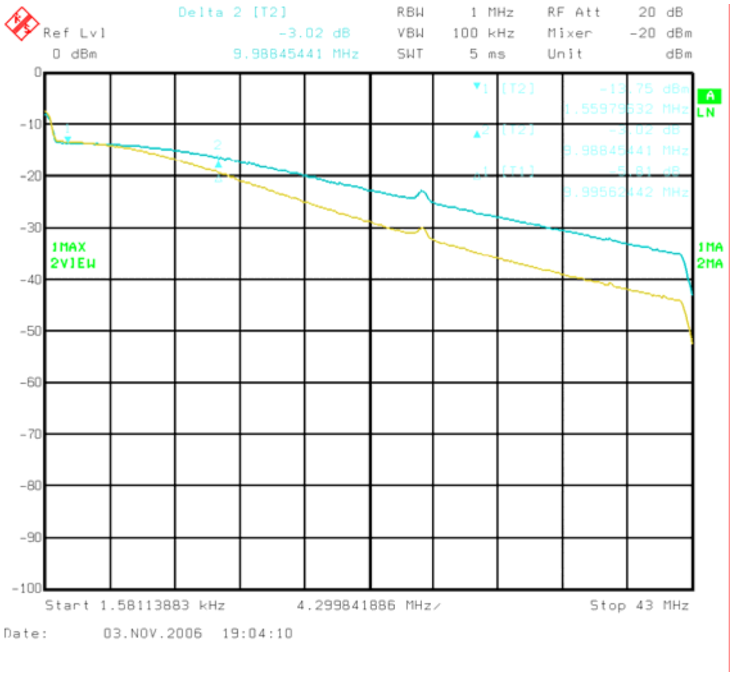
Fine tuning 4LSB, step=23.7Hz

fLO1=1400 MHz, fLO2=200MHz

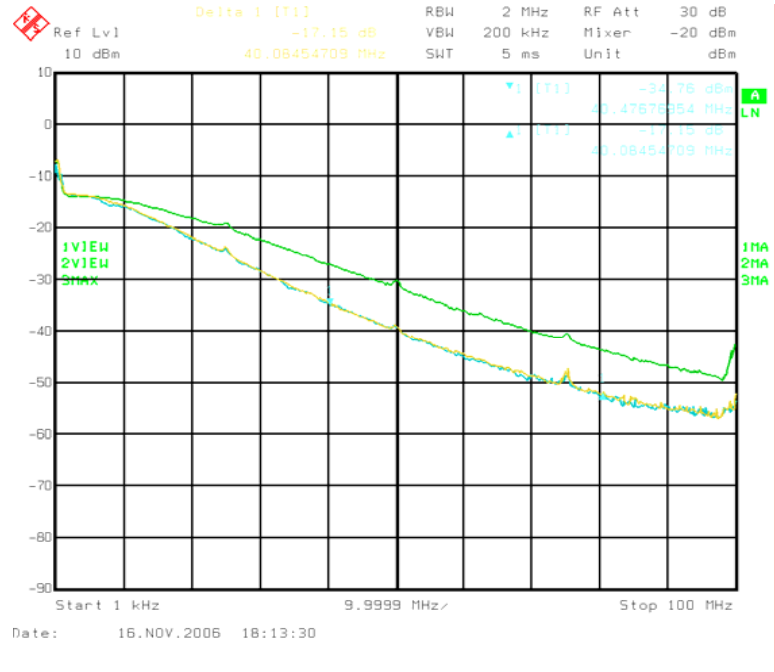
MPLL1=7, MPLL2=8

Lowpass Filters

Measured using test buffers



LPF-BW (L1) with tun=min
(Y-trace=full BW; B-trace=1/2 BW)



LPF (L1) Attenuation
LPF-BW: Y-trace=MIN tun; B-trace=Default tun; G-trace = Max tun

Channel Isolation

Settings:

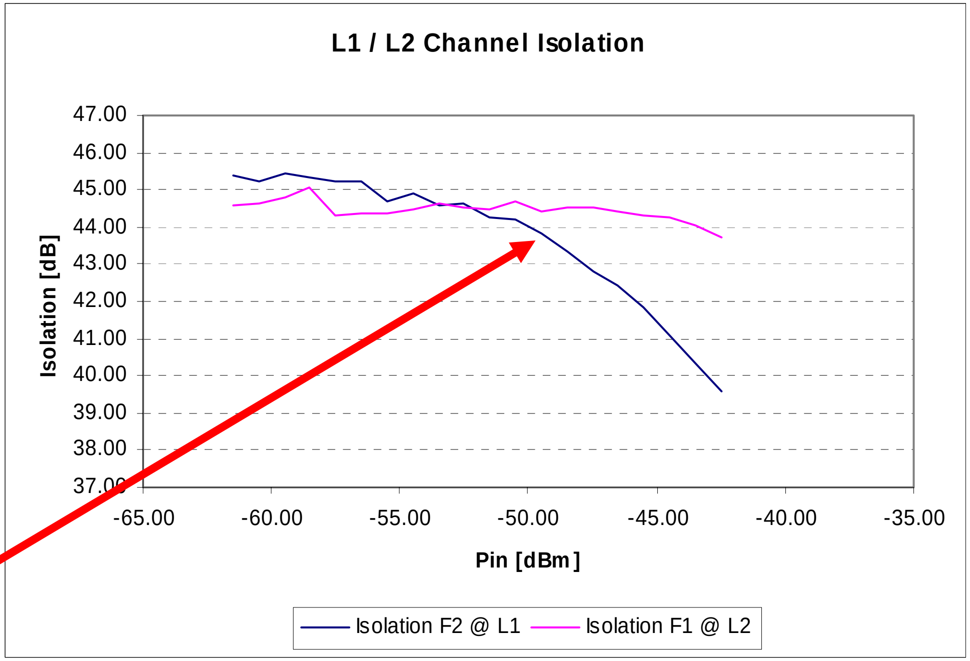
RF-Input Signal:

- •F1=1.577GHz
- •F2=1.202GHz

Input Chain:

- •L1: MIX_IN_L1 (Balun Input - S5)
- •L2: MIX_IN_L2 (Balun Input - S6)

PGA Gain:12dB



On Spec!

IQ Mismatch

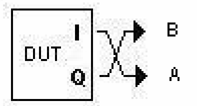
Setup:

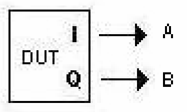
RF-Input Signal:

- •F1=1.577GHz
- •F2=1.202GHz

Test Procedure:

In order to cancel the error in the path of the differential outputs (lines length, differential to single ended buffers…) the channels had been crossed in the following way:

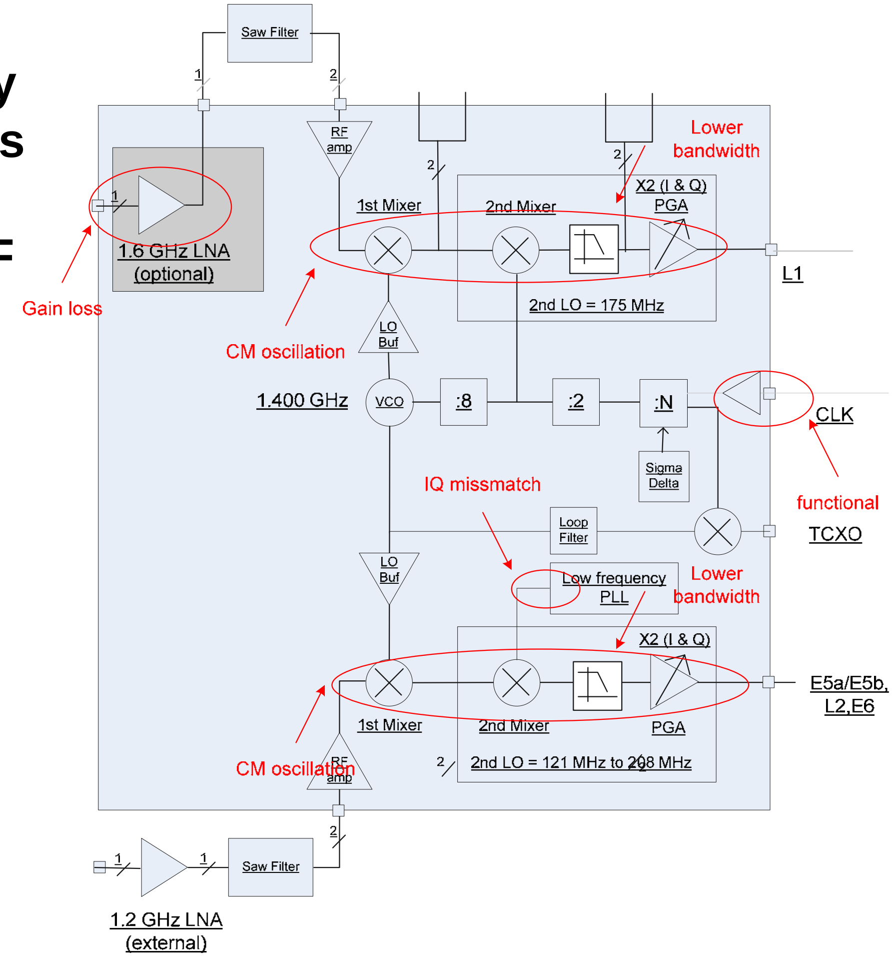




	Phase [deg]			Amplitude [dB]		
	I->A /Q->B	I->B /Q->A	Mismatch	I->A /Q->B	I->B /Q->A	Mismatch
L1	92.4	87.4	2.5	0.174	-0.105	0.14
L2	83.01	96.6	**6.79**	-0.68	0.9	**0.79**

Future Work - Issues and Solutions

- Clock squarer functionality
- Common mode oscillations
- L2 IQ missmatch
- Lower LNA gain, higher NF
- Lower bandwidth



Future Work- Receiver Tests

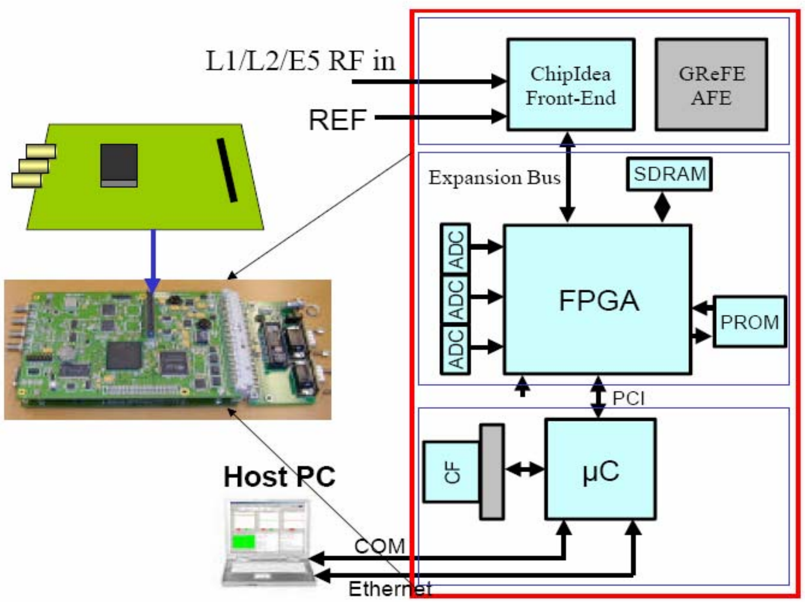


Figure 1-2: GPS/Galileo RX with Chip-Idea front-end

- Feedback to our datasheet and feasibility study.
- Functional Test
- Logging Waveform (offline analysis)
- Interference Tests
- Detailed Navigation Performance Analysis

Future Work - Radiation Tests

Defined typical and worst cases radiation environment to be used as a baseline for the chip testing:

Scenario 1 (“typical”):

- LEO Polar orbit, with 900 Km altitude;
- “Quiet” Magnetic Weather Conditions (no magnetospheric storms);
- Solar Quiet (“no flare”) conditions (absence of solar energetic particle events);
- Solar Minimum cycle (cosmic ray maximum);

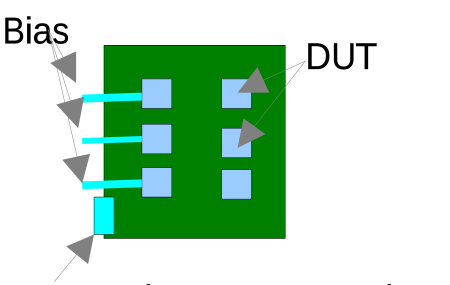
Scenario 2 (“worst case”):

- HEO orbit, with 20 000 Km altitude and 55º inclination (GPS constellation);
- “Stormy” Magnetic Weather Conditions;
- Solar-Energetic Particle (“flare”) conditions (worst-day);

TID testing

- Objectives: Radiation assessment of the chip (TID)
- ESA ESTEC Co-60 facility
- Environment scenarios and radiation level of interest:
  - LEO – 40 kRads
  - MEO – 300 kRads (600kRads)
- Samples to be irradiated - 6
  - •3 biased
  - •3 not biased

Irradiation breadboard



- Proposed Radiation Steps

Radiation level	Total dose (kRad)
M	**3**
D	**10**
E	**20**
F	**40**
R	**100**
A	**300**

- Radiation exposure rate 3.6 kRads/hr
- Other procedures after irradiation:
  - Annealing at room temperature
  - Accelerated aging

•Objectives: Radiation assessment of the chip (SEE)

•*Facilities:*

- •*Heavy-ion Irradiation Facility (HIF)*
- •*RADiation Effects Facility (RADEF)*

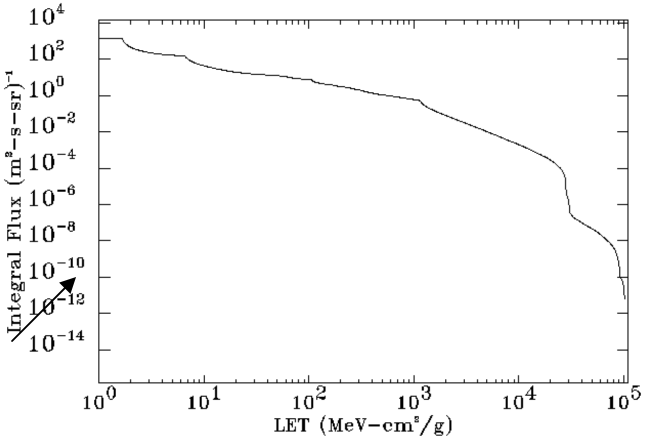
• Environment & experimental testing parameters

- • Environment - CREME96 model

  (ex: LET spectrum for polar quiet; polar orbit,..)

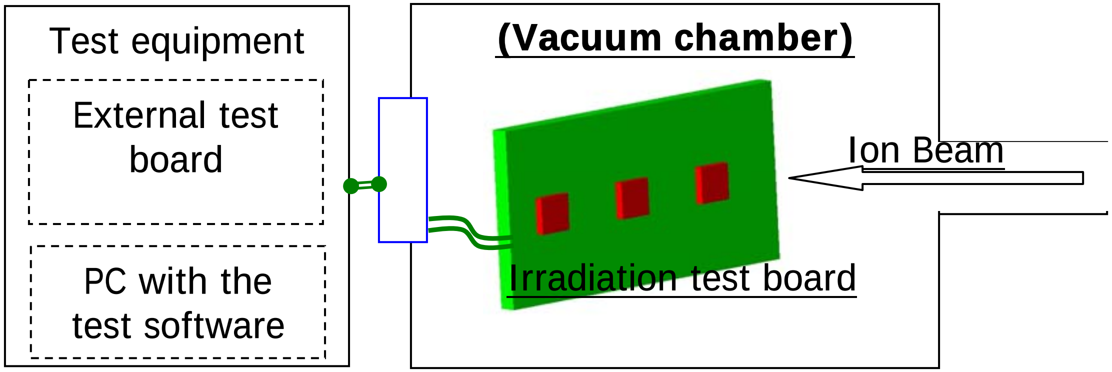
- • Ion cocktail selection in order to simulate the environment;

  (other parameters: Fluence and flux)



• Experimental setup

- • objective: Characterization of the different SEE



Conclusions and directions

- First silicon run finished with very promising results:
  - Architecture validated
  - Performance of most IP blocks validated
- Second silicon run will include ...
  - perfomance tuning and...
  - functional improvements for receiver integration.
- High–end receiver performance tests
- Radiation tests
- High probability of productization complete in 2H2007