GALILEO NSGU

Third Edition of the Microelectronic Presentation Days

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Proposed Agenda

- GSTB-V2 NSGU
- IOV NSGU

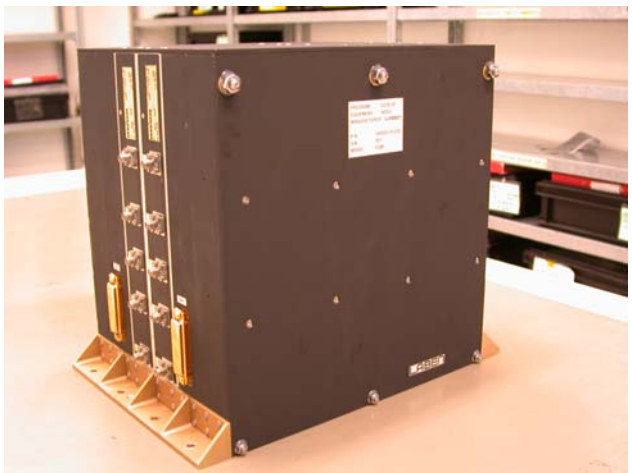
Galileo program phases

Program divided in three main phases:

- GSTB (Galileo System Test Bed)
  - Algorithm & waveform validation
- IOV (In Orbit Validation)
  - Validation of the system at a reduced scale (only 4 satellites among 30)
- FOC (Full Orbital Capacity)
  - Delivery of the full constellation (recurring phase)
  - Under concession responsibility

INTRODUCTION

- **GIOVE-A Navigation signals result from combining PRN codes and Navigation Message Data with dedicated modulation mapping**
- **NSGU offers a high level of flexibility**

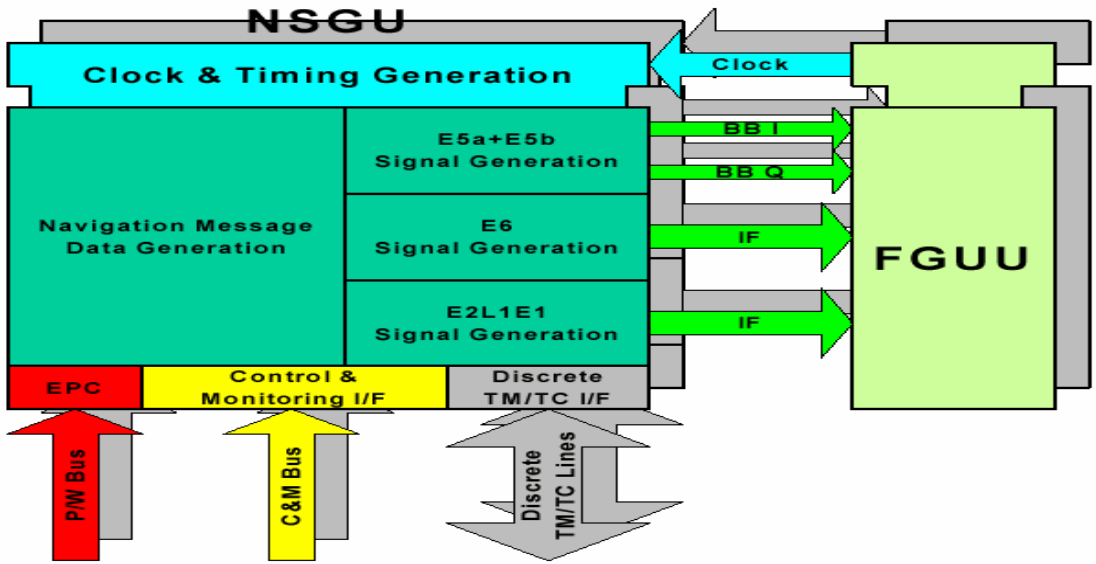


GIOVE-A NSGU
with 2 SGEN modules in the centre of the box

Overview of signals and modulations generated by SGEN module

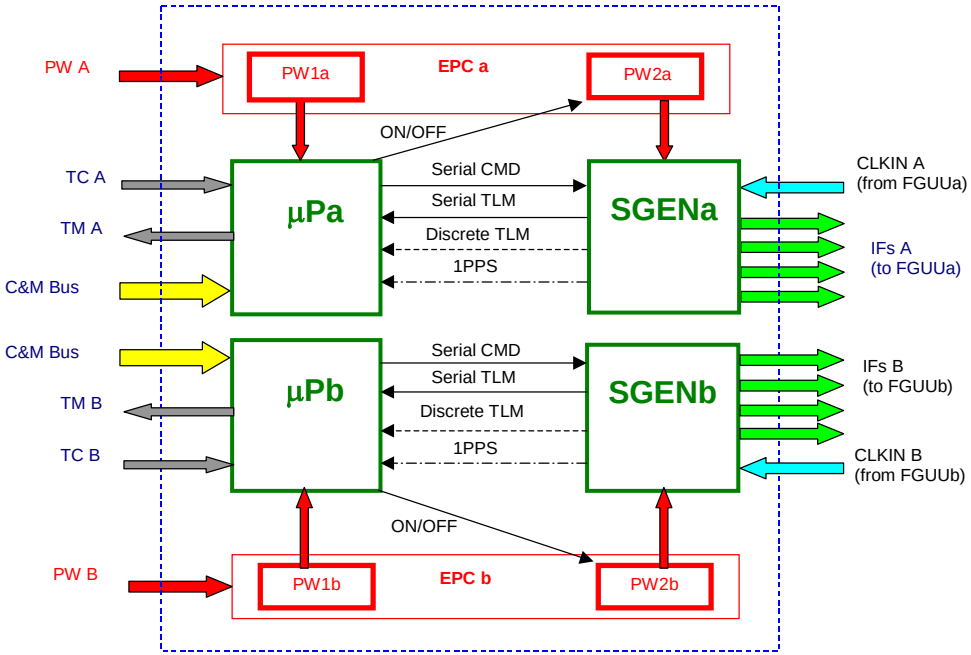
SGEN output signal type	SGEN signal modulation	Navigation message data rate (bps)	Central frequency (bps)	Maximum bandwidth (MHz)
E5AB_I	CW, BPSK, QPSK, BOC(m,n), LINSUM, ALTBOC	E5a : 50 E5b : 250	baseband	35,7
E5AB_Q				35,7
E6_IF	CW, BPSK, QPSK, BOC(m,n), INTERPLEX	E6a : 100 E6b : 1000	30 x 1,023	40
E2L1E1_IF	CW, BPSK, QPSK, BOC(m,n), LOC(14,n) INTERPLEX	E2L1E1a : 100 E2L1E1b: 250	30 x 1,023	40

- **The NSGU equipment is part of the GALILEO payload core and is responsible for the generation of the Navigation Signals**



NSGU and its environment

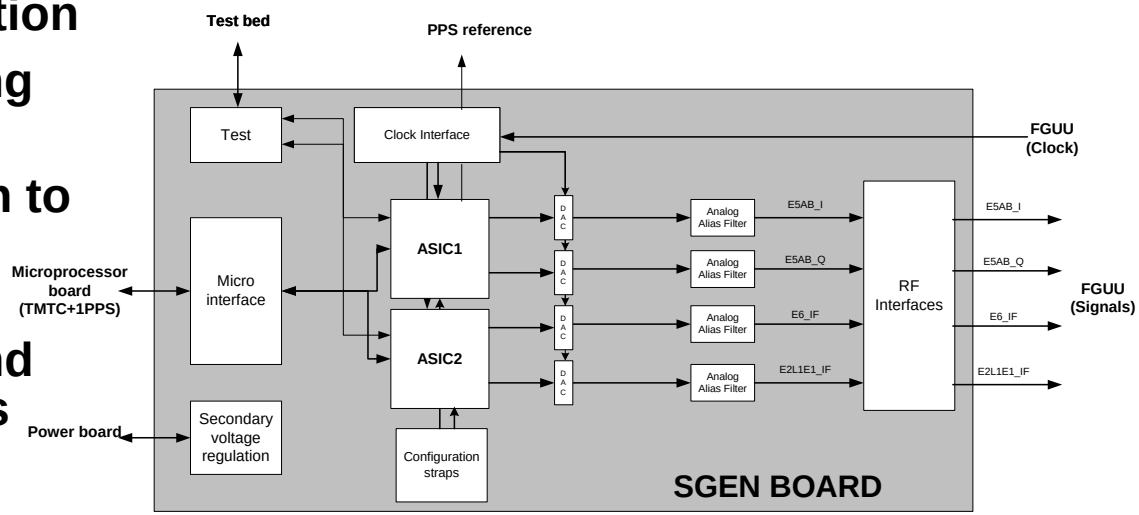
- **The unit includes :**
  - **a µP module in charge of Navigation Message data handling and**
  - **a module named S(ignal)GEN(erator) in charge of the data spreading and signal processing&conditioning up to signal delivering to FGUU.**



NSGU hardware breakdown

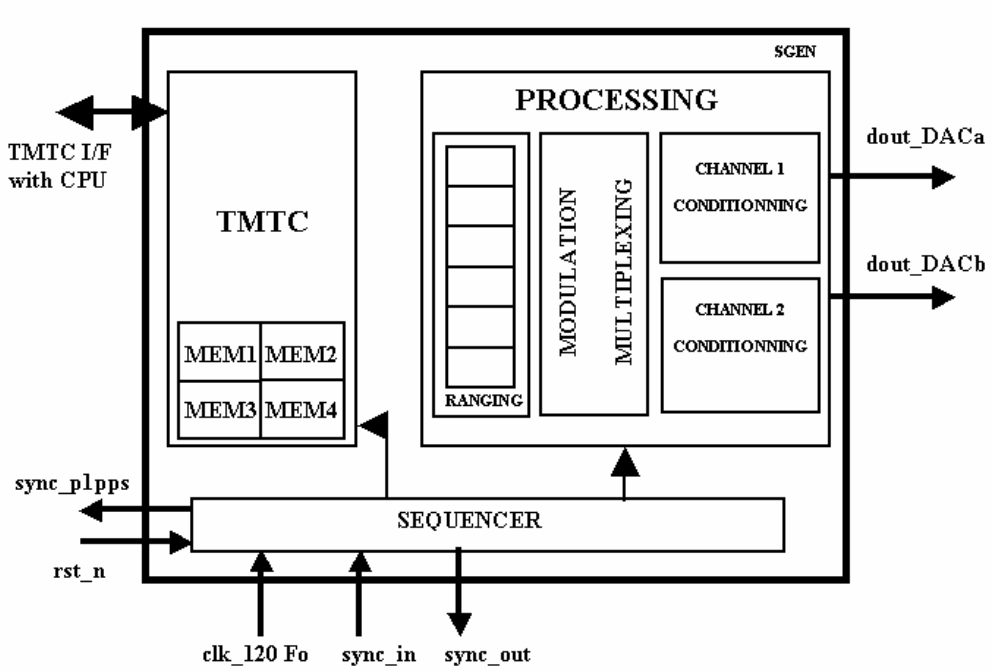
- **SGEN module generates signals from navigation data transmitted by µP module**

- **Main functions of SGEN are :**
  - **Spreading codes generation**
  - **Navigation data spreading**
  - **Digital modulation and eventually up-conversion to IF**
  - **Digital filtering, pre-compensation of DAC and analogue part distortions (amplitude/phase)**
  - **Digital to Analogue conversion**
  - **Analogue output filtering**



Main blocks of ASIC are :

- TMTC
- SEQUENCER
- PROCESSING
  - Ranging
  - Modulation/multiplexing
  - Signal conditioning



SGEN ASIC budget

Name	SGEN (GSTBV2)
Complexity	490 kgates + 53 kbits of memory blocks
Working Frequency	120 fo
Technology	MH1RT (ATMEL 0,35 µm)
Matrix	MH1_156E1 Composite matrix with 4 RAM blocks: 256x48 TPRAM
Package	MQFPF 256
Useful pins	72
Core Power Supply Voltage	3 V
Periphery Power Supply Voltage	3 V
Power Consumption	6 W
Generated Signals (Config. 1)	E5 I and Q
Generated Signals (Config. 2)	E6 and L1

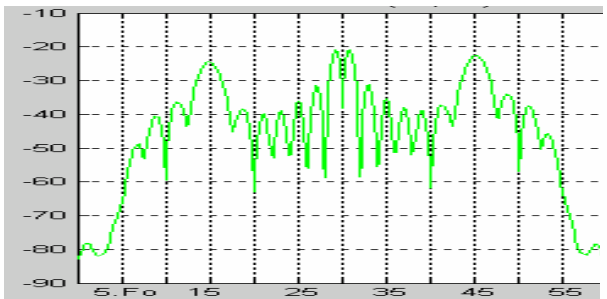
SGEN ASIC challenges

- High data frequency (120 MHz) comparing to ASIC technology 0.35µm
  - Use of retiming for critical data path
    - DC Ultra from Synopsys for logic synthesis
    - Difficulties to manage formal proof
    - Number of FF increased => power consumption increased
- CMOS DAC interface at 120 MHz
  - Difficulties to adjust data to the DAC
  - Worst case analysis at board level very accurately calculated
- ASIC Power consumption
  - First estimations lower than measured worst case power consumption
  - Power supply had to be regulated at 2.85V (+/- 10%) to keep consumption budget

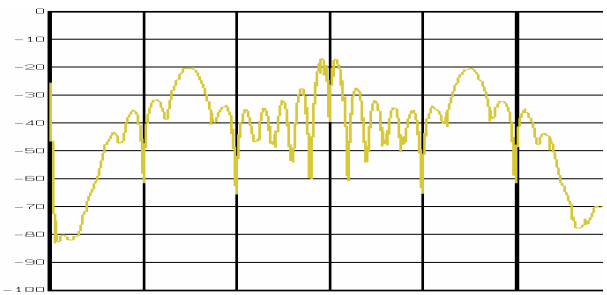
Conclusion

- First run success
  - Fully functional and full performance spec
  - Without FPGA prototyping, in a very challenging schedule
- GIOVE-A launched on December 28th 2005
- First signal transmitted on January 12th 2006

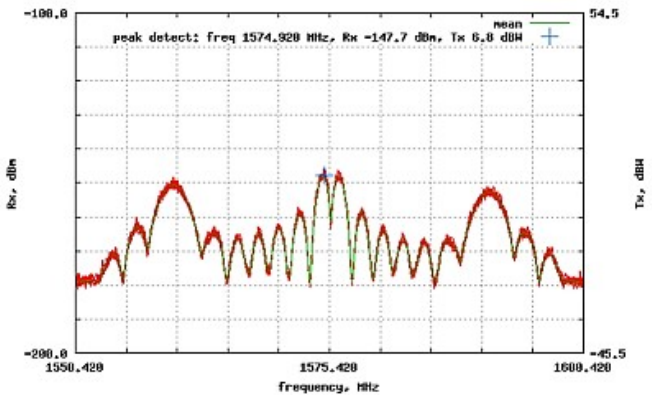
E2L1E1 ABC INTERPLEX [BOC(15,5/2 + BOC(1,1) + BOC(1,1)]
from simulation up to real signal received at Earth station



Simulation during NSGU conception



measurement during NSGU integration



Signal transmitted by GIOVE-A and received at Chilbolton observatory

- IOV NSGU : main evolutions versus GSTB-V2 and consequences on ASIC design
  - PLSU interface for PRS codes providing

    ➔ New interface for the ASIC
  - Capability to compensate analogue distortions for all the payload emission chain (NSGU but also subsequent payload units)

    ➔ New digital filter design
  - Modulation scheme concept going beyond than the GSTB-V2 one
    - GSTB-V2 modulation flexibility is based on predefined modulation schemes associated with flexibilities on codes rates and BOC frequencies
    - IOV modulation flexibility is much more open and offers also a huge flexibility on the modulation scheme for each signal.

    ➔ This new flexible modulation scheme offering a huge amount of possibilities is more consuming in term of complexity and amount of memory

NSGE ASIC : the SGEN new generation

- Use the GSTB ASIC (SGEN) experience feedback to avoid previous development difficulties and manage the new challenges
- Use AAS previous successful experience with Atmel ATC18RHA technology to offer required flexibility

Challenges

- Higher signal generator flexibility and new services
  - Large increase of ASIC complexity
  - ATC18RHA capability widely exceeds the needed amount of gates
- High data frequency (120 MHz)
  - No more a really important difficulty with a 0.18µm technology
  - No more need of complex synthesis optimisation like retiming
- CMOS DAC interface at 120 MHz
  - DAC interface carefully studied and implemented
- ASIC Power consumption
  - ATC18RHA power consumption is 5 to 7 times lower than MH1RT

Conclusion

- NSGE ASIC development is on-going
- Full spec ASIC thanks to ATC18RHA capabilities