ESA IP Cores Service

Current status, activities, and future plans

Kostas Marinis
ESTEC/TEC-EDM
Kostas.Marinis@esa.int

Agenda

- Introduction
- List of available IP cores
- Overview of ESA IP Cores service
- Usage statistics
- Current activities and future plans
  - Current activities : Open Cores Protocol (OCP)

Introduction

- What is an IP core?
  - A reusable design in HDL format (VHDL, Verilog, etc).
  - ESA IP cores are “soft cores”, i.e. technology independent.
    - Can be synthesized and targeted to any ASIC or FPGA technology.
- Why an IP Cores service by ESA?
  - Promote and consolidate the use of functions, protocols and/or architectures for space use (e.g. SpaceWire, CAN, TMTC, etc),
  - Counteract obsolescence and discontinuity of existing space standard ASICs,
  - Facilitate the reuse of results from TRP/GSTP programs, thus reducing costs of large IC developments (e.g. Systems-on-Chip)
  - Centralize IP users’ feedback to improve quality of existing IPs and identify future needs.

List of available IP Cores

- 14 IP Cores available

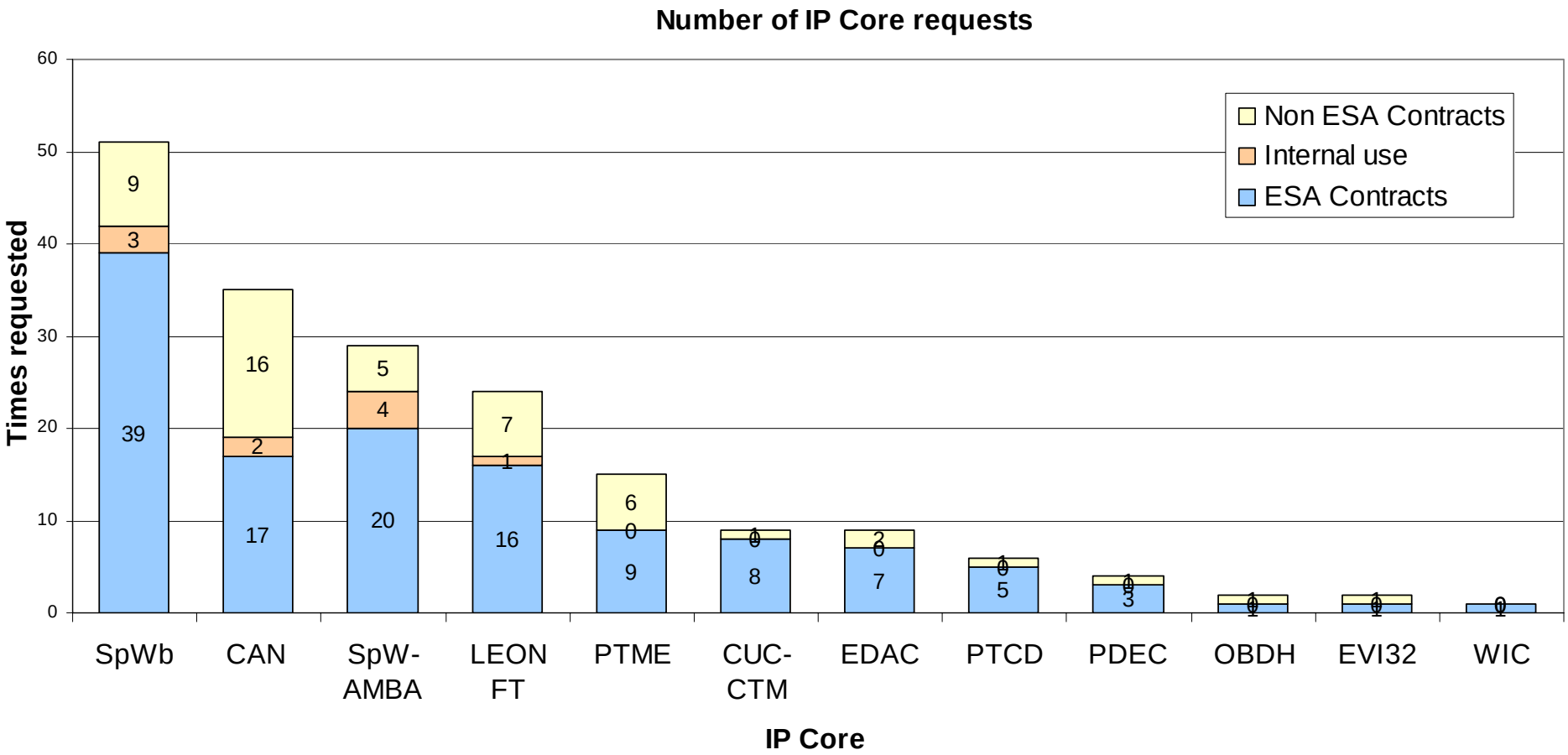
SpW-b	SpaceWire CODEC	**OBDH**	On-Board Data Handling bus
SpW-AMBA	SpaceWire CODEC with AMBA interface	**CUC-CTM**	CCSDS Unsegmented Code (CUC) & CCSDS Time Manager (CTM)
LEON2-FT	32-bit microprocessor (SPARC-compliant)	**EDAC**	Error Detection And Correction Encoder/Decoder
PTME	Packet Telemetry Encoder	**IP1553**	
CAN	Controller Area Network	**EVI32**	32-bit VMEbus interface for the ERC32 processor chip set
PDEC	CCSDS Packet Telecommand Decoder	**WIC**	Wavelet
PTCD	CCSDS Packet Telecommand Decoder. VHDL model of MA28140 chip by GEC-Plessey Semiconductors	**VCA, VCM, TCE**	Virtual Channel Assembler (VCA), Virtual Channel Multiplexer (VCM) and Telemetry Channel Encoders (Reed-Solomon, Convolutional and Turbo Encoder)

- Deliverables with each IP core distribution
  - Documentation
  - VHDL source code
  - Testbenches
  - Simulation and synthesis scripts

Overview of ESA IP Cores service

- How to obtain an ESA IP core:
  - Get details about available IP cores
  - Submit IP request form
  - IP request screening and license preparation by ESTEC/ESA
  - Delivery of requested IP Core(s) to customer
- Pre-compiled simulation models available upon request (for evaluation purposes; no license required!)
- Details and information on ESA IP Cores webpage (TEC-EDM website)
  - http://microelectronics.esa.int/core/corepage.html
    Documents can be downloaded directly from the IP cores website
  - ESA IP Cores website currently undergoing major update and restructuring
    - Announcement of launch date for the new website will be sent via ESA IP User's Forum to all registered users.
    - New site will conform to the standard ESA format/template

Usage Statistics (April 2002 – March 2007)

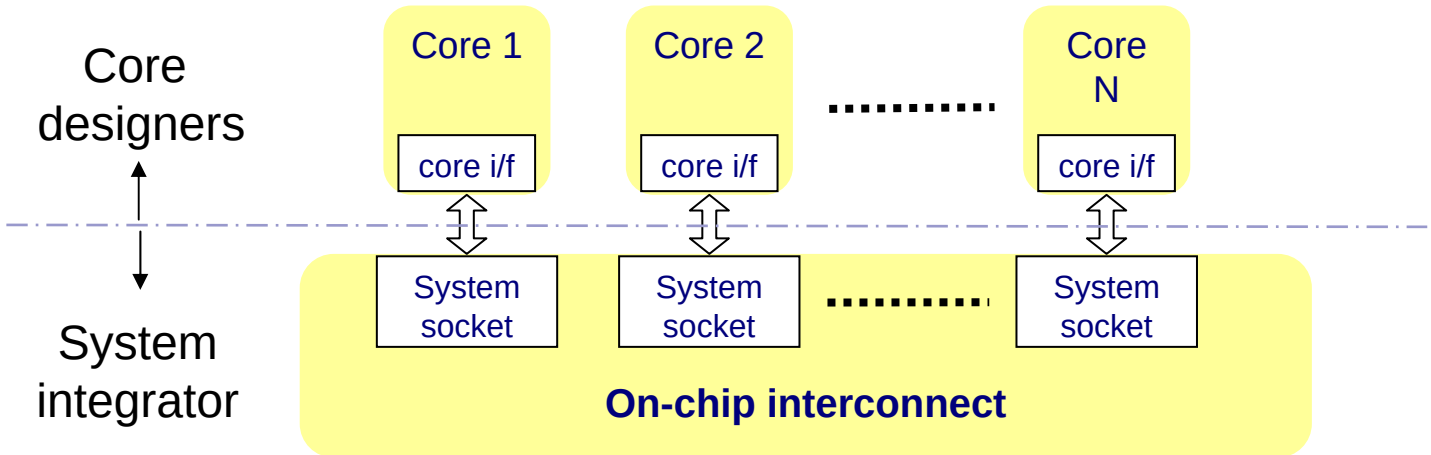


Current activities and future plans

- Open Core Protocol (OCP) compliance
- AMBA interface for UoD SpW-b
- CAN v.5.2 (revised source code + AMBA interface + full documentation)
- LEON2-FT release 1.0.9.16.1 (available on week 11)
- SPIRIT / IP-XACT
  - Investigate suitability, CAD tools support and possible benefits
- SystemC models
  - LEON2 model currently being developed
  - More models required/useful??
- New IP Cores website (coming soon!)
- Suggestions and ideas for new IP cores are always welcome!!

Current activities : Open Cores Protocol (OCP) 2.0

- OCP is a specification for a scalable interface (“socket”-type)
- Emerging as a new standard, already adopted by most major semiconductor and EDA/CAD vendors (Alcatel, Cadence, Mentor Graphics, MIPS, Nokia, Synopsys, Texas Instruments, Siemens, STMicroelectronics, Xilinx …)



Current activities : Open Cores Protocol (OCP) 2.0 - cont'd

- Open Cores Protocol (OCP) 2.0
  - Point-to-point, uni-directional, synchronous
  - Master/Slave, Request/Response model
    - Well-defined, simple roles
  - Extensions
    - Added functionality to support cores with more complex interface requirements
  - Configurability
    - Match a core's requirements exactly
    - Tailor design to required features only
- OCP is configurable to tailor the interface exactly to the features required by the core
  - Basic OCP is very simple
  - Many extensions exist for cores with more complex interface requirements

Current activities : Open Cores Protocol (OCP) 2.0 - cont'd

- Internal work on OCP
  - Stagiaire's project in TEC-EDM (OCP interfaces for CAN + LEON2)
  - Evaluation of tools from OCP-IP (CoreCreator)
  - Feasibility study
- Conclusions
  - OCP can provide benefits and advantages when interoperability and easy adaptation of IP cores and CPUs/DSPs is a major issue.
  - Space segment tends to accept as a "standard" the use of the LEON processor as the core of space SoCs, and AMBA as the interconnection architecture
    - This limits the benefits of using the concept of sockets
    - Therefore, further use of OCP in SoCs for space use is *not justified*

THANK YOU!

QUESTIONS

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Licensing

- Licensing process:
  - Fill out and submit IP request form
  - Internal review of submitted IP request form (approve/reject)
  - Preparation of license agreement by RES-PTE
    - For ESA-funded activities => CCN (Contract Change Notice)
    - For company-funded activities => Stand-alone license
  - Internal approval and signing of license agreement
    - CCNs need to go through a more extended internal approval loop => more delays
  - Distribution of IP core package (via email)

- Full licensing details and info on the website:
  http://microelectronics.esa.int/core/licensing.html

- Technical Officers are requested and expected to assist

Technical Support

- No provision for technical support (according to license agreement)

  We do try to help as much as possible, nevertheless

  - Support provided by ESA staff and contractors with expertise in the some of the ESA IP Cores (SpaceWire, CAN, LEON2, etc).
  - YGTs and stagiaires are also assigned with technical support tasks (investigating reported problems, doing more testing, etc).
  - Support also subcontracted externally
    - University of Dundee (SpaceWire-b)
    - Gaisler Research (LEON2)
    - Aurelia Microeletronica (CAN)

- ESA IP Cores Users' Forum

  http://tech.groups.yahoo.com/group/ESA_IPCores/

  - The more active it is, the more useful it will become!