The COLE System-On-Chip

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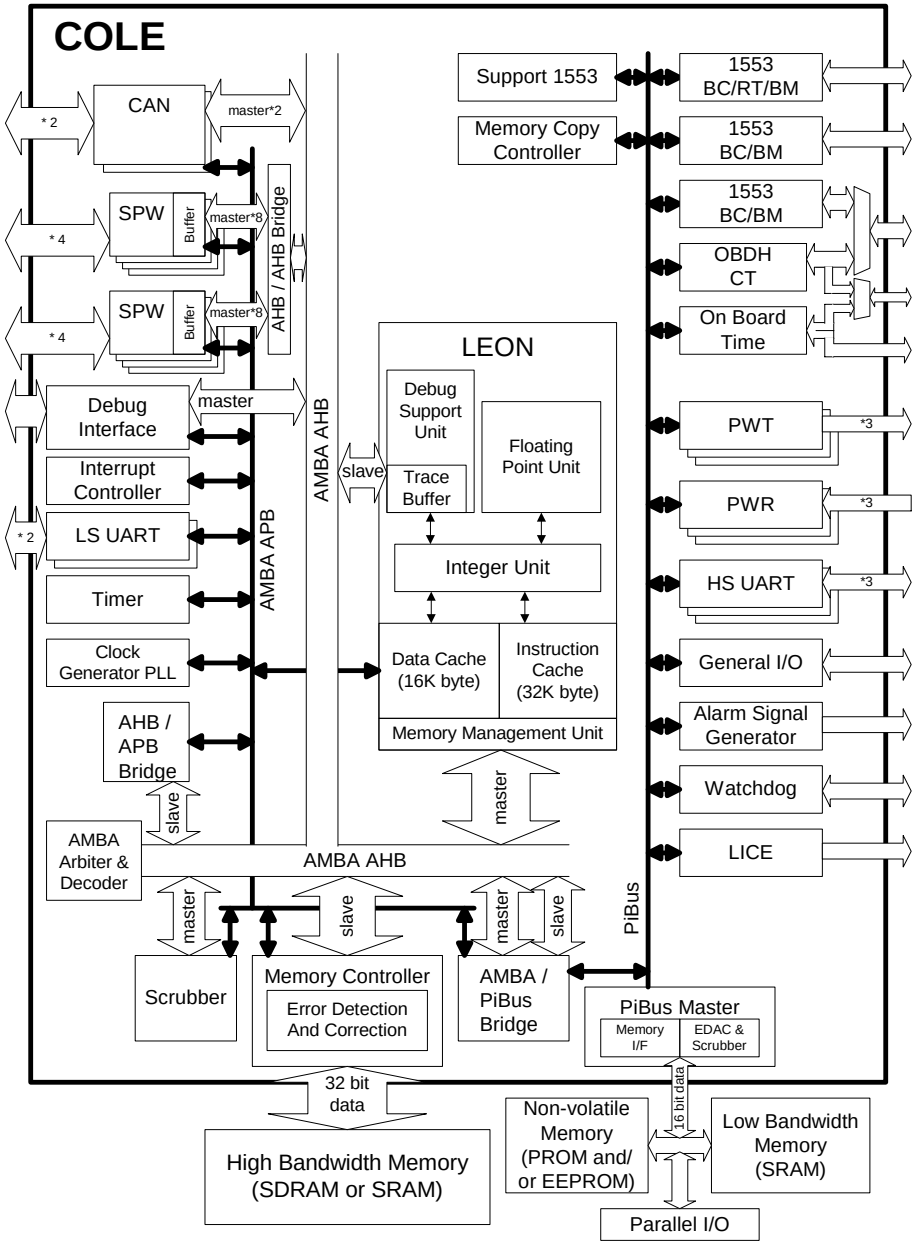
The COLE System-On-Chip

- COLE Overview
- Leon2-FT SPARC V8 processor
- Memory Interfaces
- COCOS, SpaceWire, CAN and LEON I/O
- Panther Processor Board

COLE Overview

- **CO**COS (COmputer COre Support) I/O + **LE**ON2-FT processor = COLE
- New high-speed SpaceWire Links replacing COCOS SpaceWire implementation
- Two CAN buses added
- Atmel ATC18RHA radiation hard 180 nm standard cell ASIC technology
- 3 MGates
- MCGA472 package
- Prototypes available 2007 Q4
- Flight parts 2008


COLE
CAN
* 2
master*2
SPW
Buffer
* 4
master*8
AHB / AHB Bridge
Debug Interface
master
Interrupt Controller
LS UART
Timer
Clock Generator PLL
AHB / APB Bridge
slave
AMBA APB
AMBA AHB
AMBA Arbiter & Decoder
Scrubber
Memory Controller
Error Detection And Correction
AMBA / PiBus Bridge
LEON
Debug Support Unit
Trace Buffer
Floating Point Unit
Integer Unit
Data Cache (16K byte)
Instruction Cache (32K byte)
Memory Management Unit
Support 1553
Memory Copy Controller
1553 BC/RT/BM
1553 BC/BM
OBDH CT
On Board Time
PWT
PWR
HS UART
General I/O
Alarm Signal Generator
Watchdog
LICE
*3
PiBus
PiBus Master
Memory I/F
EDAC & Scrubber
32 bit data
16 bit data
High Bandwidth Memory (SDRAM or SRAM)
Non-volatile Memory (PROM and/ or EEPROM)
Low Bandwidth Memory (SRAM)
Parallel I/O

Leon2-FT SPARC V8 processor in COLE

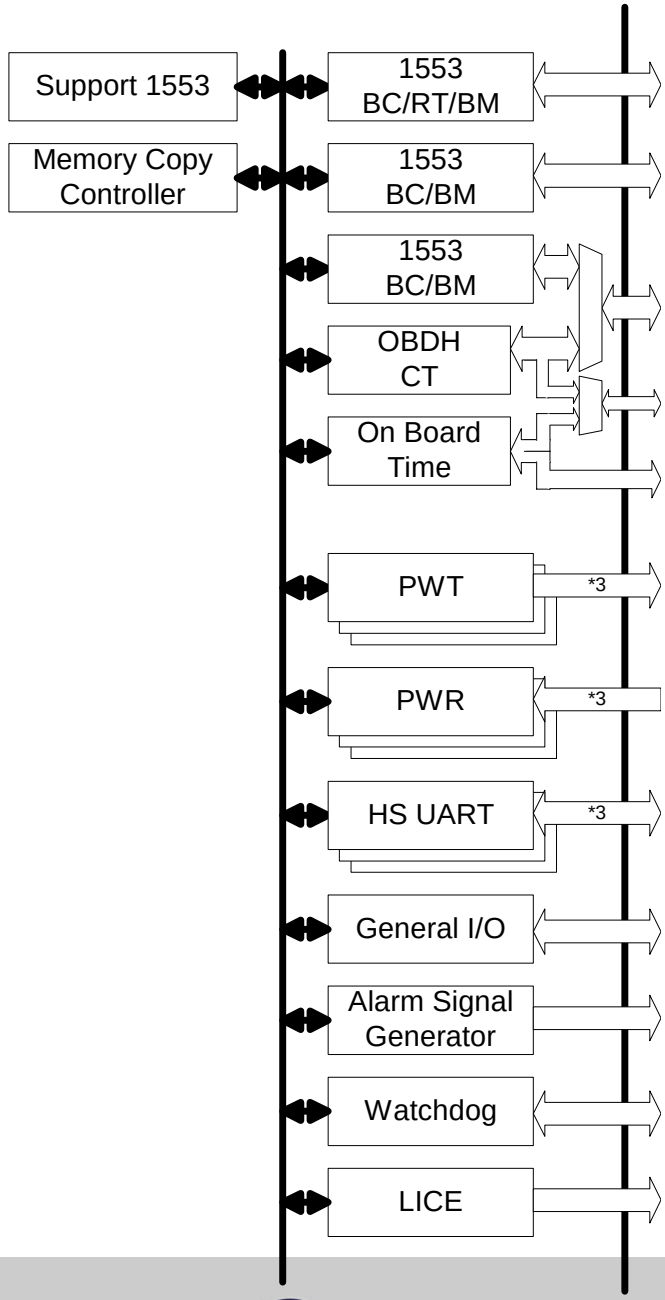
- LEON2-FT Fault Tolerant SPARC V8 processor, 86 MIPS@100 MHz
- Version 1.0.9.16.1, same as planned to be used for Atmel's upcoming AT697F processor
- IEEE-754 Floating Point Unit (FPU)
- SPARC V8 Reference Memory Management Unit (MMU)
- 32 kbytes 4-way set associative instruction cache
- 16 kbytes 2-way set associative data cache
- Extended Debug Support Unit (E-DSU) with 4096 trace lines. Extensions include Trace Buffer compression, real time dumping of Trace Buffer via SpaceWire link and collection of cache statistics.

Memory Interfaces

- High speed memory interface for SRAM and SDRAM with memory scrubber
- Enhanced error detection and correction using a double 4-bit symbol correcting Reed-Solomon code that can detect and handle Single Event Functional Interruption (SEFI), allowing SDRAM to be used as processor memory for applications requiring very large memory
- Low-Speed 8-bit/16-bit memory interface for PROM, EEPROM, communication SRAM and parallel I/O, with EDAC and memory scrubber

COCOS I/O Functions

- Three MIL-STD-1553B bus interfaces
- OBDH bus Central Terminal
- Three PacketWire Receivers and Transmitters
- Three High-Speed UART
- General I/O Interface with 12 I/Os
- On Board Time (OBT) with synch. pulses
- Alarm Signal Generator
- Memory Copy Controller
- Watchdog
- LICE Interface

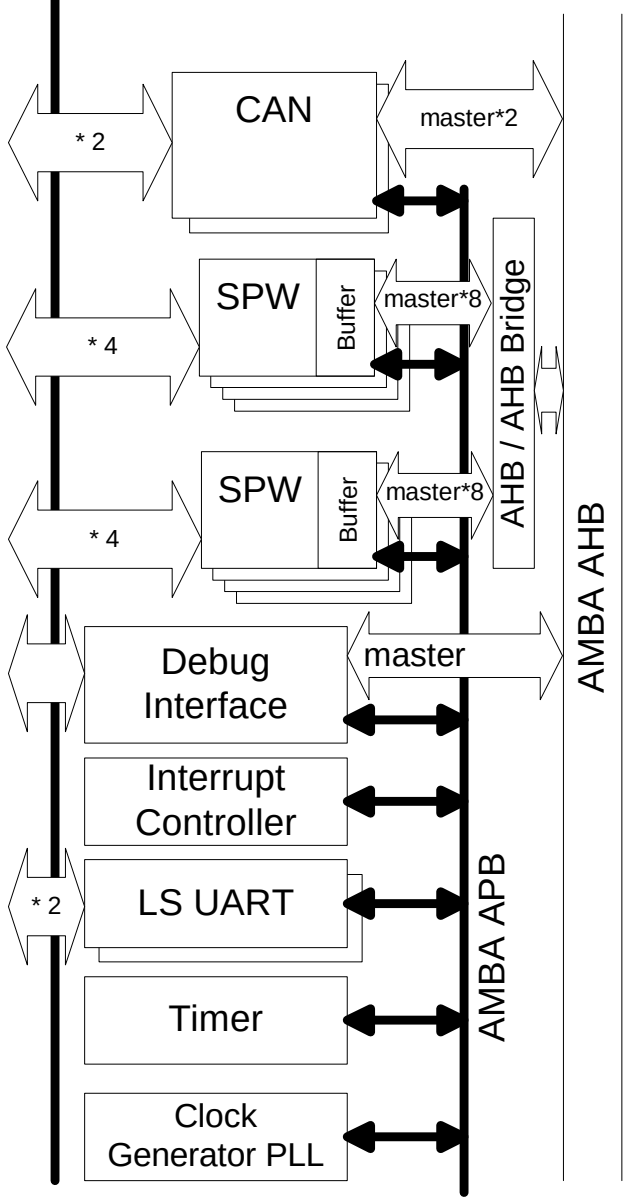


SpaceWire, CAN and LEON I/O

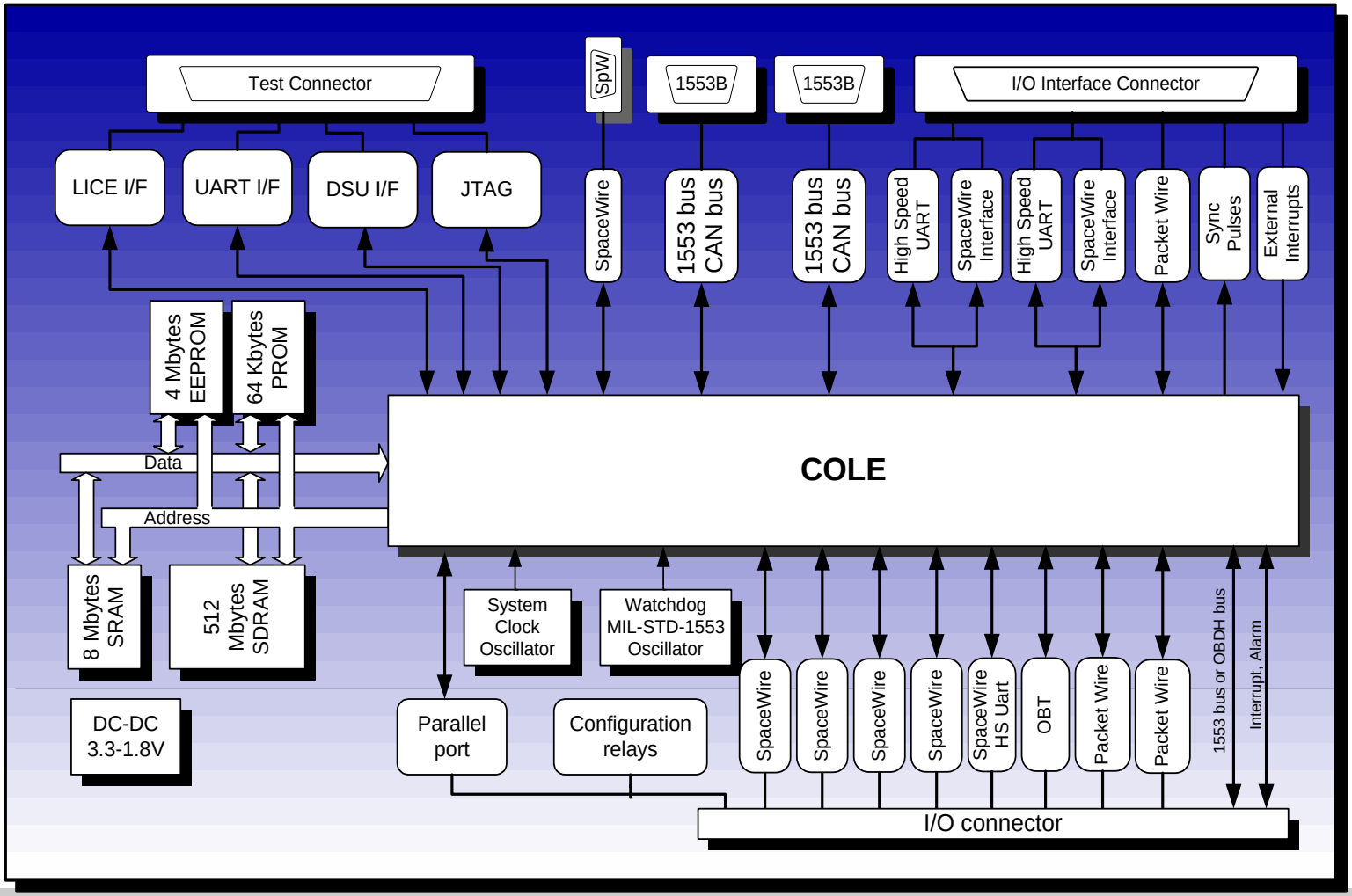
- Eight ECSS-E-50-12A SpaceWire Interfaces capable up to 200 MHz/160 Mbps, based on the UoD SpaceWire Codec IP core. Hardware support for Remote Memory Access Protocol (RMAP) compliant with ECSS-E-50-11 Draft F

- Two Controller Area Network (CAN) interfaces based on the HurriCANe IP core, supporting up to 1 Mbps

- Debug Interface UART to DSU
- Two Low Speed UART Interfaces
- Two Timers



Panther Processor Board



Panther Processor Board

- COLE ASIC, integrating LEON2-FT processor and IO interfaces
- 64 kbytes boot PROM, 4 Mbytes EEPROM
- 8 Mbytes SRAM or 512 Mbytes SDRAM
- 1553, OBDH, SpaceWire, PacketWire, CAN, UART, OBT and parallel I/O interfaces
- 6 watt power consumption
- Upward compatible with existing ERC32SC-based processor boards used in Herschel-Planck, Pléiades, Aeolus, Gaia, Galileo etc.
- Package of standard software drivers will be available
- Main supported operating systems RTEMS 4.6.2 and VXWorks 6.3
- Panther-FPGA board available now, Panther board available 2008 Q1

Panther-FPGA Board