ATF280E
A Rad-Hard reprogrammable FPGA

ESA/ESTEC 3rd Microelectronics Presentation Days 2007

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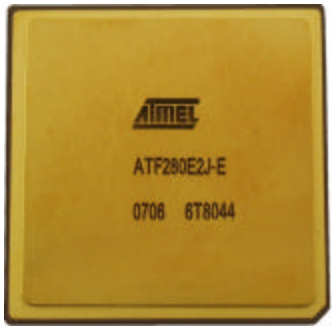
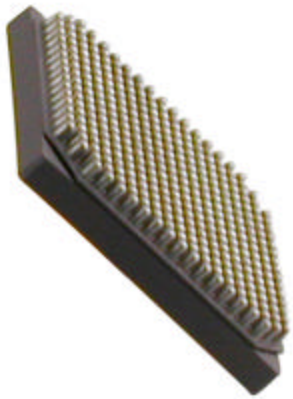
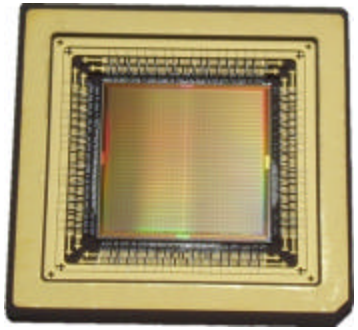






Overview

- **ATMEL rad-hard FPGA family**
- **The ATF280E FPGA**
- **ATMEL FPGA architecture overview**
- **The AT69170E serial EEPROM**
- **Securing the ATF280E configuration**
- **ATF280E hardware & software design tools**
- **Key dates**

AT40KEL040 ATMEL rad-hard FPGA

- **The first generation, the AT40KEL040, is a fully compatible rad-hard version of the commercial AT40K40AL**
- **No need for SEU mitigation while designing with it**
- **AT40KEL040**
  - **AT56KRT 0.35um technology (same as MH1RT ASIC)**
  - **All memory points are SEU hardened:**
    - **Core-cell DFF / FreeRAM**
    - **Configuration Memory & Controller**
  - **TID tested up to 300 Krad**
  - **7 E-5 error/device/day in GEO**
- **Developed under CNES contract n° 721/00/8286/00 and n° 03/1433**

AT40KEL040 Overview

- **Key features**
  - **46K gates equivalent ASIC gates**
  - **20 MHz clock speed**
  - **2304 core-cells (each 2 LUT + 1 DFF)**
  - **18 Kbit SRAM/TPRAM (144 modules of 32x4)**
  - **3.3V Core and I/Os with 5V-tolerance**
  - **MQFPF-160 (129 User I/O) / MQFPF-256 (233 User I/O) packages**
- **Experience and lessons learned:**
  - **Average 50% density (specific designs may go higher)**
  - **Average 10 MHz clock speed (specific designs may go higher)**

AT40KEL040 Design Examples

- **SODERN**
  - **CNES Megha-Tropic project**
  - **Includes a Spacewire interface**
- **KONGSBERG**
  - **ESA Gaia project**
  - **Solar array self-deployment system**

ATF280E Overview

- **ATMEL's second generation rad-hard FPGA**
  - **AT58KRHA 0.18um technology (same as ATC18RHA ASIC)**
  - **Heavy ions induced SEU Fault-Tolerance by design**
  - **SET hardening (clocks and reset)**
  - **TID up to 300 Krad**
  - **1 E-6 error/device/day in GEO**

- **Developed under CNES contract n° 04/1643/00 - 12245**

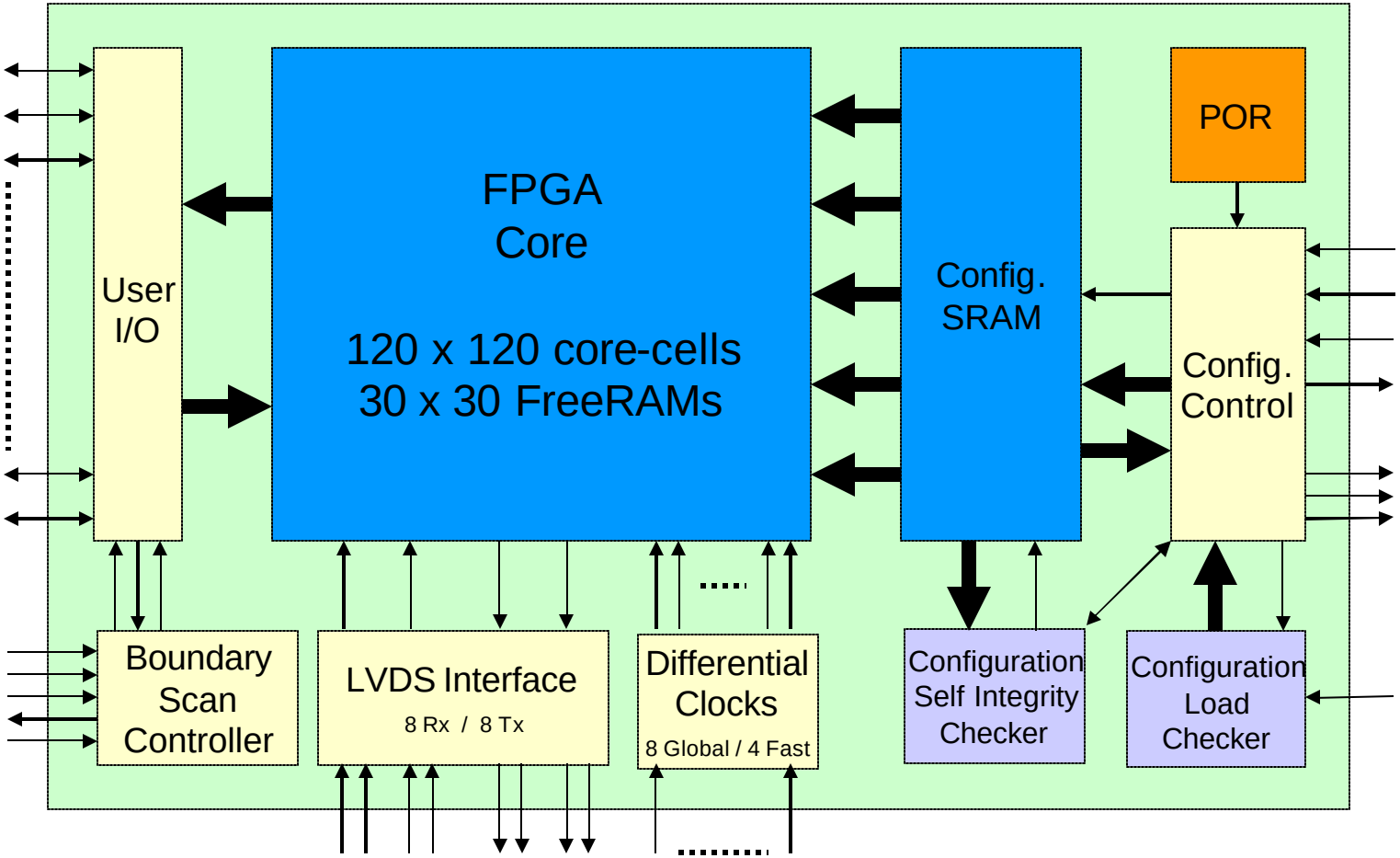
ATF280E Key Features

- 280K equivalent ASIC gates
- 50 MHz clock speed
- 14400 core-cells (each 2 LUT + 1 DFF)
- 115 Kbit SRAM/TPRAM (900 modules of 32x4 blocks)
- 1.8V Core / 1.8V and 3.3V I/Os
- LVDS: 8 Rx + 8 Tx
- Cold-sparing and 3.3V PCI-compliant I/Os

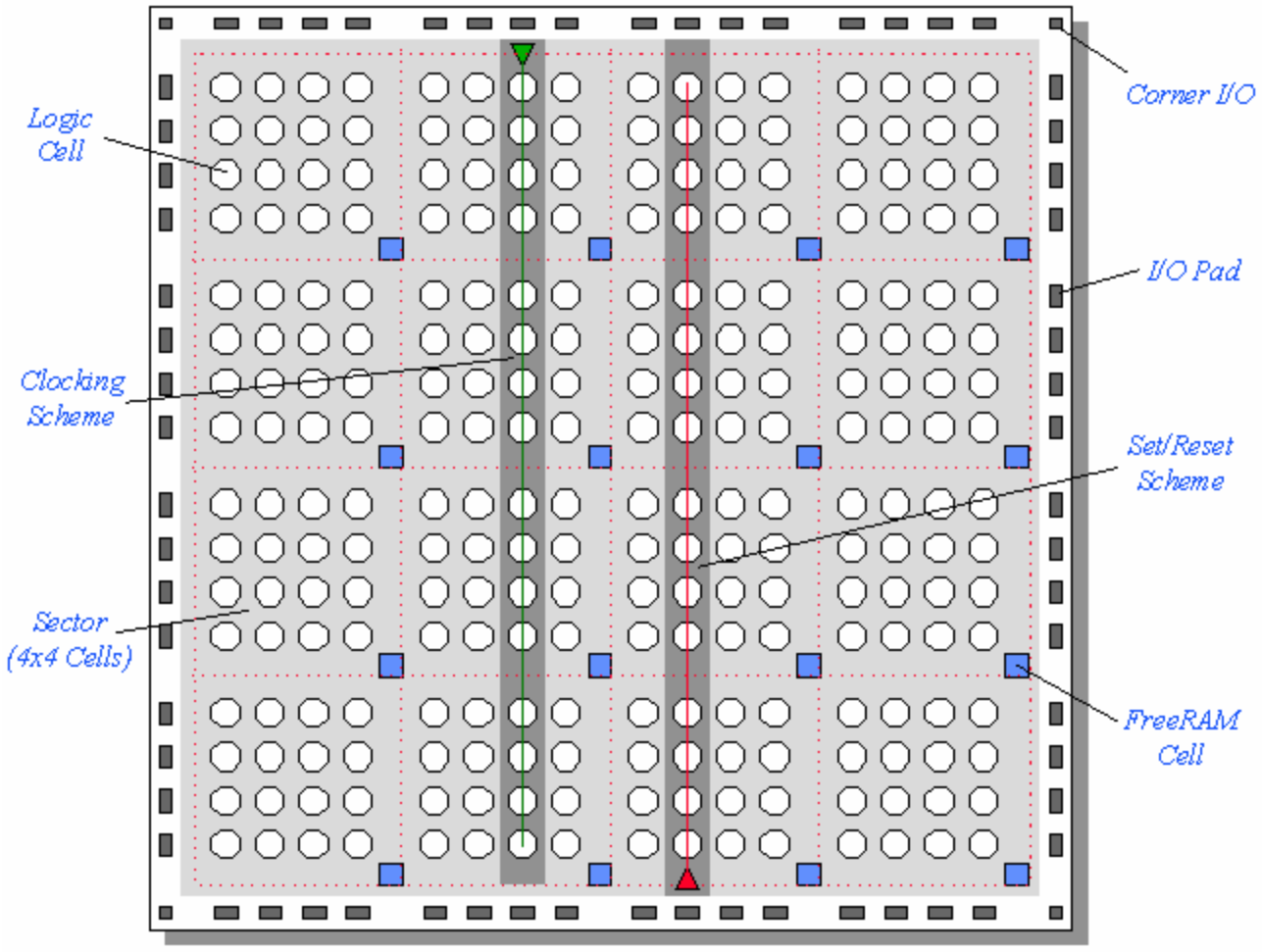
- MCGA 472 (308 User I/O) / MQFP-256 (150 User I/O) packages

- Configuration load integrity check
- Configuration self-integrity check
- Boundary scan interface

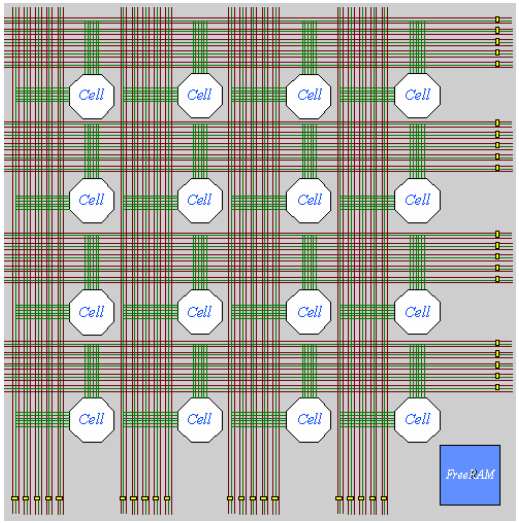
ATF280E Block-Diagram



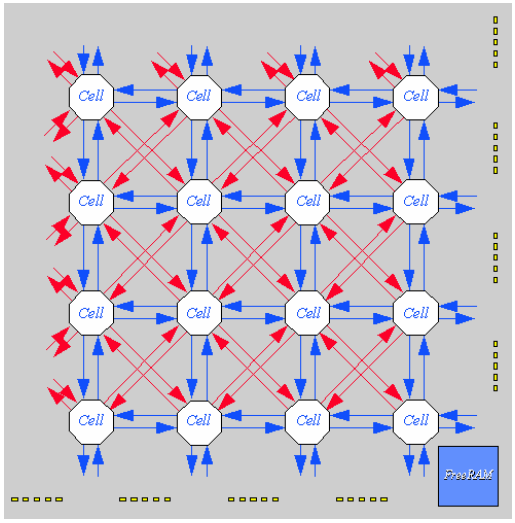
FPGA Architecture Overview



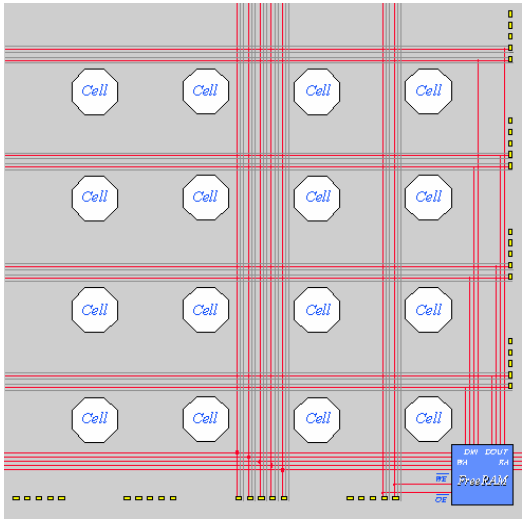
Efficient Routing Architecture



Cell to bus connection



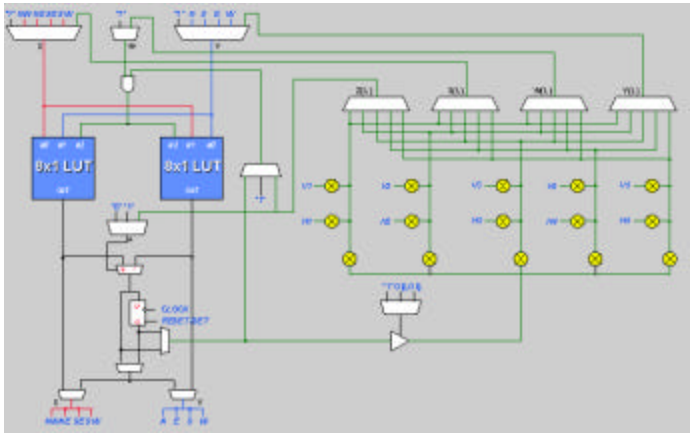
Cell to cell connection

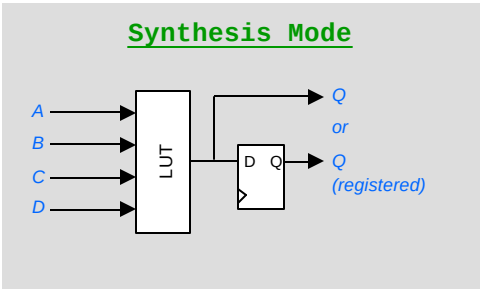


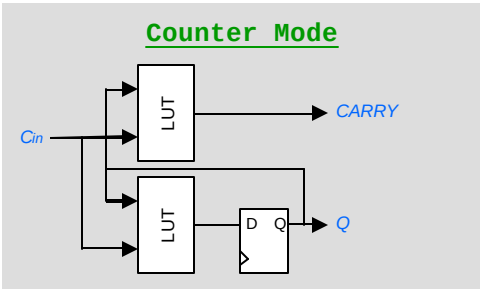
FreeRAM to bus connection

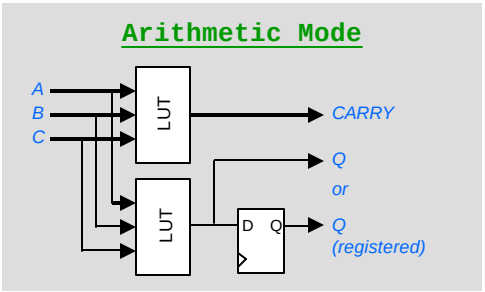
- **Efficient functions using almost only cell to cell connections**
- **FreeRAM uses very few global routing (address) and local (data) routing bus (free otherwise)**
- **Most of the routing structure is still available even if using all core-cells and FreeRAM**

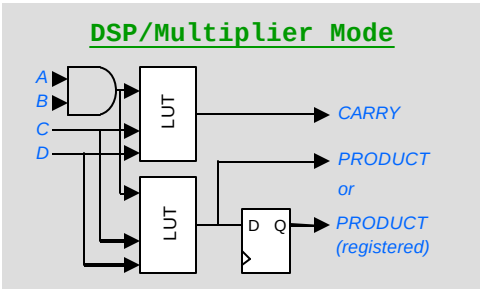
Core-Cell Modes

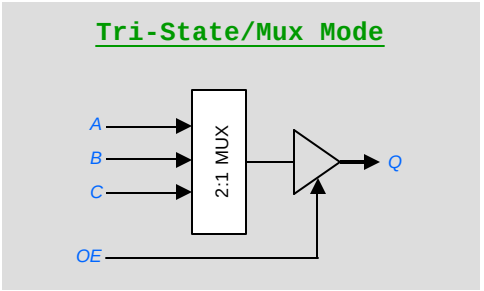






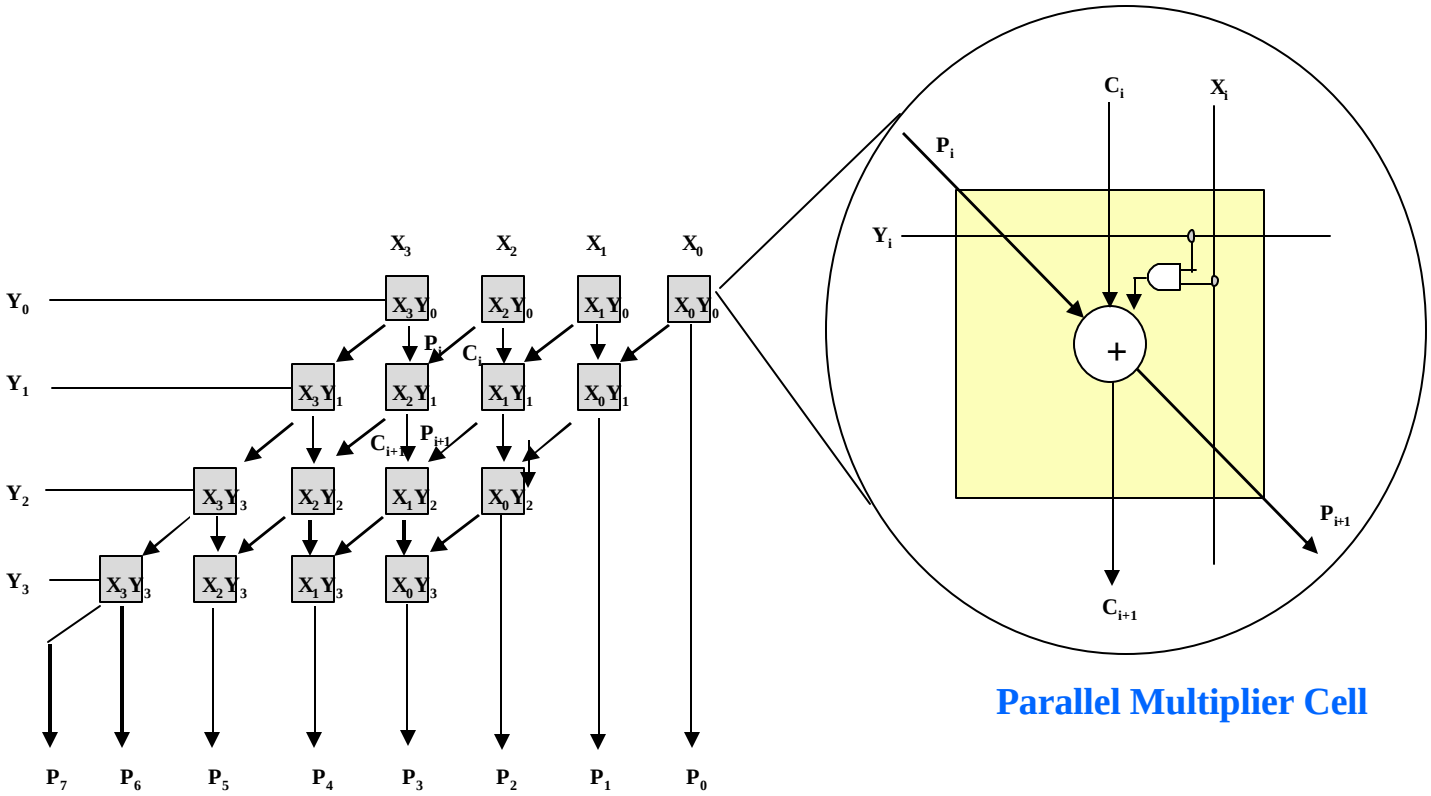






- **Efficient operators only use 1 core-cell / bit**
- **Fast multi-bit operators using cell to cell diagonal/orthogonal connections**
- **Pipelining (DFF) possible inside core-cell**

Example of Optimized Function



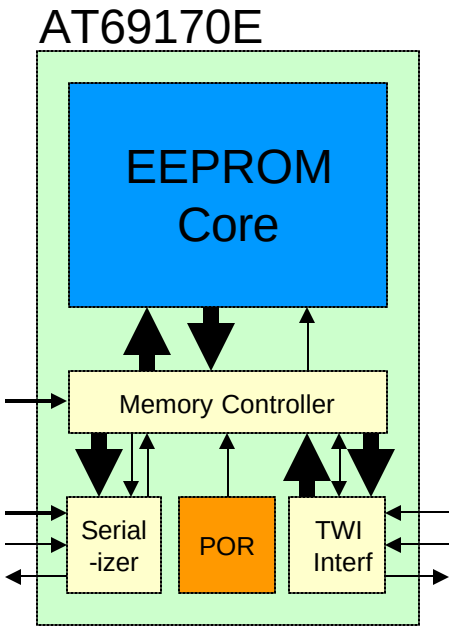
Parallel Multiplier Cell

AT69170E Overview

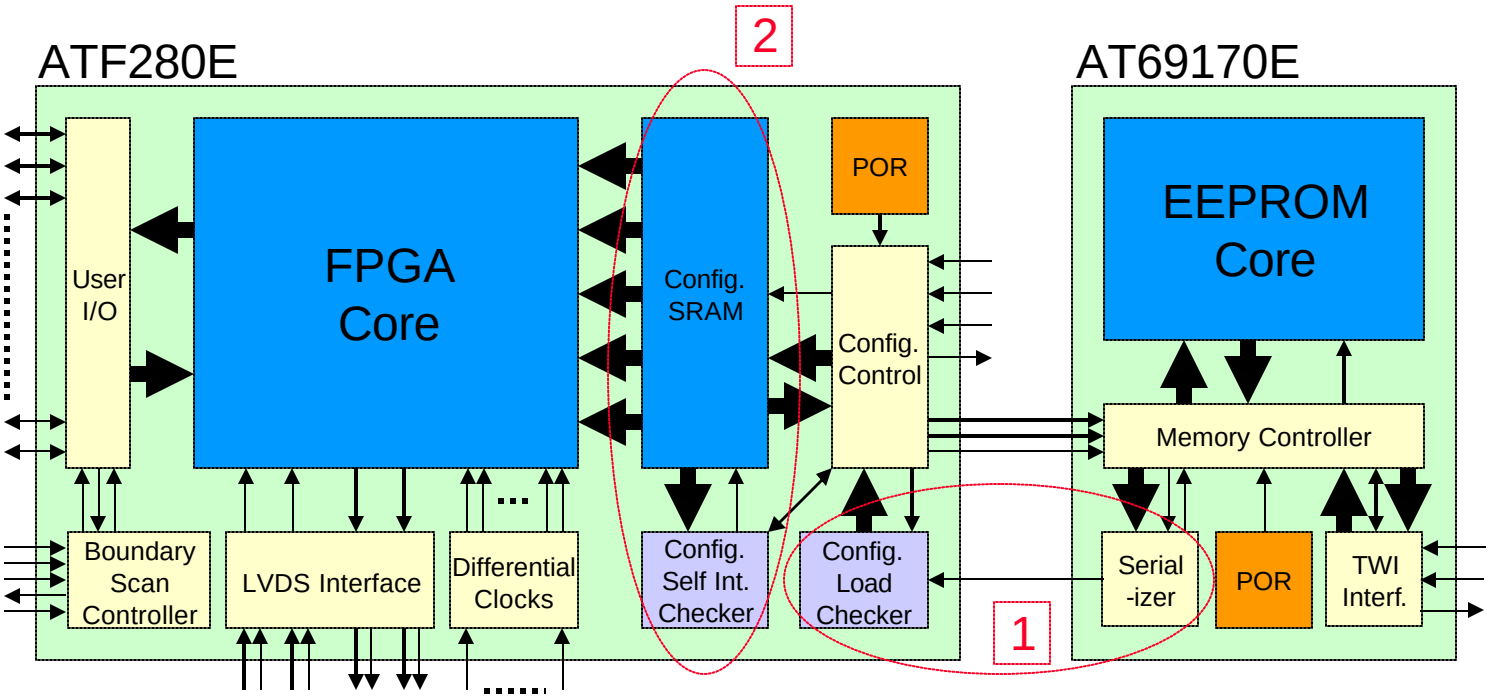
- **ATMEL's first rad-hard by design serial EEPROM**
  - **AT58K85RHA 0.18um technology**
  - **5 E-7 error/device/day target in GEO**
  - **TID expected up to 60 Krad**
- **ATF280E configuration download companion chip**
- **Developed under ESA contract n° 19083/05/NL/FM - COO1**

AT69170E Key Features

- **4 Mbit Rad Hard EEPROM**
- **512 bytes Pages**
- **FPGA serial configuration interface**
- **Standard TWI programming interface**
- **3.3V Supply Voltage**
- **FP18 Package**
- **Endurance: 10K cycles**
- **Data retention: 10 years**



Securing FPGA Configuration

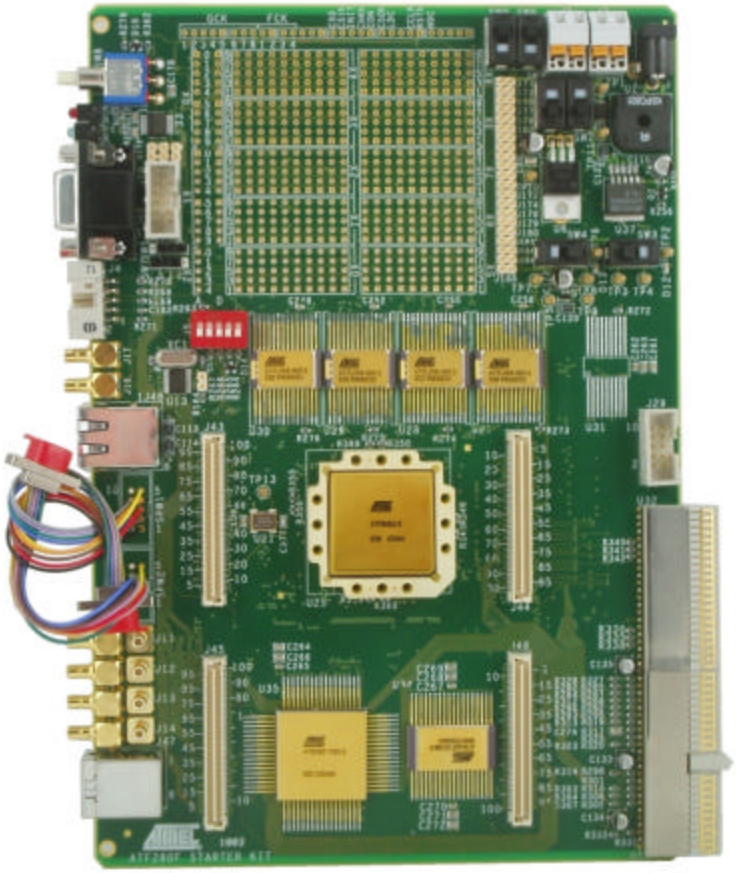


- **SRAM-based FPGAs reload their configuration on power-up**

  [1] Configuration Load checker (CRC) secures bitstream download

  [2] Configuration Self-Integrity checker secures internal configuration during operation

ATF280E Compact-PCI Evaluation Board



- **Compact PCI plug-in format:**
  - **6U format, 32 bit, 33MHz interface**
  - **Suitable for Peripheral slot**
- **On-board ATMEL devices**
  - **ATF280E (MCGA-472)**
  - **AT69170E / 4 x AT17LV010 EEPROM**
  - **AT60142 + AT68166 SRAM**
- **Front-panel connectors**
  - **2 x Mini-DB9 (LVDS: 4Tx + 4Rx)**
  - **8 x SMB (LVDS: 2Tx + 2Rx)**
  - **1 x RJ45 (LVDS: 2Tx + 2Rx)**
  - **1 x DB9 (RS232)**
- **On-board supply for standalone use**
- **On-board clock sources**
- **Probe / extension capability**

ATF280E Design Tools

- **Front-End**
  - **MENTOR Modelsim for VHDL/VERILOG simulation**
  - **MENTOR Precision Synthesis**
    - **VHDL / Verilog entry**
    - **Automatic IDS Macro detection and mapping**
- **Back-End**
  - **ATMEL Figaro IDS**
    - **Automated Place & Route**
    - **VHDL / Verilog netlist export with SDF back-annotation**
    - **Bitstream generation**
  - **ATMEL Configurator Programming Tool**
    - **ATMEL EEPROM support**
    - **Used during development and ISP in final application**

Key Dates

- **ATF280E**
  - **Design completed**
  - **Silicon in debug**
  - **Prototypes for Beta customers in end Q2 2007**
  - **Space qualification Q4 2007**
- **AT69170E**
  - **On going design**
  - **First silicon in Q3 2007**
  - **Prototypes for Beta customers Q4 2007**
  - **Space Qualification Q1 2008**