ATC18RHA MULTI-PROJECT WAFER

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CNES CONTRACTS

- **Radiation evaluation of the standard CMOS 0.18µm AT58K:**
  - **CNES contract n° 02/0709/00**
- **Rad-Hard characterization of the CMOS 0.18µm AT58KRHA:**
  - **CNES contract n° 03/1433**
- **Development of the memories cells and evaluation of ATC18RHA:**
  - **CNES contract n° 721/00/8286**
- **ATC18RHA optimization:**
  - **CNES contract n° 04/1643/00-19302**

ESA CONTRACTS

- **Development of the rad hard cell libraries ATC18RHA:**
  - **ESA contract n° 15677/01/NL/FM**
- **Space MPW:**
  - **ESA contract n° 17767/03/NL/FM**

AGENDA

- ATC18RHA SUMMARY
- SINGLE PAD RING MATRICES
- DOUBLE PAD RING MATRICES
- FORESEEN IMPROVEMENTS
- QUALIFICATION STATUS AND PLANS
- SMPW
- CURRENT BUSINESS OPPORTUNITIES
- SMPW CONTACTS
- CONCLUSIONS

SUMMARY (1)

- **Dual processes and libraries using ATC18 libraries, and 0.18µm CMOS process with a Radiation and Hirel Assurance plans**
- **Encompasses, among others, SEE hardened DFF, Cold Sparing buffers, RHBD 3.3V buffers, 400MHz+ PLL and LVDS,… characterized to mil temp range**
- **5.5Mgates capability and up to 504 signal pads for standard matrixes, and up to 7.4 Mgates for dedicated design**
- **Production design kit released since end 03/05**

SUMMARY (2)

- **Though ATC18RHA is a standard cell library, pre-defined matrices sizes and pad frames have been set so as to ease the assembly of every individual ASIC design into standard package cavity sizes and layouts**

- **For the smallest matrix, MQFPF 160 & 196 pin counts are introduced in the preferred package list**

- **For the largest matrix, introduction of 625 pins MCGA package planned during 2007**

SUMMARY (3)

Vendor	Software Package	Tool	Purpose
Cadence	Nano Encounter	AMOEBA	Place
		Nano-Route	Route
		CTS	Clock tree
		PKS	Physical synthesis
		Voltage Storm	Power scheme check
		Celtic	Cross talk analysis
Synopsys	Physical Compiler	Physical Compiler	Physical synthesis
		Primetime	STA
		Star-RC-XT	3D extraction
		Formality	Equivalence checking
Mentor		DFT-Advisor	Test insertion + ATPG

SINGLE PAD RING MATRICES (1)

One pad ring	Size (mm) S (mm²)	Programmable Pads	Buffer Power Supply Pads	Typical Nbr of Usable Gates
ATC18RHA95_220	6.19x6.19 38	220	8	1 M
ATC18RHA95_324	8.76x8.76 77	324	8	2.2 M
ATC18RHA95_404	10.66x10.66 114	404	8	3.5 M
ATC18RHA95_504	13.03x13.03 170	504	8	5.5 M

SINGLE PAD RING MATRICES (2)

- **Package matrix combinations for Single Pad Ring (SPR)**

Package Variant	Number of leads	ATC18RHA 95-220	ATC18RHA 95-324	ATC18RHA 95-404	ATC18RHA 95-504	Package Number of Signal Pins
MQFPF	T352		X	X	X	336
	256		X	X	X	240
	196	X	X			180
	160	X	X			144
MCGA	625				ESA contract X	575
	472			X	X	440
	349		X	X	X	312

DOUBLE PAD RING MATRICES (1)

- **Though the physical buffers layouts are 70µm wide, the implemented pad pitch is set to 95µm to allow for:**
  - **Matching the ceramic package bonding fingers pitch capability**
  - **Adding, next to every buffer, decoupling capacitors for better noise filtering**

- **New assembly activities are ongoing for implementing a double ring of pads in several steps resulting:**
  - **On a first place, into its availability by limiting the use of the inner ring to array power supplies pads**
  - **And later on (2008), to extend its use to almost any type of use**

DOUBLE PAD RING MATRICES (2)

Two pad rings	Size (mm) S (mm²)	Outer ring Programmable Pads	Inner ring typical number of array power pads	Buffer Power Supply Pads	Typical Nbr of Usable Gates
ATC18RHA95_220	6.19x6.19 38	220	88	8	0.725 M
ATC18RHA95_324	8.76x8.76 77	324	140	8	1.8 M
ATC18RHA95_404	10.66x10.66 114	404	180	8	2.97 M
ATC18RHA95_504	13.03x13.03 170	504	232	8	4.83 M

SINGLE PAD RING MATRICES (3)

- **Package matrix combinations for Double Pad Ring (DPR)**

Package Variant	Number of leads	ATC18RHA 95-220/88	ATC18RHA 95-324/140	ATC18RHA 95-404/180	ATC18RHA 95-504/232	Package Number of Signal Pins
MQFPF	T352		Y			336
	256	Y				240
	196					180
	160					144
MCGA	625			Y	ESA contract Y	575
	472		Y			440
	349	Y				312

FORESEEN IMPROVEMENTS

- **Add an IO25 library** **2Q07**

- **LVDS ref pads with internal routing between clusters so as to save pads and pins** **2Q07**

- **Merge/combine array and buffer grounds so as to save still more pins** **3Q07**

QUALIFICATION STATUS AND PLANS

- **Currently QML Q and V qualified**
- **Available with the SMD 5962-06B02**
- **EPPL 1 listed**
- **Available space quality grades: ESCC & QML Q/V**
- **Plan to go for E QML certification by 2H08**

SMPW (1)

- **Concept validated since 2005 with 2 customer codes**
- **Rationales: share mask and silicon costs with multiple customer designs**
- **Implementation: when it is an ESA ASIC design, the customer doesn't pays for it**
- **Foreseen launch rate: every 6 months, depending on designs availability**

SMPW (2)

- **Major steps:**
  - **RTE**
  - **ELAP**
  - **Detailed feasibility study**
  - **PO**
  - **Preliminary LR (optional)**
  - **LR**
  - **LRCD** — **T0-4 MONTHS**
  - **Preliminary DR (optional)**
  - **DR**
  - **DRCD** — **T0-2 WEEKS**
  - **Tape out** — **T0**
  - **Prototyping** — **T0+16 WEEKS**
  - **FM**

SMPW (3)

- **Planned launch time scales**

Runs	LRCD	DRCD	Prototypes	FM
E1	March 07	July 07	Nov 07	June 08
E2	Sept 07	January 08	May 08	Dec 08
E3	March 08	July 08	Nov 08	June 09
E4	Sept 08	January 09	May 09	Dec 09

SMPW (4)

- **Candidates:**
  - **COLE and SpW RTC with SAAB**
  - **SCOC3, FFTC and MDPA with Astrium**
  - **And 5 other firm candidates which cannot be disclosed**
- **Foreseen first run launch: 3Q07**

SMPW information

- **Atmel hotline for SMPW:** smpw-atc18@nto.atmel.com
- **Direct link**
  http://www.atmel.com/dyn/resources/prod_documents/ATC18RHA_SMPW.PDF
- **Contact point**
  - **Jean Bouillon**

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CONCLUSIONS

- **ATC18RHA manufacturability demonstrated with 2 TVs and alpha customer design**
- **SMPW manufacturability demonstrated with 2 customer designs and 2 TVs**
- **Still waiting the launch of the first formal SMPW run**
- **Meanwhile, optimization and improvements are on going**
- **Already MIL QML Q/V**
- **ESCC QML this year**