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High-performance low power front-end for multi-band satellite navigation systems

ESTEC Contract nr 13982/99/NL/FB

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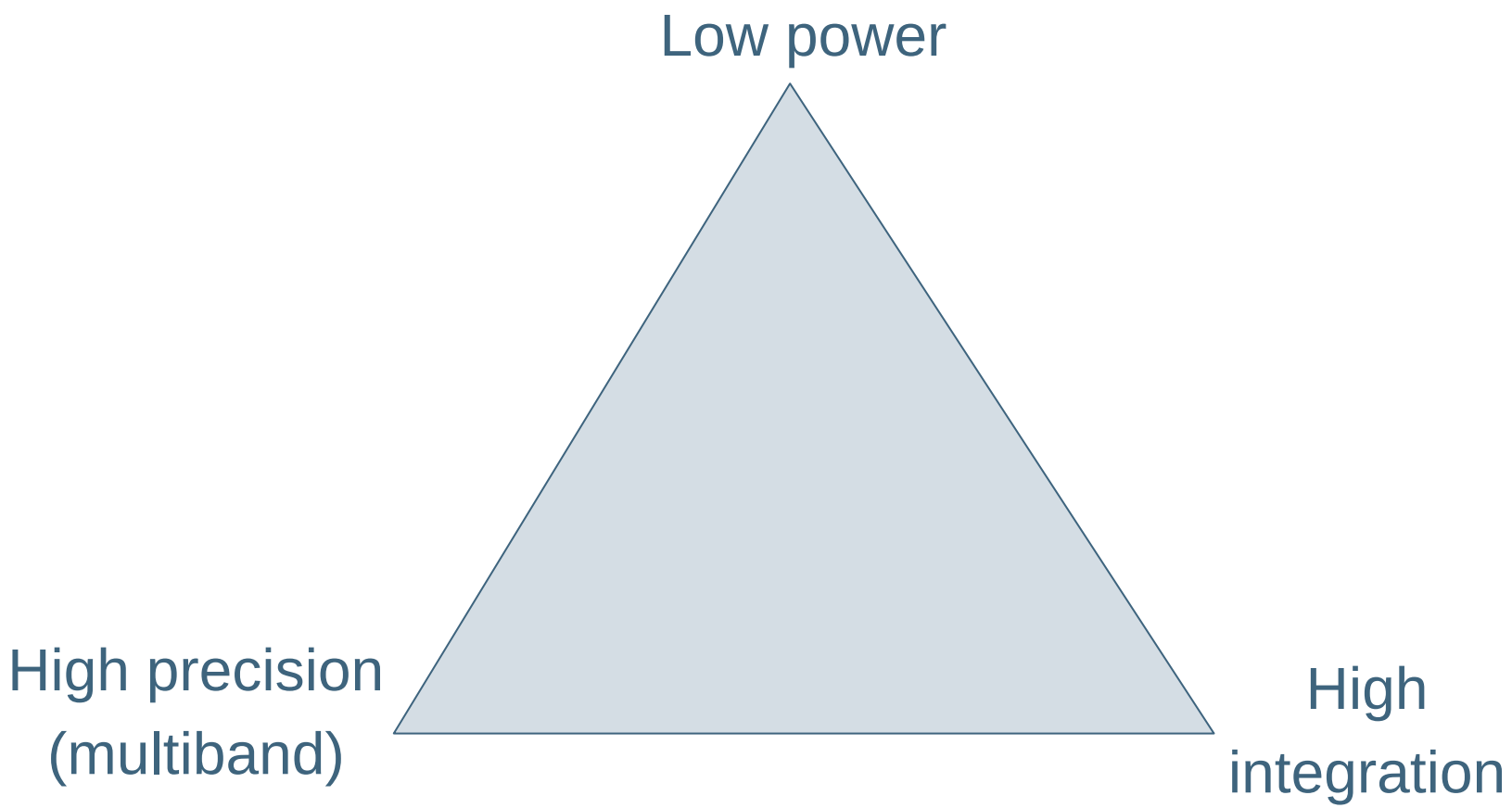
on behalf of IMECs GPS/GLONASS team

Satellite systems face contradictory targets

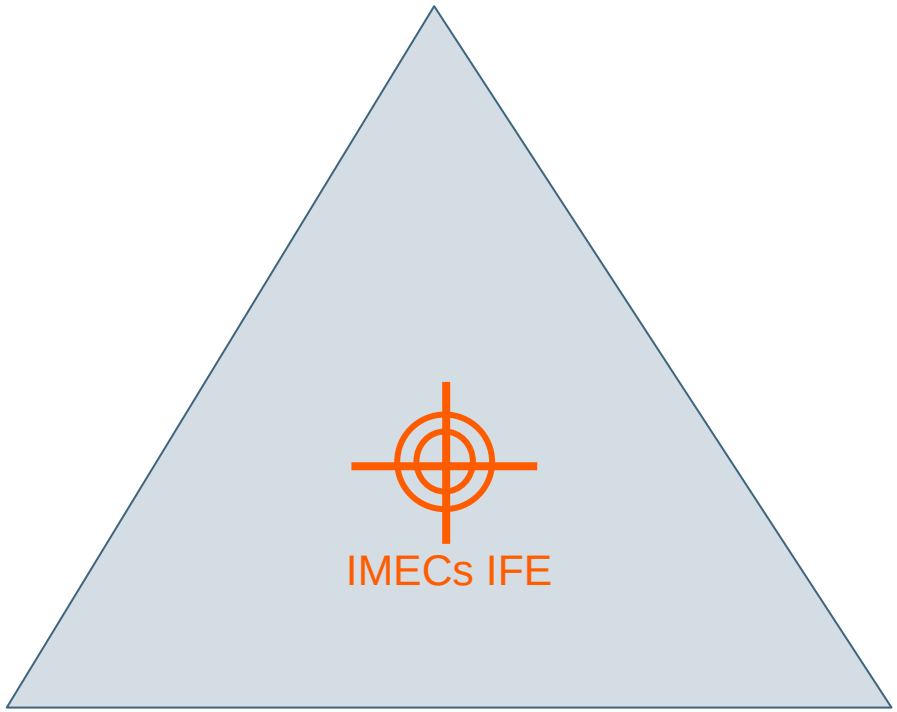


Satellite systems face contradictory targets

55 mW per channel

RF: 22 mW
Dig: 25 mW

Low power



High precision (multiband)

5 channels + low noise
Cascaded NF RF module: 2.2 dB

High integration

System-in-a-package without external filters

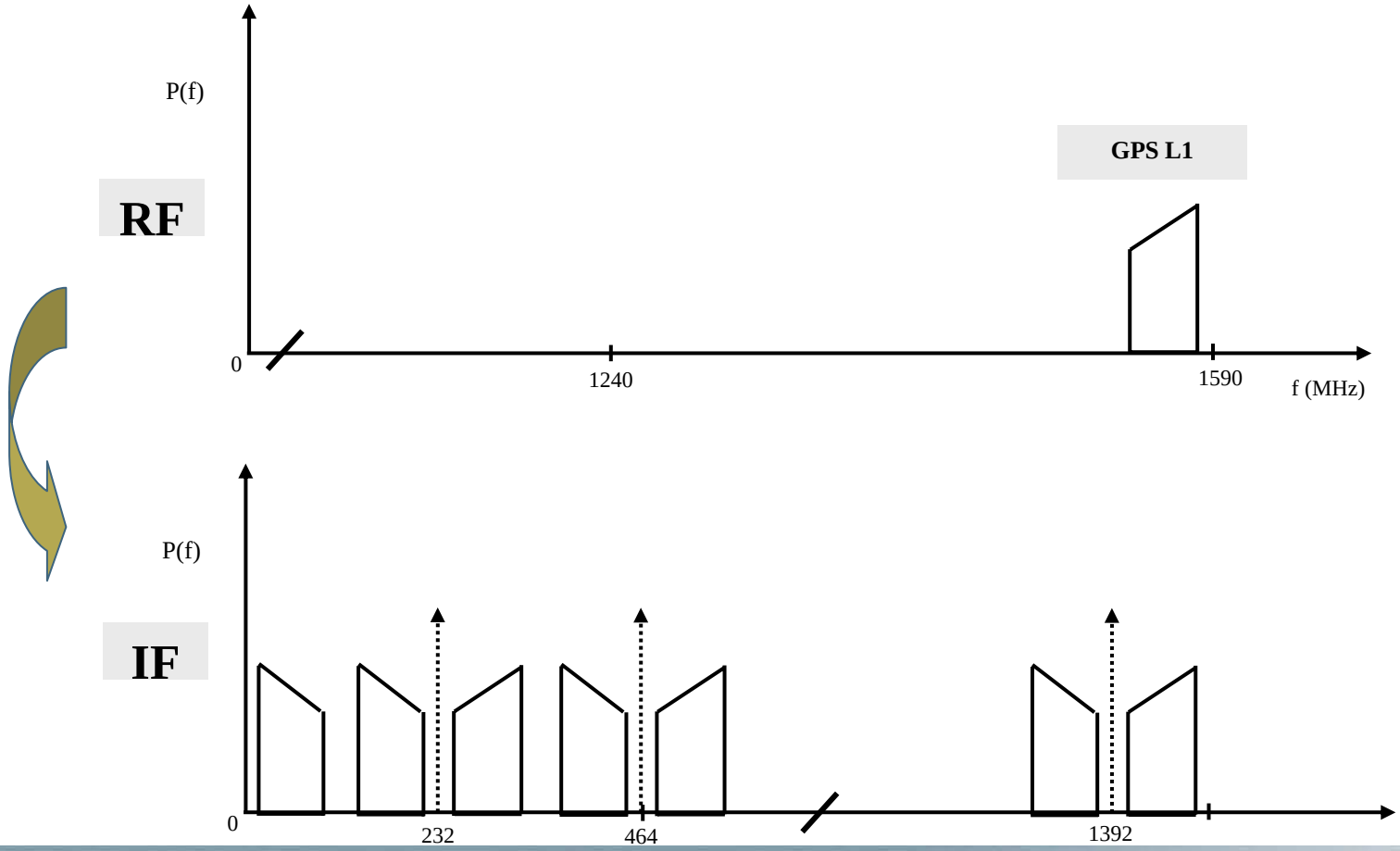
High-performance low power front-end for multi-band satellite navigation systems

- Coverage of 5 channels
- Integrated Front-End (IFE)
- System integration
- Project status
- Lessons learned

Front-End uses subsampling @ 232 MHz

RF satellite signals sampled at 232 MHz

$\Rightarrow$ aliasing occurs and RF signal is converted to IF

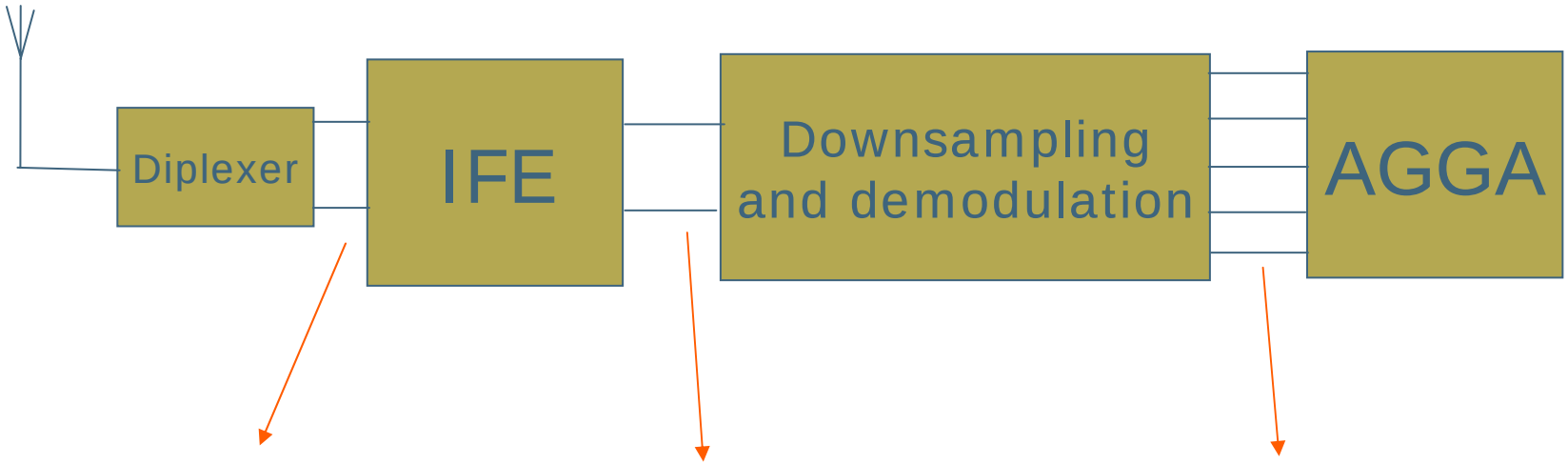


Multi-band reception without inter-band interference

Channel	RF Frequency (MHz)		Sample Frequency (MHz)	Digital IF Frequency (MHz)		
	Low	High		Low	High	
GPS L5	1164.4	1188.5	232	4.5	28.5	Lower band
GPS L2	1217.37	1237.83	232	57.37	77.83	
GLONASS L2	1241.33	1256.36	232	77.83	96.36	
GPS L1	1565.19	1585.65	232	38.35	58.81	Upper band
GLONASS L1	1592.9525	1613.86	232	10.14	31.05	

- Oversampling will provide a possibility to have extra accuracy.
- Subsampling requires good pre-filtering of the signal.

Integrated FE within complete chain

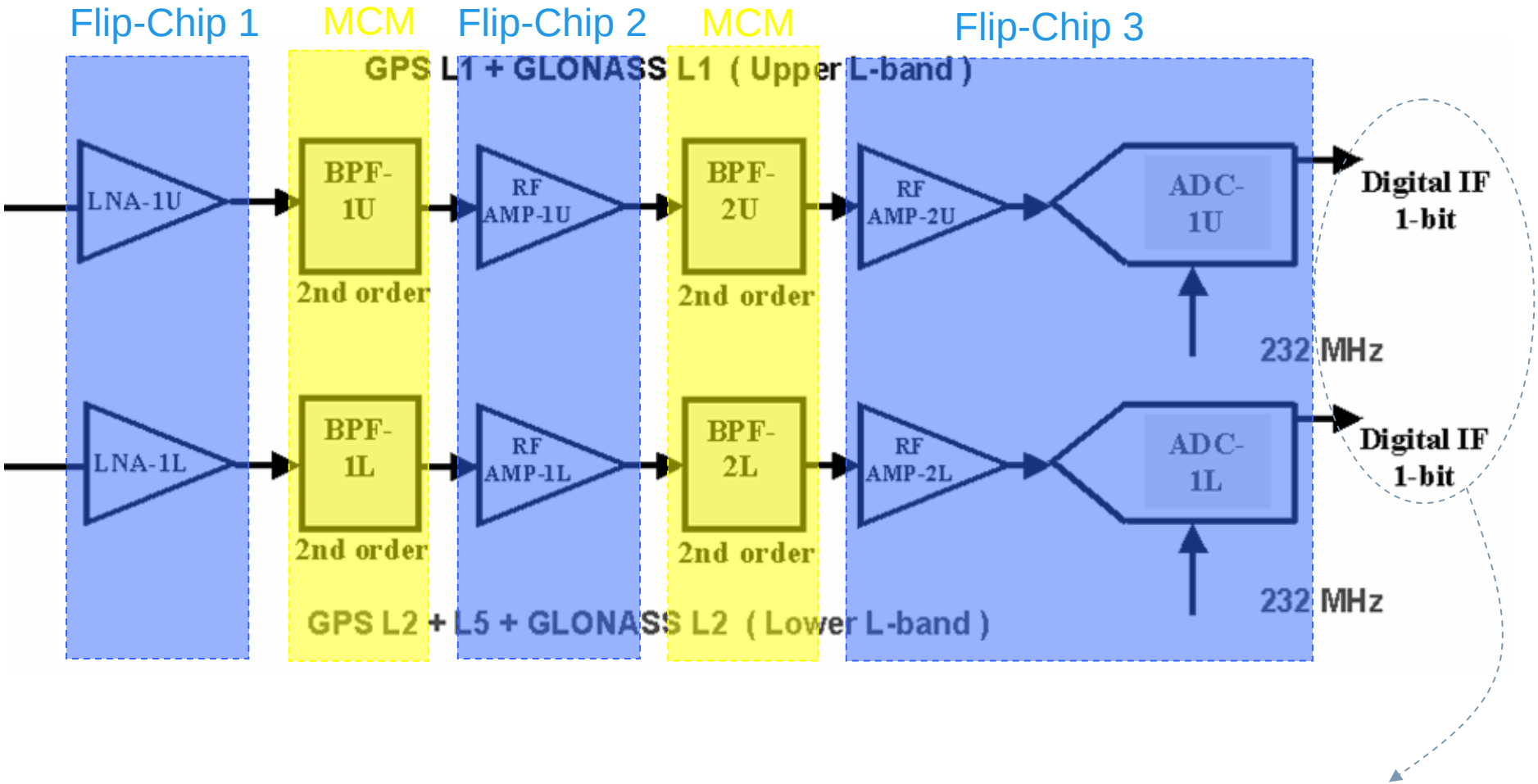


RF signals for upper and lower band

1-bit quantized signal at 232 MHz (upper/lower band)

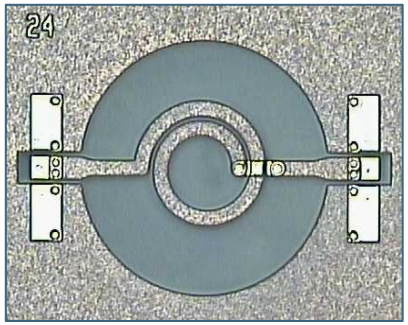
2-bit IQ signal for GPS L1, L2 and L5 GLO L1 and L2

Separate RF branch for upper and lower band

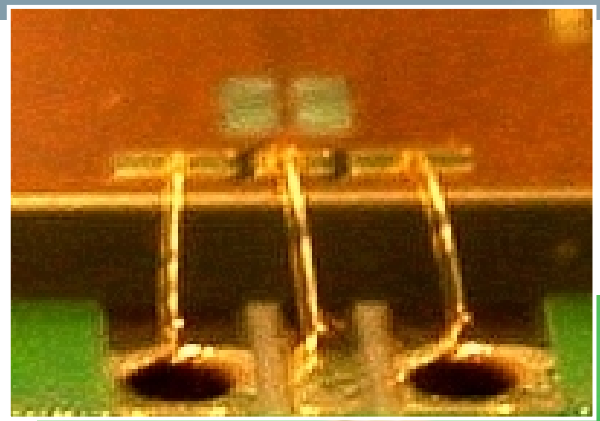


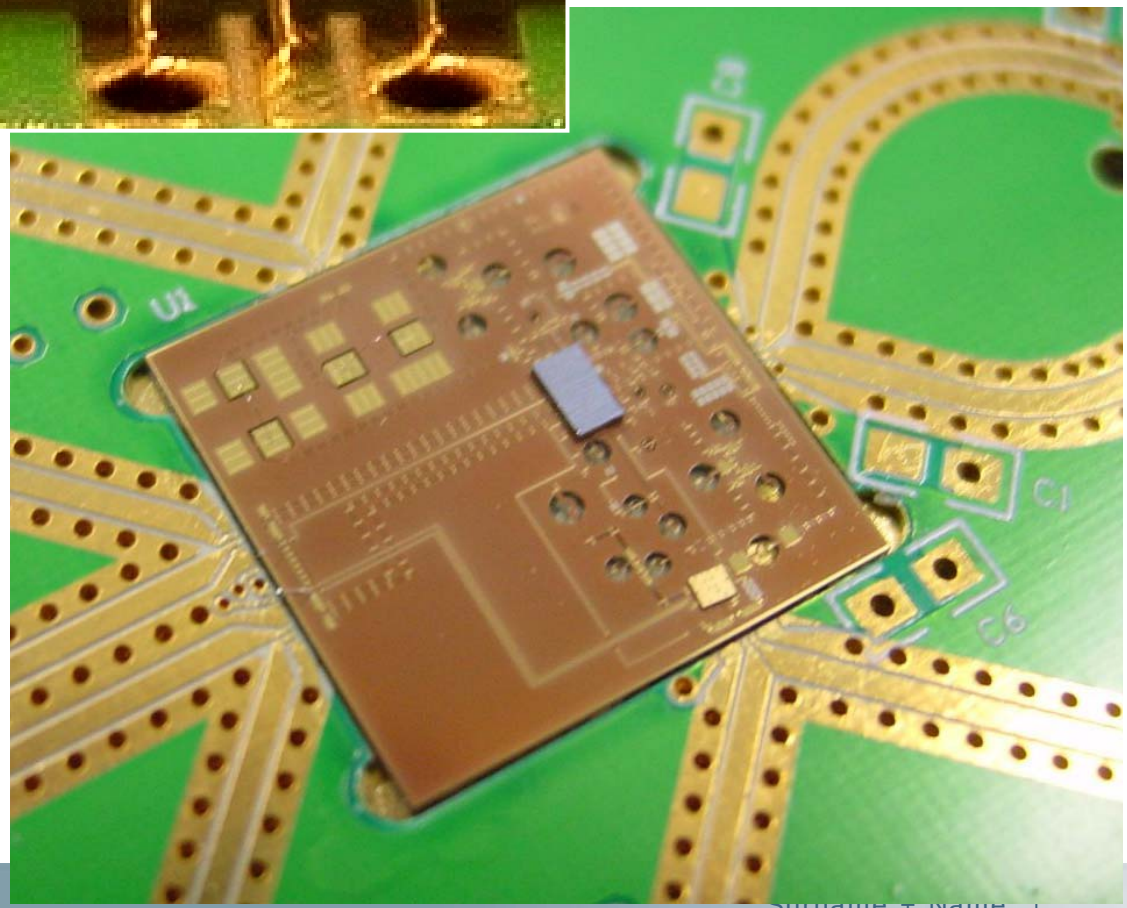
Outputs LVDS compliant

High integration possible due to IMECs MCM-D technology



Inductor Q up to 100



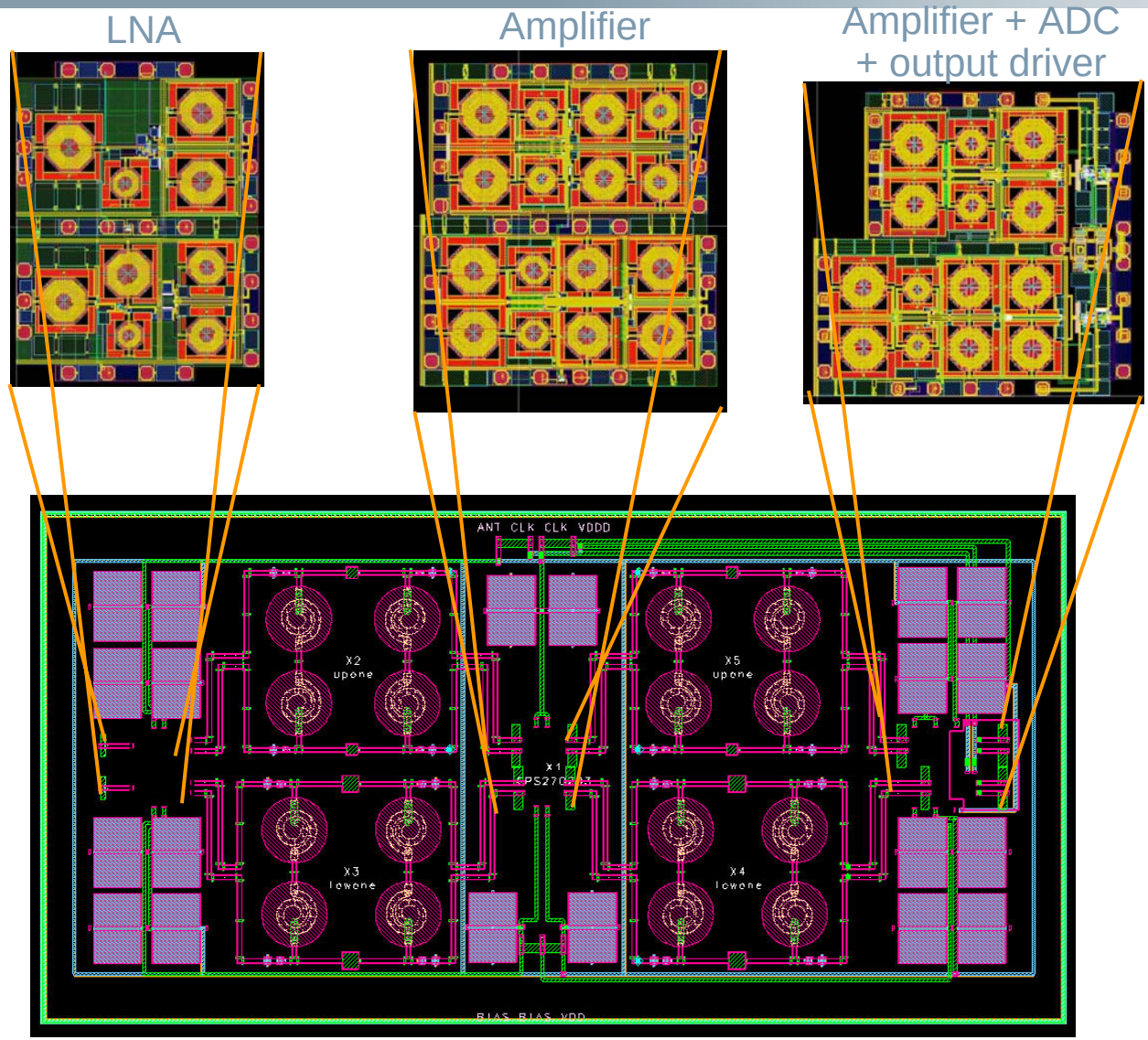


RF MCM-D technology

- glass substrate
- flip-chip mounting
- high-quality embedded passives

Amplifiers with 1-bit ADC onto MCM

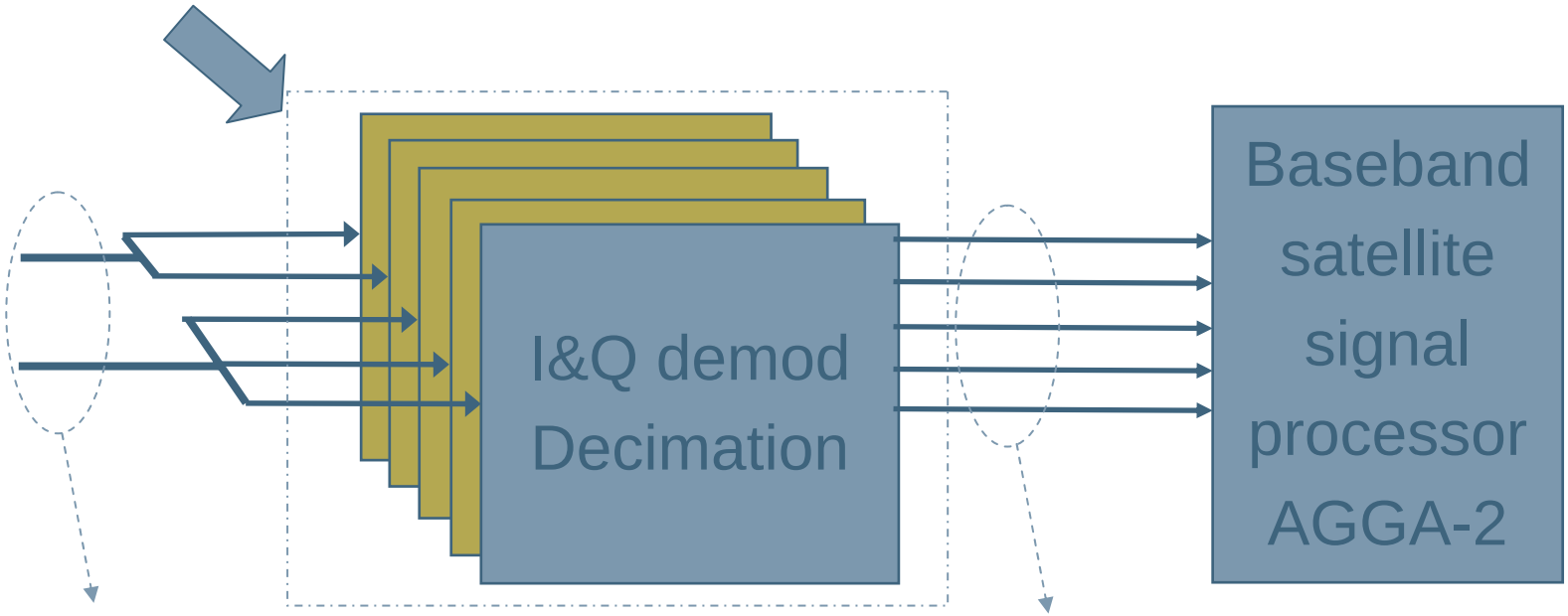
22 x 11 mm



BiCMOS 0.35 um

IMEC builds on previous baseband satellite signal processor

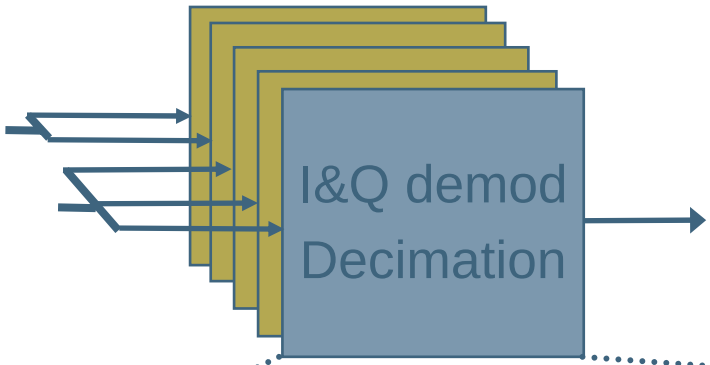
Existing baseband processor will be used, focus on signal treatment



1-bit @ 232 MHz
Upper/lower band

2-bit I&Q @ 29 MHz
For each satellite subband

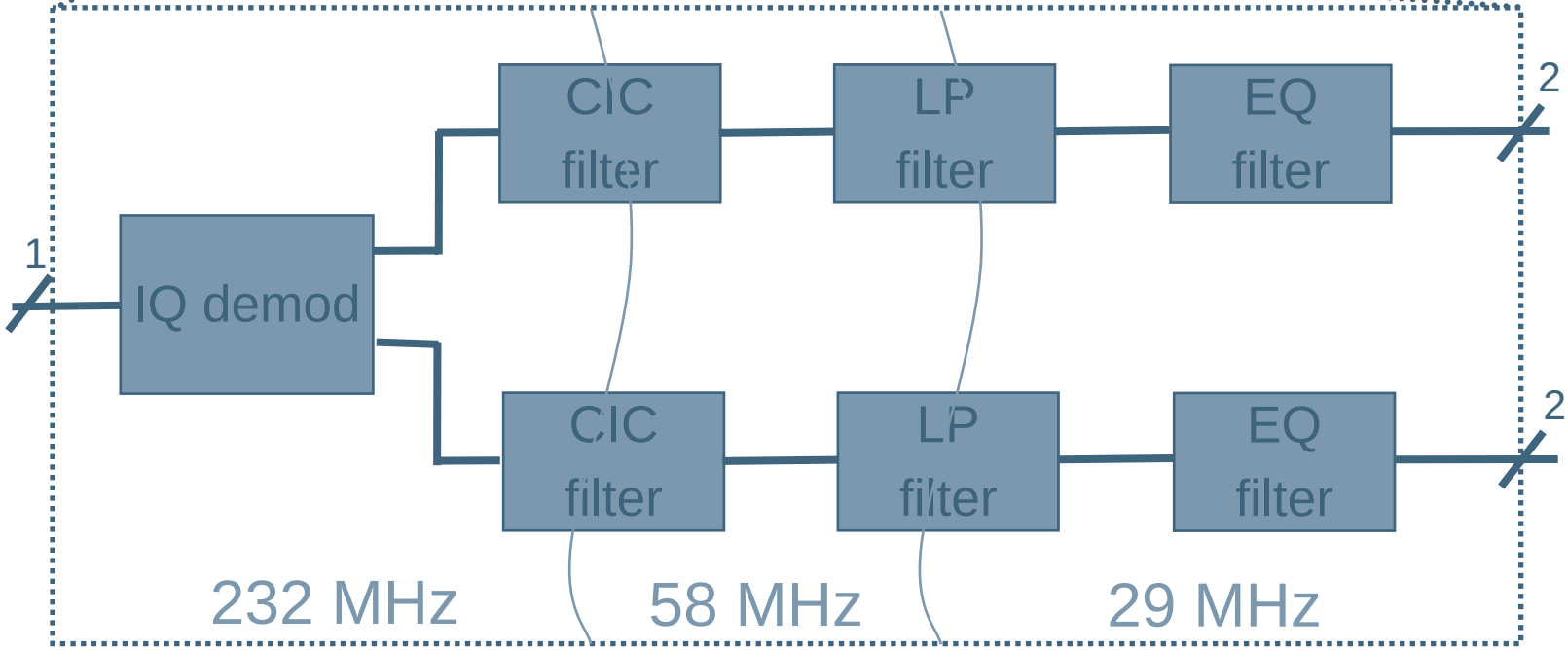
Multistage decimation reduces the power



Multistage decimation

⇒ reduced filter complexity & operating frequency

⇒ reduced power dissipation



Project status

- Original project timing was extended to end 2006.
- Active components designed and measured
  (redesign no longer possible -> processing terminated)
  - Chip 1 (LNA): on spec
  - Chip 2 (AMP1): on spec
  - Chip 3 (AMP2+ADC): only one working device
- Final MCM designed and measured:
  - High and low band filters within 50MHz of their target specification
  - Termination and grounding improved in the final design
  - Nevertheless, bonding problems on the final MCM carriers
- IQ demodulation and decimation implemented on custom developed FPGA board

Lessons learned

- Integration of AMP2 and ADC converter into single chip makes debugging and characterization difficult.
- The layout of the bond pad on-chip should be optimized to increase the flip-chip yield.
- Fewer bumps per chip increase the flip-chip yield. The 6-chip solution might thus be worth reconsidering.
  (solution put aside due to the large total amount of required bumps)
- For the MCM filters, the trade off between the center frequency sensitivity and the common mode rejection should be studied.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