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# *LEONUMC – The LEON-2 Fault-Tolerant Processor in 0.18 $\mu\text{m}$ Commercial UMC Technology*

Microelectronics Presentation Days  
ESTEC, 4 – 5 February 2004

*Roland Weigand*  
*European Space Agency*  
*Data Systems Division TOS-EDM*  
*Microelectronics Section*  
*Tel. +31-71-565-3298*  
*Fax. +31-71-565-6791*  
*Roland.Weigand@esa.int*

*Steven Redant*  
*IMEC*  
*Leuven, Belgium*  
*Tel. +32-16-281928*  
*Fax. +32-16-281584*  
*redant@imec.be*



Microelectronics Section



LEONUMC  
MPD 2004

## ◆ **Introduction and Objectives**

- ▲ Objectives
- ▲ Project Timeline
- ▲ Design Presentation

## ◆ **SEU Fault-Tolerance (FT) by Design**

- ▲ EDACs and parity protection of memories
- ▲ TMR Implementation in VHDL and netlist
- ▲ Clock and reset triplication and clock edge spreading

## ◆ **Impacts of FT to the Design Flow**

- ▲ Simulation and Synthesis of a design with TMR inserted partially in VHDL or at netlist
- ▲ Initialisation of gate level simulations
- ▲ Timing issues due to the clock edge spreading
- ▲ Scan insertion and scan testing of a multiple clock and clock-edges design

## ◆ **Packaging issues**

- ▲ Bonding of a very small die

## ◆ **Conclusion**

# Objectives

- ◆ **Prove the efficiency of the SEU protection in LEON2**
  - ▲ LEON1 Demonstrator in 0.35  $\mu\text{m}$  Atmel technology ( $\leq$  May 2001)
  - ▲ Now added clock edge spreading and mapped to 0.18  $\mu\text{m}$  UMC technology
- ◆ **Measure radiation behaviour of commercial library**
  - ▲ Comparison to the Rad-Hard-By-Design (RHBD) library (same technology)
  - ▲ Total dose and latchup behaviour to be analysed
- ◆ **Provide early prototypes of the AT697 chip**
  - ▲ Almost compatible (LEON2-1.0.4 + InSilicon PCI interface)
  - ▲ 100 MHz clock frequency - significant performance gain compared to FPGA
  - ▲ Development board has been designed and is available
- ◆ **Lessons learned – an important outcome of the project**
  - ▲ Experience with LEON and PCI interface in general
  - ▲ Lessons for FT implementation
  - ▲ Interfacing to the ASIC/MPW flow of IMEC/Europractice
  - ▲ Important know-how transfer to other projects

# Project Schedule (1)

- ◆ **Q1/2002: Initiation, design definition and VHDL design**
  - ▲ Green light (budget) for activity given 6. March, proposal from IMEC
- ◆ **Q2/2002: Detailed Design, contract placement (13. June)**
  - ▲ Selection and generation of Macrocells (PLL's, memories)
  - ▲ First netlist end of May, final pre-layout netlist and floorplan 9. August – in several iterations, numerous issues had to be solved:
    - » Netlist compatibility issues (Verilog naming rules in Synplify ASIC)
    - » Change of source code (insertion of test pins, bugfixes of LEON 22. July)
    - » Preparation of scan insertion interactively between IMEC and ESTEC
- ◆ **Q3/2002: Gate level simulation, layout, scan insertion and –pattern generation**
  - ▲ Severe initialisation problems at gate level simulation → forcing flip-flops necessary
  - ▲ Final pre-layout netlist with scan path ready 19. August
  - ▲ Place & route, clock tree synthesis, layout checks, several iterations performed by IMEC
  - ▲ Hold time fix and two reoptimisations facing Synopsys bugs
  - ▲ Final layout 19 September, tapeout released 9 October
  - ▲ Difficult package selection (small chip, high I/O count, suitable for radiation tests)
  - ▲ Scan pattern generation completed 18. October (after tapeout)

# Project Schedule (2)

- ◆ **Q4/2002: Manufacturing and test preparation**
  - ▲ Test specification established together with IMEC
  - ▲ Test board preparation by IMEC and Microtest (Italy)
  - ▲ Functional test pattern generation and conversion
  - ▲ Samples delivered beginning of December, yet ongoing package discussions
- ◆ **Q1/2003: Bonding and Packaging**
  - ▲ Problems bonding small die in large cavity: “demetallisation”
  - ▲ HCM (France) failed bonding, switch to AMIS (Pocatello, USA)
- ◆ **Q2/2003: Testing – Q3/2003: Final Report and close of project**
  - ▲ Testing at Microtest (Lucca, Italy)
  - ▲ Scan test abandoned – identified hold problems in scan path
  - ▲ Functional tests affected by flip-flop forcing in gate simulation
  - ▲ Pattern mismatch due to (slow) pull-up’s in the test board
  - ▲ A yield of 80% (40/50) was obtained on functional pattern @ 10 MHz
  - ▲ Additional clock speed characterisation confirms the 100 MHz target

# The LEONUMC Design

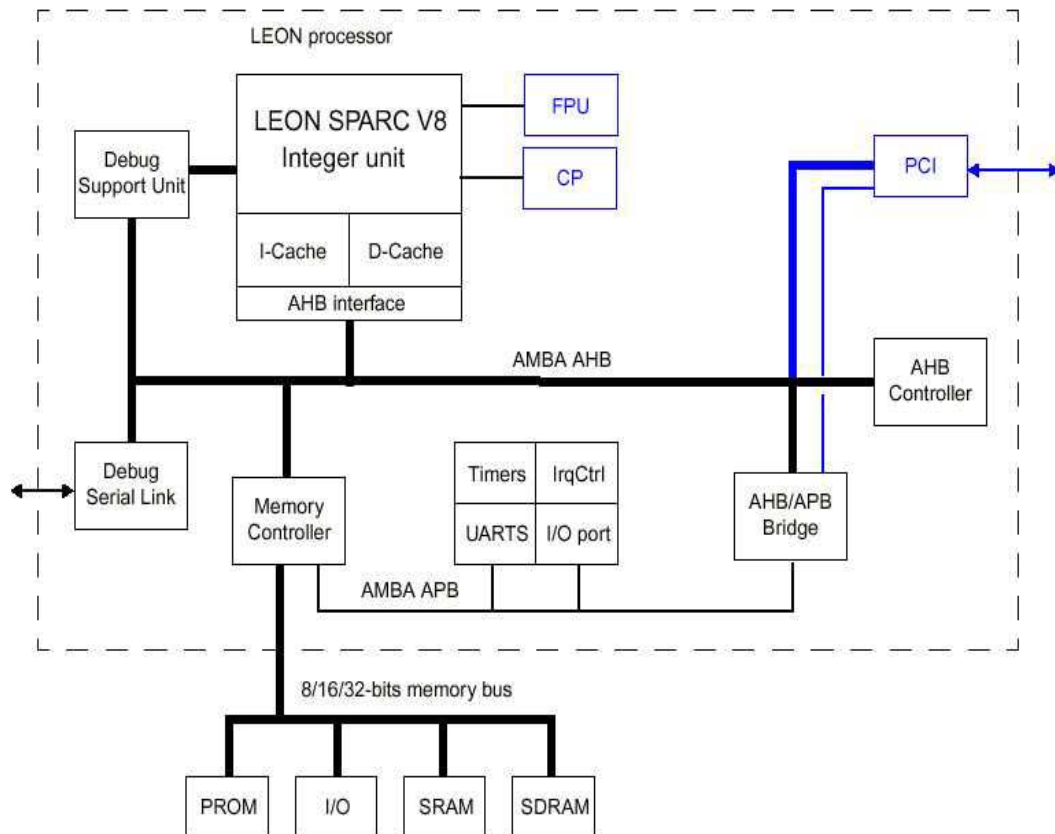


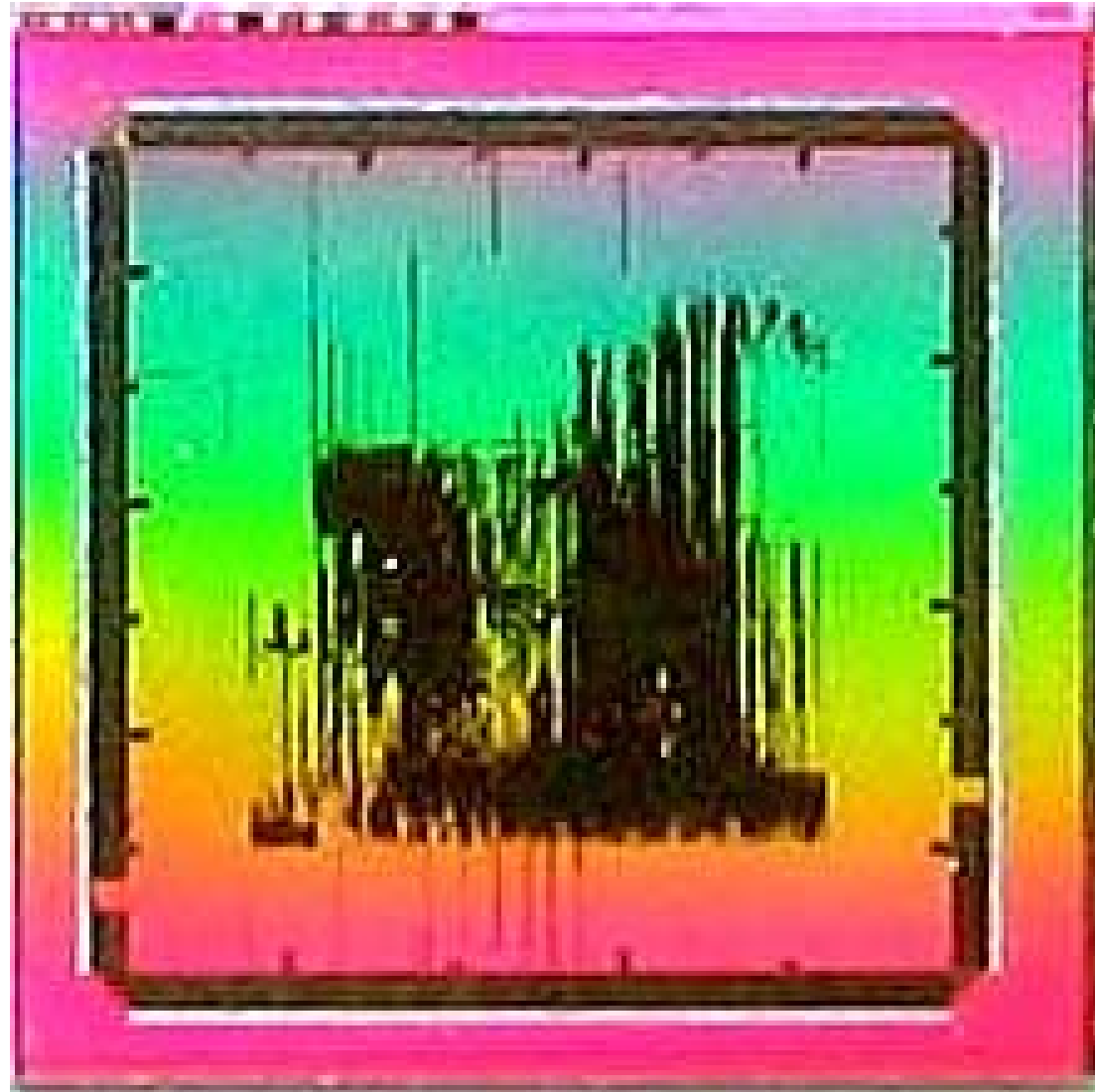
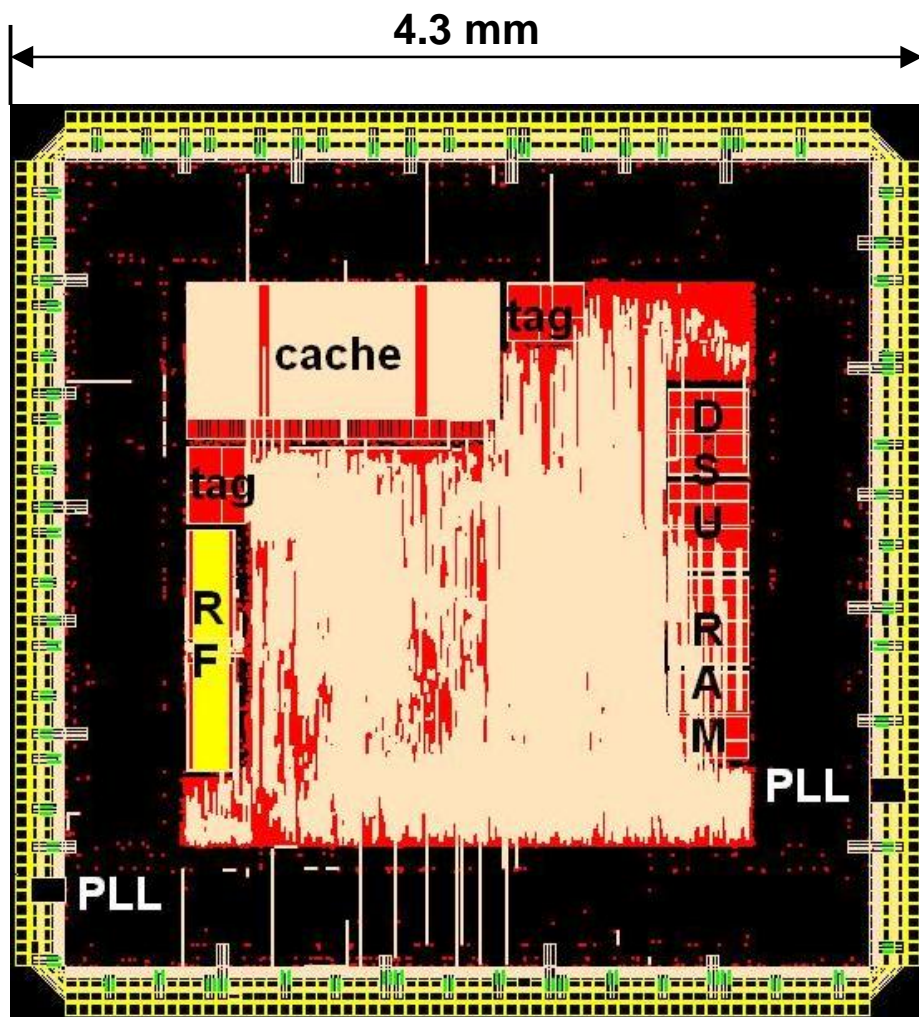
Figure 1: LEON2 block diagram

## ◆ Chip Design Data

- ▲ LEON2FT-1.0.4 with Meiko FPU
- ▲ InSilicon PCI core with ESA wrapper
- ▲ UMC 0.18  $\mu\text{m}$  libraries from Virtual Silicon (VST): core, pad, memory, PLL
- ▲ 14 Memories: 4 cache/tags, 2 two-port register files, 8 DSU memories 128x32
- ▲ 2 PLL: 33/33 MHz PCI, 25/100 LEON
- ▲ 256 Pads (including 68 power pads)
- ▲ 2x3 (TMR with edge spreading) clock domains (33 MHz PCI, 100 MHz LEON)
- ▲ On-chip memory:  $2.18 \text{ mm}^2 = 200 \text{ kbit}$
- ▲ Standard cells:  $3.55 \text{ mm}^2 = 290 \text{ kGates}$   
 $= 170 \text{ kG flip-flops} + 120 \text{ combinatorial} = 100 \text{ kG for PCI} + 190 \text{ kG for LEON}$
- ▲ Core area:  $2.68 \times 2.68 \text{ mm} = 7.18 \text{ mm}^2$
- ▲ Chip size:  $4.3 \times 4.3 \text{ mm} = 18.5 \text{ mm}^2$
  
- ▲ **High share of flip-flops (PCI FIFOs!)**
- ▲ **The chip is pad-limited!**



# Layout and Chip Photo

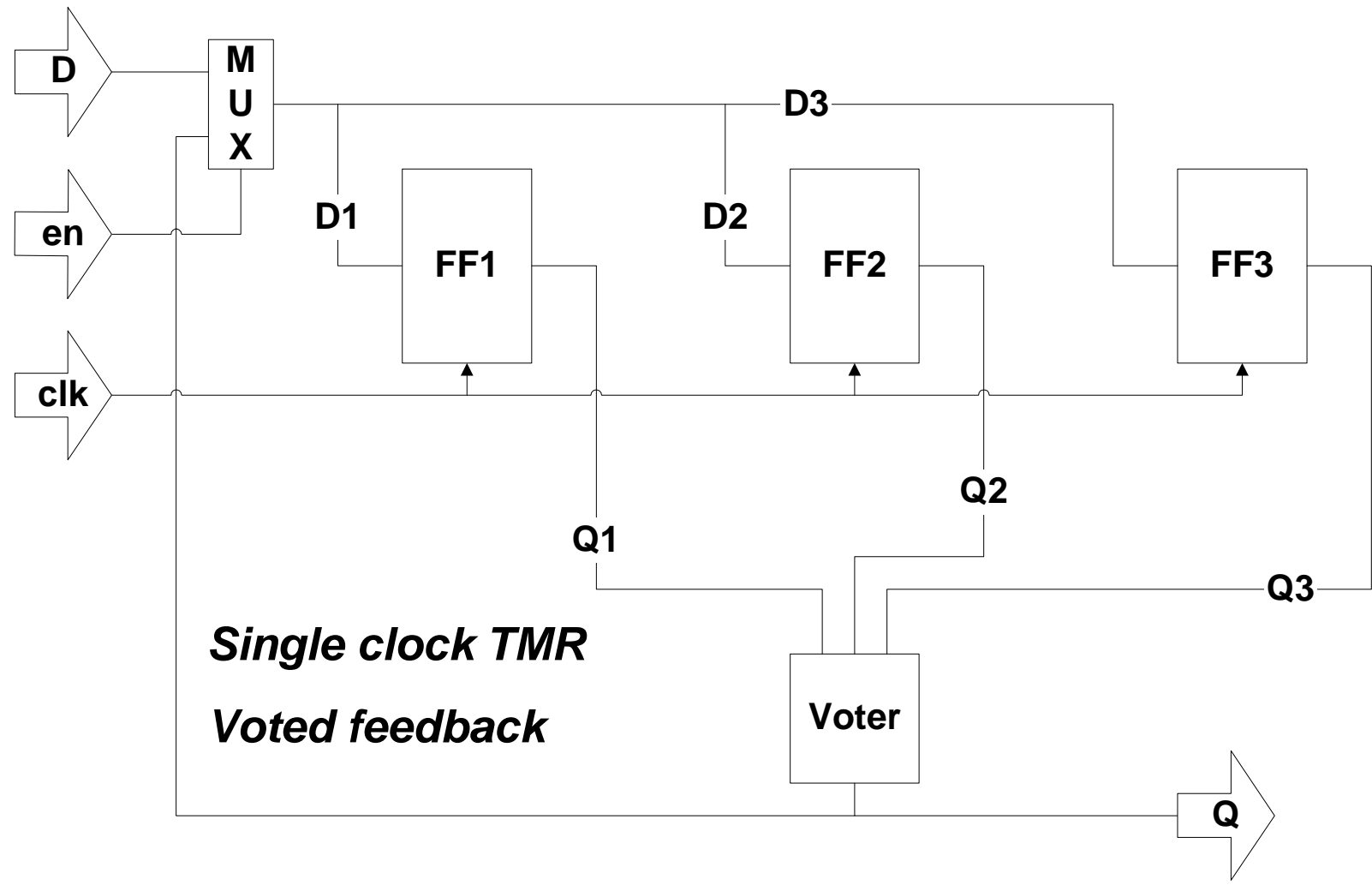


# SEU and SET Fault Tolerance

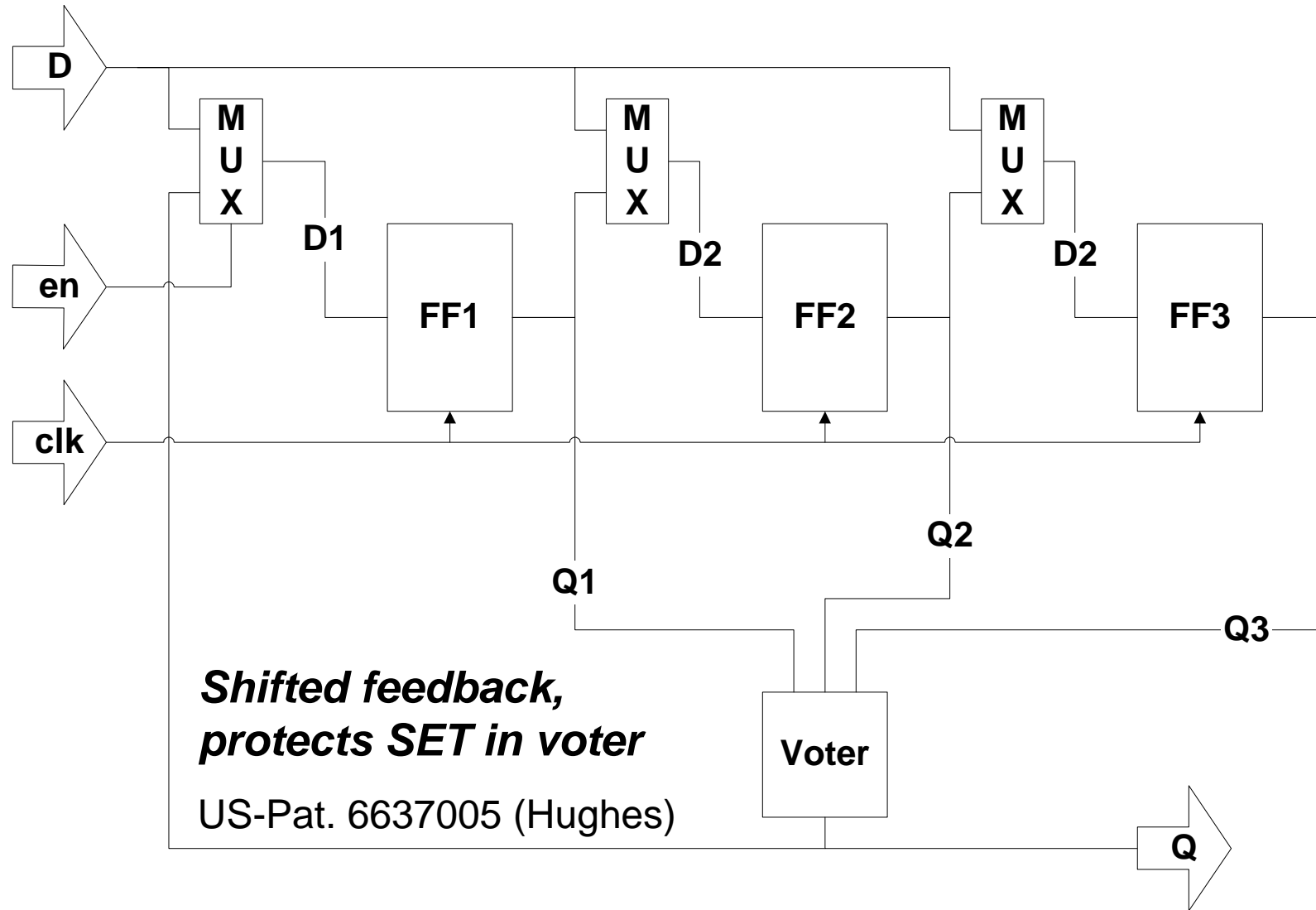
- ◆ **EDAC and parity protection protect against Single Event Upsets (SEU)**
  - ▲ Used for internal and external memories – impact on processor control
- ◆ **Triple Modular Redundancy Flip-Flops**
  - ▲ Triplication and voting of every flip-flop in the design mitigates SEU (1)
  - ▲ Increasing importance of Single Event Transient (SET) in combinatorial logic
  - ▲ SET protection in voter logic by shifted feedback (2) (not implemented in LEONFT)
  - ▲ SET protection in clocks (and asynchronous resets) by triplication
  - ▲ LEON-FT: SET protection in all combinatorial logic by skewing the clock edges
    - » Delay  $\delta$  between the clock trees technology dependent (SET pulse length)
    - » Increases minimum clock period by  $2\delta$
    - » Risk of hold time problems
    - » In LEONUMC: 0.5 ns fixed  $\delta \sim 10\%$  of the clock target (10 ns = 100 MHz)
    - » In ATC697 – use programmable  $\delta$  ???



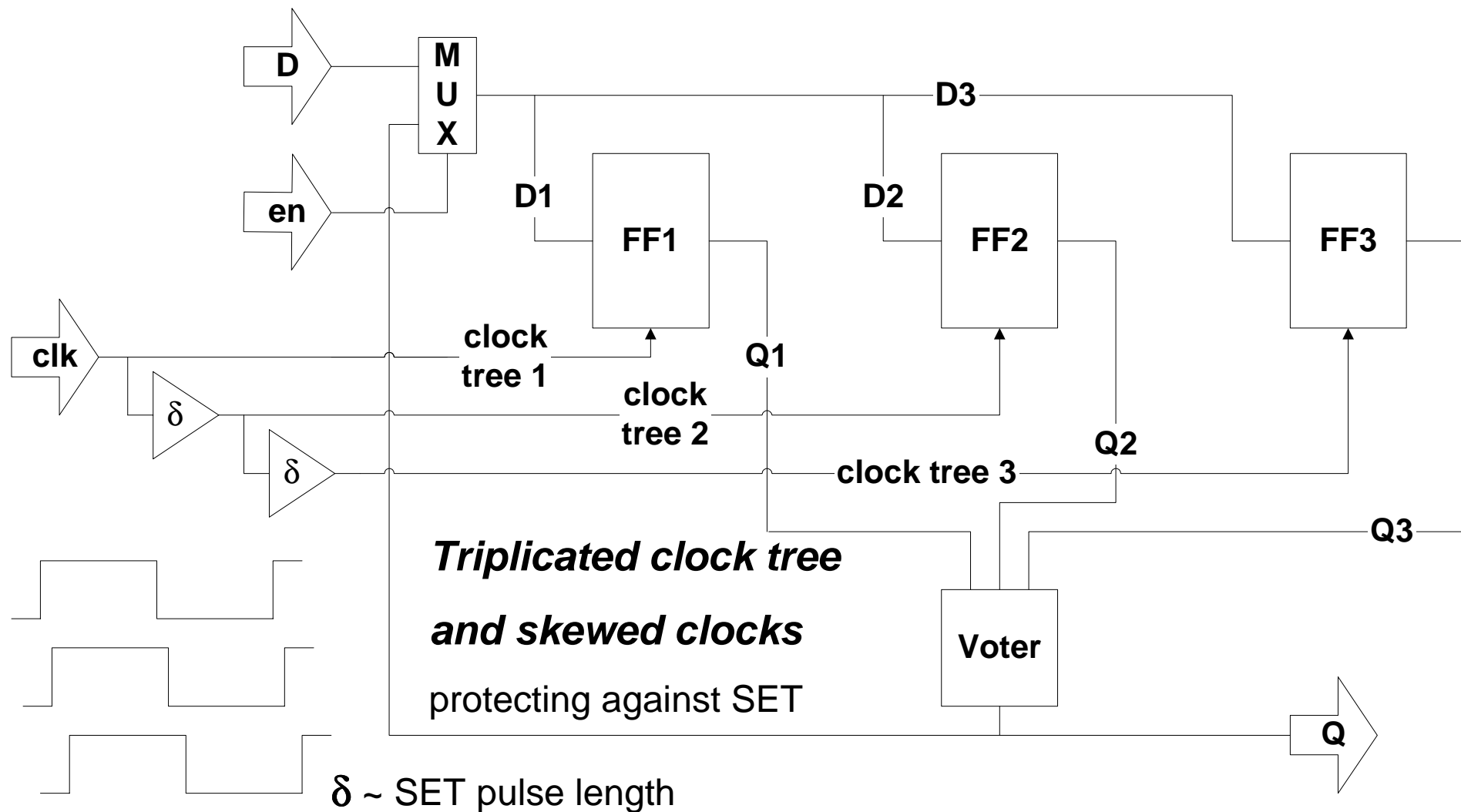
# TMR Flip-Flop with enable (1)



# TMR Flip-Flop with enable (2)



# TMR Flip-Flop with enable (3)



# TMR Flip-Flop Insertion

## ◆ 'Native' in VHDL-RTL source code

- ▲ TMR can be instantiated or inferred
- ▲ Mixed TMR and non-TMR RTL code requires resolution function for clocks

```
entity DFF1_TMR is
  port ( clk : in std_logic_vector(2
        downto 0) ; -- triplicated clock
        d : in std_logic;
        q : out std_logic );
end;

-- One process per TMR Flip-flop
rx0 : process(clk) begin if
  rising_edge(clk(0)) then r(0) <= d;
end if; end process;
rx1 : process(clk) begin if
  rising_edge(clk(1)) then r(1) <= d;
end if; end process;
rx2 : process(clk) begin if
  rising_edge(clk(2)) then r(2) <= d;
end if; end process;

-- Voting outputs
q <= (r(0) and r(1)) or (r(0) and r(2))
      or (r(1) and r(2));
```

## ◆ At Gate Level

- ▲ Preferred for third party IP's, facilitating maintenance of the source code
- ▲ Library and synthesis tool dependent
- ▲ Unique clock names in RTL source code
- ▲ Synthesise netlist without TMR
- ▲ Use package with equivalent TMR cells for all flip-flops used in the netlist
- ▲ Edit netlist to triplicate clocks (including any clock buffers/inverters), instantiate **TMR cells** instead of **library flip-flops**
- ▲ Carefully inspect edited netlist
- ▲ Resynthesise the edited netlist

```
sed -e 's/CLK\(.*\) std_logic/CLK\1
      std_logic_vector(2 downto 0) /'
-e 's/bufx\(.*\)INVDL/bufx\1INVDL_TMR/'
-e 's/DFF1 port map/DFF1_TMR port map/'
-e 's/DFF2 port map/DFF2_TMR port map/'
netlist_notmr.vhd > netlist_tmr.vhd
```

# Simulation and Synthesis

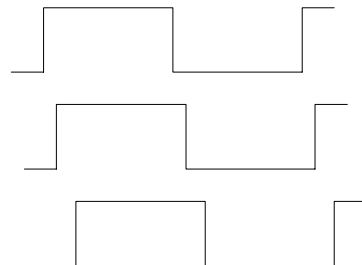
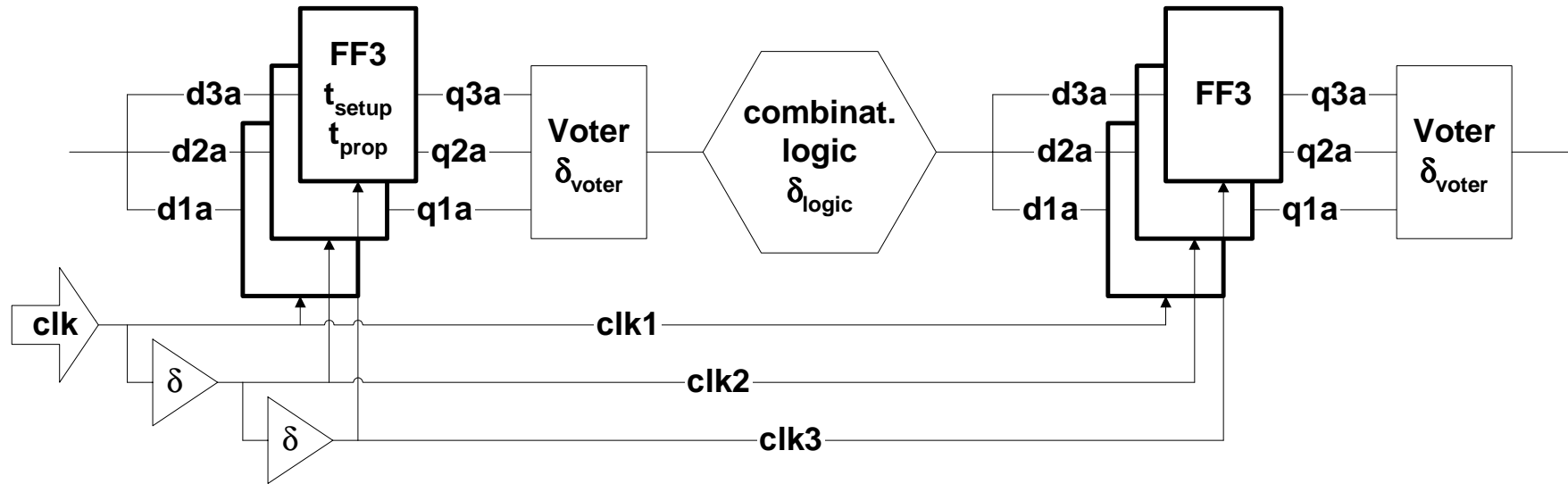
- ◆ **Mixed RTL simulation of 'native' TMR and non-TMR design**
  - ▲ Definition of two clock types (triple and single), connection by a resolution function
- ◆ **1<sup>st</sup> Synthesis of non-TMR block and script-based TMR insertion to netlist**
  - ▲ Overconstraining required to allow insertion of TMR voters
  - ▲ Inspection and resimulation of TMR inserted netlist in 'native' TMR RTL code
- ◆ **Resynthesis of TMR inserted netlist in TMR RTL code**
  - ▲ Retiming of TMR inserted netlist difficult → better use margin at 1<sup>st</sup> synthesis
  - ▲ Conserve TMR in netlist, yet prune unused logic
  - ▲ Conserve triplicated clock nets and define three (virtual) clocks
  - ▲ Instantiated TMR flip-flops → several thousands of design units → critical (in Synopsys)
    - » Selective flattening after elaboration: only flip-flops, not the design hierarchy
    - » No relation between signal names and flip-flop instance names
- ◆ **Post-layout timing analysis and re-optimisation**
  - ▲ Three clock trees per domain with clock delay cells instantiated
  - ▲ Carefully model the clock scenario → propagate clocks
  - ▲ Mandatory hold time fix after each re-optimisation step
  - ▲ Include scan path routing to hold time fix

# Gate Level Simulation

- ◆ **Initialisation of the LEON model with the UMC/VST libraries**
  - ▲ Processor turns 'X' few cycles after reset in timed or un-timed gate simulation
  - ▲ Not FT-related, reported by a university project using the same libraries
  - ▲ Library related – problem never occurred on Atmel libraries
  - ▲ Investigation of modeling in VST Verilog models did not show apparent bugs
  - ▲ Problem remains unsolved... (dirty) workaround:
    - » → reset all flip-flops by simulator command before hardware reset
  - ▲ Leads to ambiguity in production test pattern
    - » some flip-flops are initialised in simulation, but not in reality... workaround:
      - » → run two simulations, one with reset, one with preset, mask all differences
- ◆ **Initialisation of memories**
  - ▲ General problem of all processor designs using on-chip memories
  - ▲ More critical with FT: EDAC affects processor control and facilitates X propagation
  - ▲ → Initialise memory (Verilog) simulation models for netlist verification
  - ▲ → Execute memory initialisation program for test pattern generation
- ◆ **Asynchronous clock domains**
  - ▲ RTL simulation with different clock frequencies (LEON 100 MHz, PCI 33 MHz)
  - ▲ Non deterministic at gate/hardware level (cycle slips, timing violations in synchronisers)
  - ▲ → Use equal (or integer multiple) clock frequencies for test pattern generation



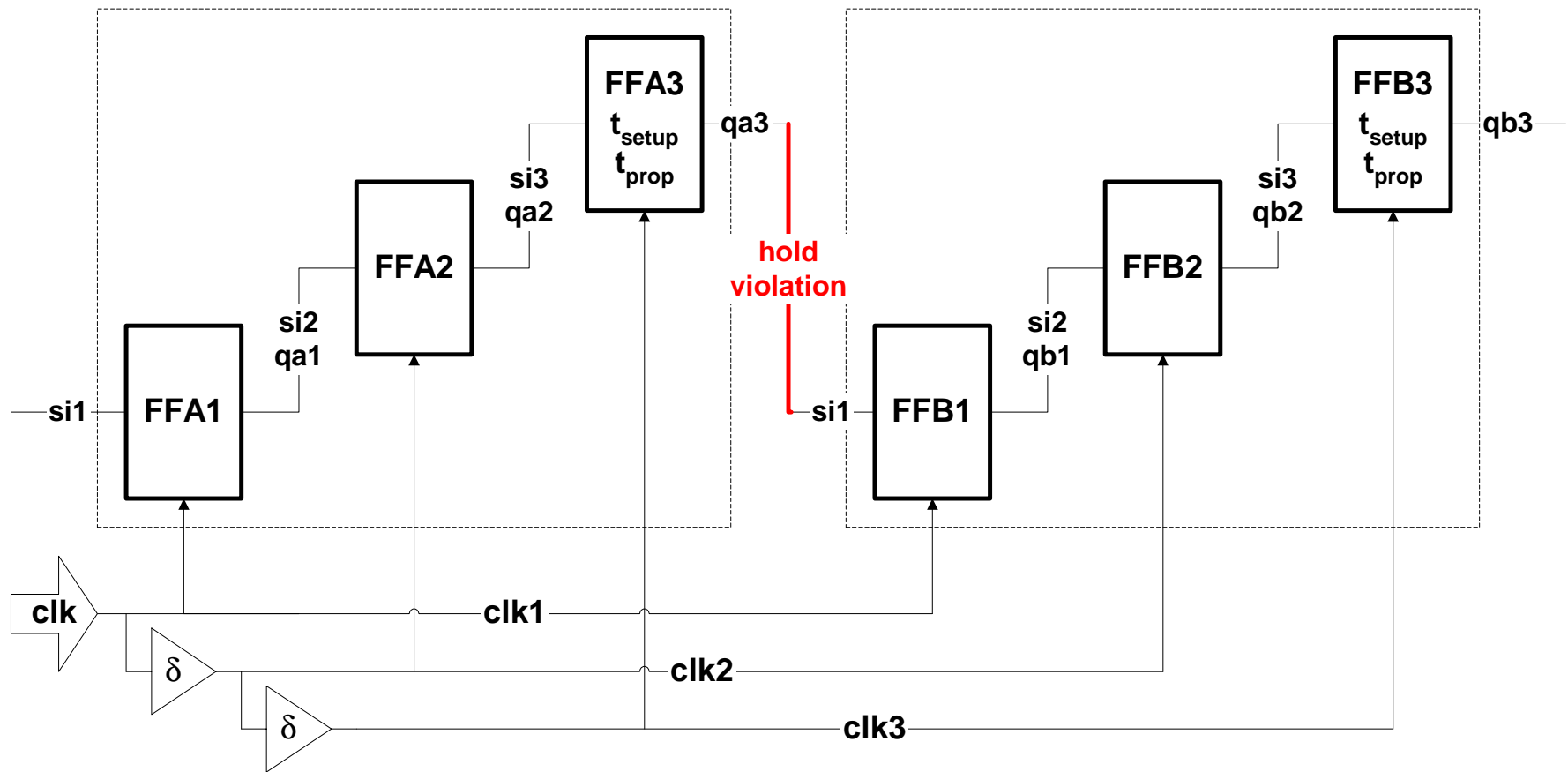
# TMR Timing Issues



$$\text{Cycle Time } T \geq t_{prop} + \delta_{logic} + t_{setup} + \delta_{voter} + 2\delta$$

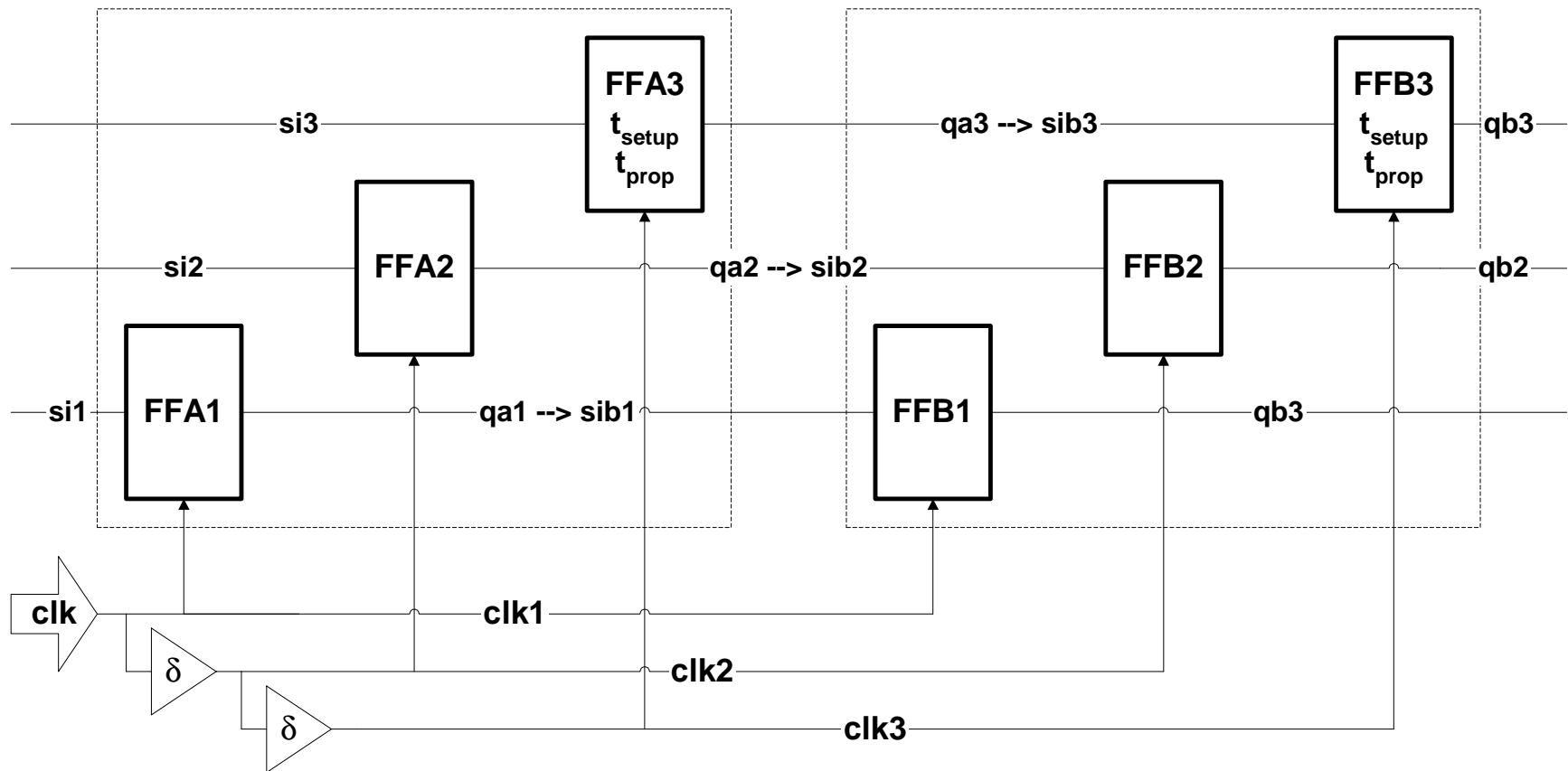
**TMR voters and clock skewing reduce operating frequency**

# Scan Path Insertion (wrong)



Scan path routing across sub-clock domains → **hold violations**

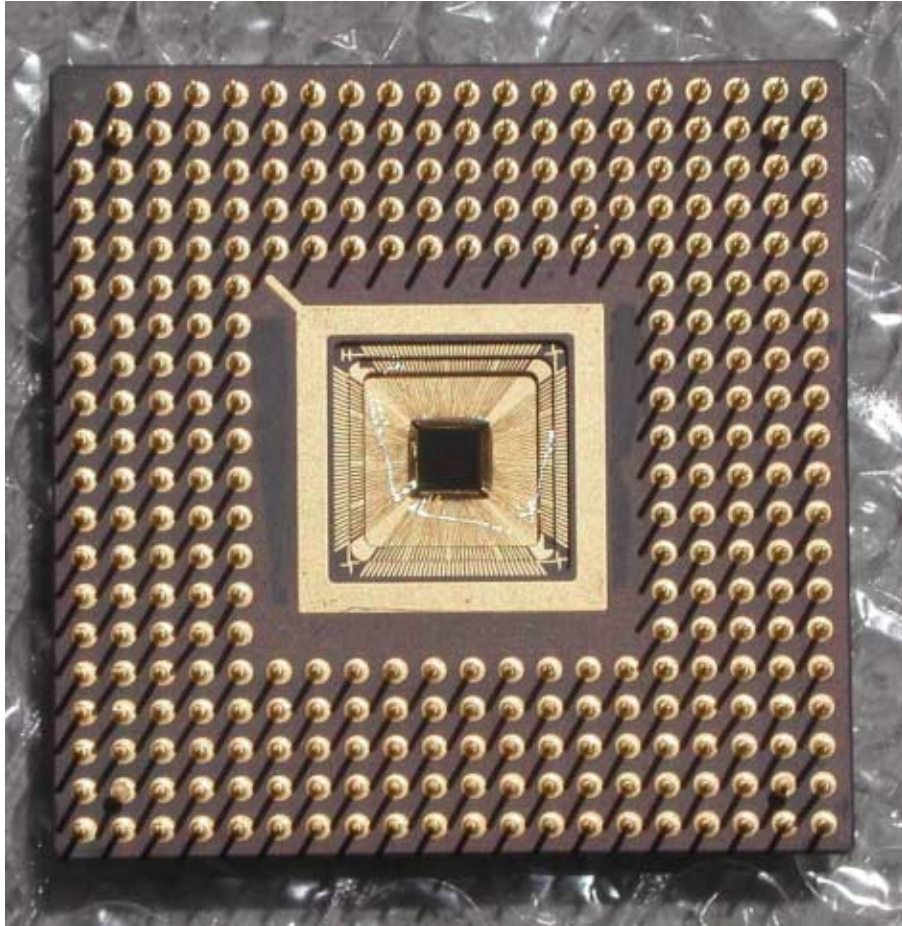
# Scan Path Insertion (right)



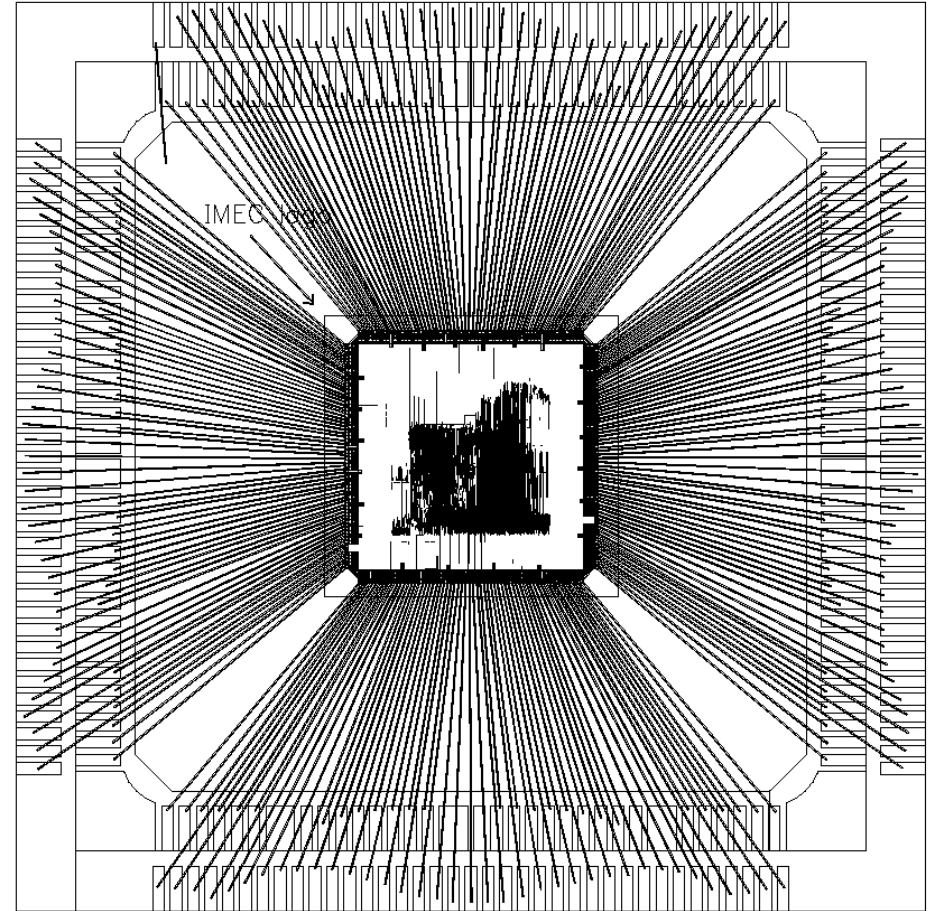
***Better: one scan path per sub-clock domain***

***may also simplify pattern generation***

# Packaging and Bonding



**Ceramic package required for radiation tests: PGA-299**



**Despite a small cavity: Long bonding wires**

# Conclusion

- ◆ **1<sup>st</sup> Silicon of the LEON2-FT in 0.18  $\mu\text{m}$  UMC commercial technology**
  - ▲ Functionally (but not pin) ~ compatible to AT697 -- Prototype board available
  - ▲ 100 MHz clock frequency target confirmed in production test and validation board
  - ▲ Power consumption ~ 5 mW/MHz – power down mode inefficient (in this technology)
- ◆ **Lessons learned**
  - ▲ Critical issues of the LEON processor (reset behaviour)
  - ▲ TMR Implementation in VHDL and netlist
  - ▲ Timing issues in a multiple (skewed) clock environment
  - ▲ Packaging and bonding of a very small die with high pin count
- ◆ **Basic SEU tests done in Californium environment**
  - ▲ All memory SEU's corrected, no SEU errors in flip-flops detected
  - ▲ More in-depth testing should be performed
  - ▲ See next presentation...