IRIS3
Visual Monitoring Camera … on a chip

ESTEC contract 13716/99/NL/FM(SC)

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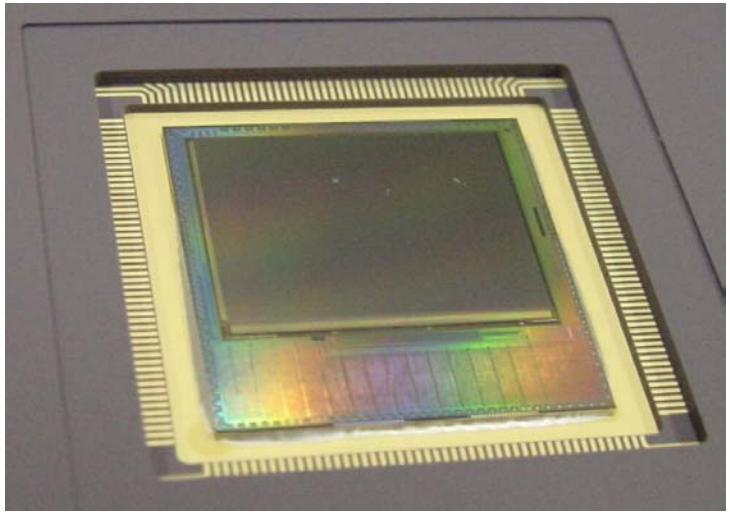


IRIS3

- 1999: IRIS1-based Visual Monitoring
  - Low quality (1997 tech.)
  - FPGA for control/IF
  - Slow data interfaces
  - No local memory (XMXU box on Cluster-2)
  - Not RH
- Do better
  - More image(s)
  - More functionality
  - Less components

IRIS3

- IRIS3 aim
  - Megapixel camera-on-a-chip
  - CCSDS protocol
  - Local image storage
  - Interface to optional processor
  - Rad-hard
  - => heart of a remote instrument

IRIS3

- Study logic
  - Part of ‘new generation’ CMOS APS sensors
  - Synchronised three ESA contracts in 1998
  - Phase 1: development of rad-hard by design method
  - Phase 2: development of three sensor chips
    - STAR250: 512x512 optical beam tracker
    - STAR1000: 1024x1024 sun sensor
    - IRIS3
    - => common technology
  - Phase 3: flight-worthy IRIS3 camera

IRIS3

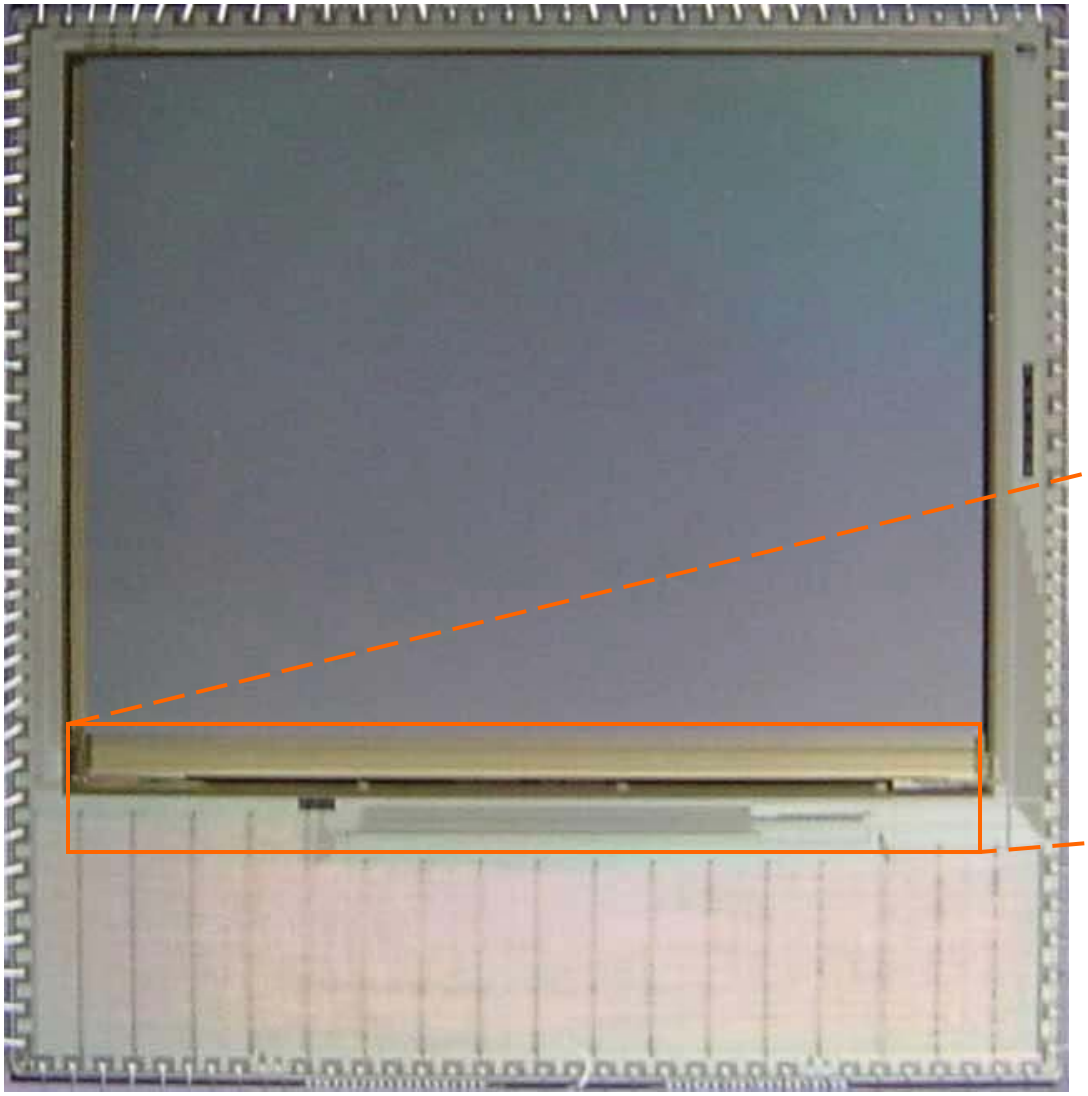
- Time line
  - 2 STARs finished in 2000
  - 2000 FillFactory created
    - Split
      - IRIS3 architecture => FillFactory
      - IRIS3 analogue core => FillFactory
      - IRIS3 logic implementation => IMEC
      - IRIS3 wafer purchase order => FillFactory
      - IRIS3 characterisation => IMEC
      - Flight-worthy microcamera => IMEC
  - 2001 IRIS3 emulated as STAR1000 + FPGA
  - 2002 IRIS3 silicon

IRIS3 Block Diagram

Pixel Array

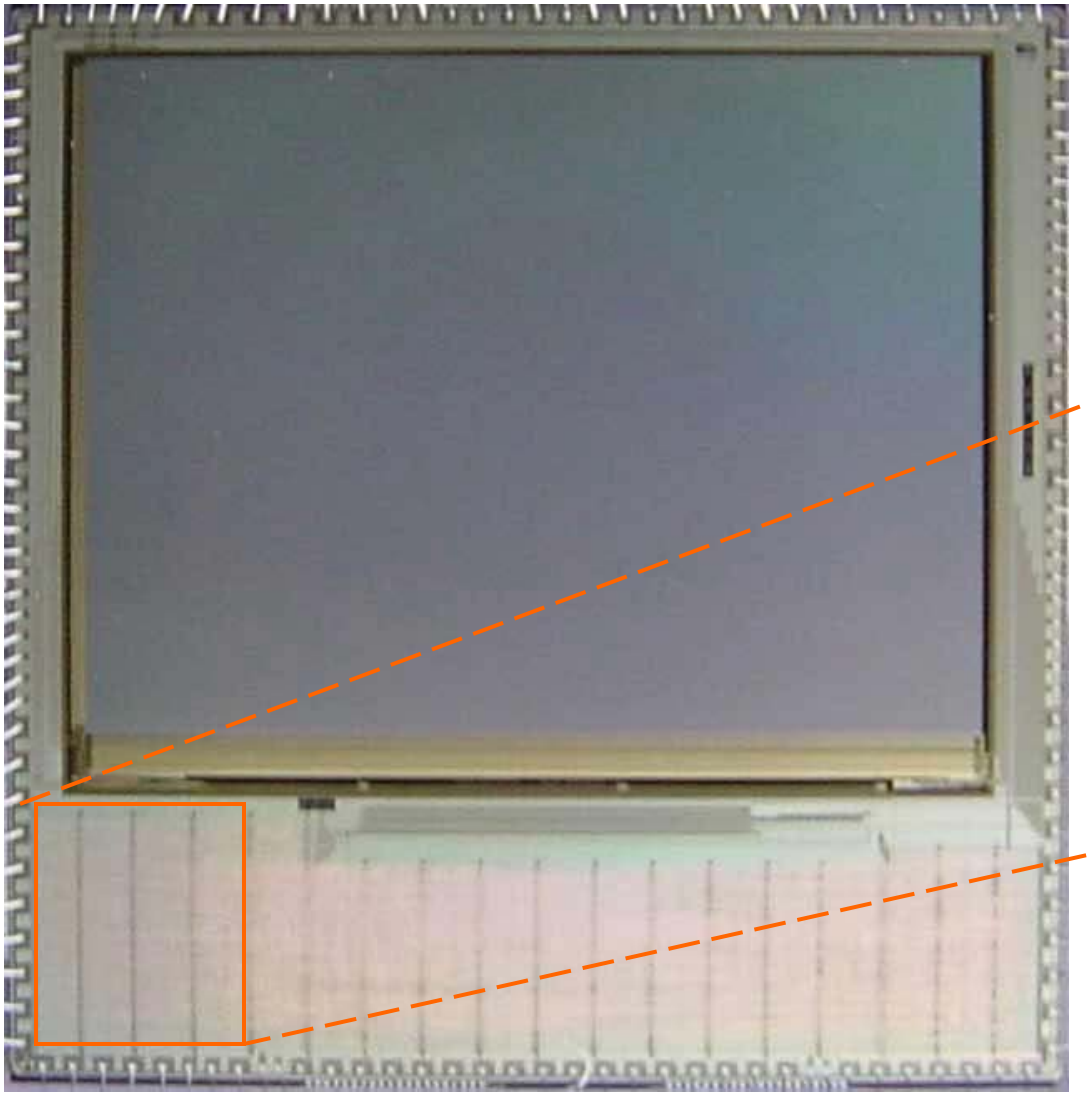
- 1024 x 768
- 15 um
- 1 photodiode
- 3 transistors
- RH-by-design

IRIS3 Block Diagram



Analogue output
- Double sampling columns
- PGA
- 10-bit flash ADC
- RH-by-design

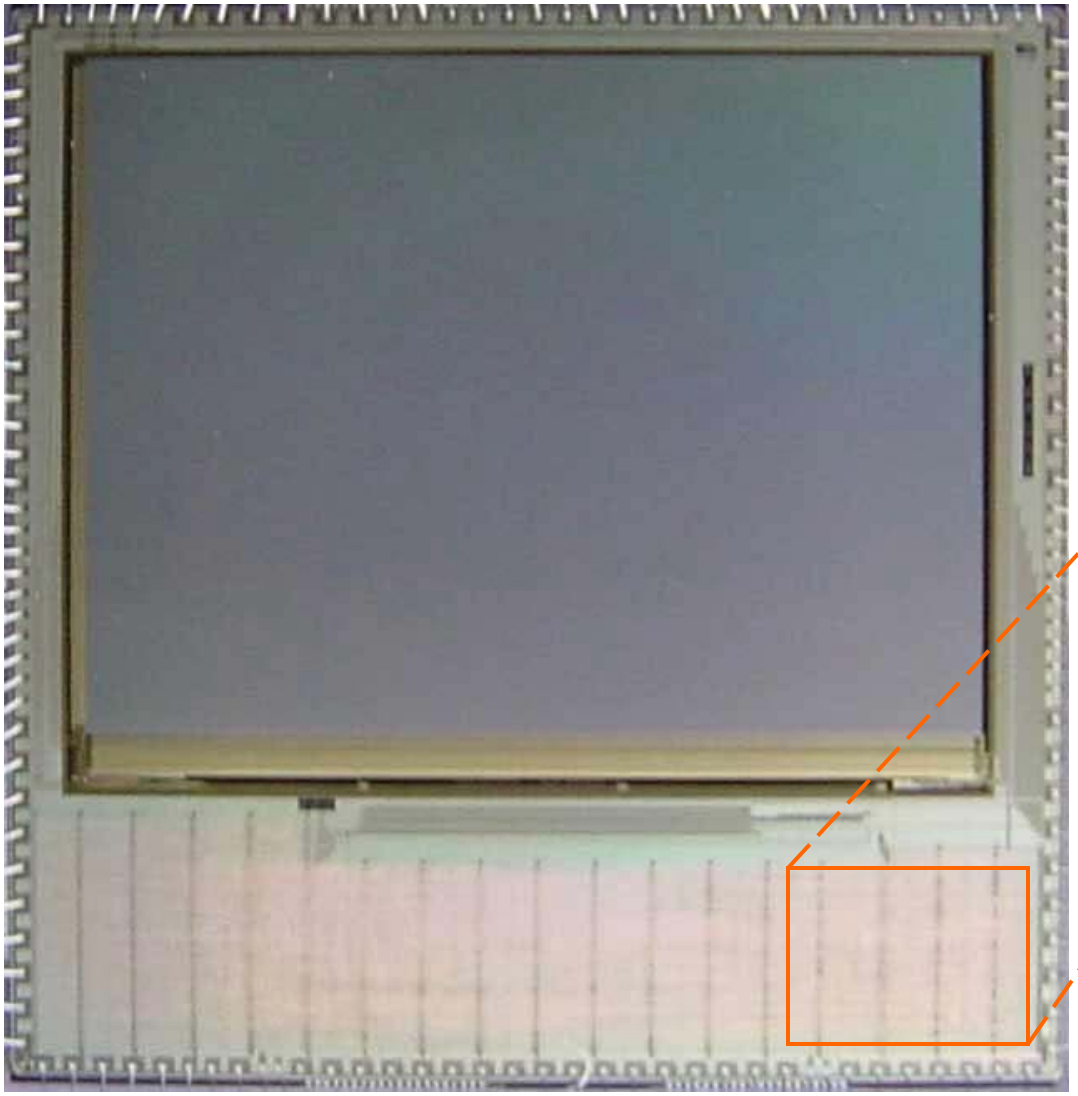
IRIS3 Block Diagram



Readout sequencer

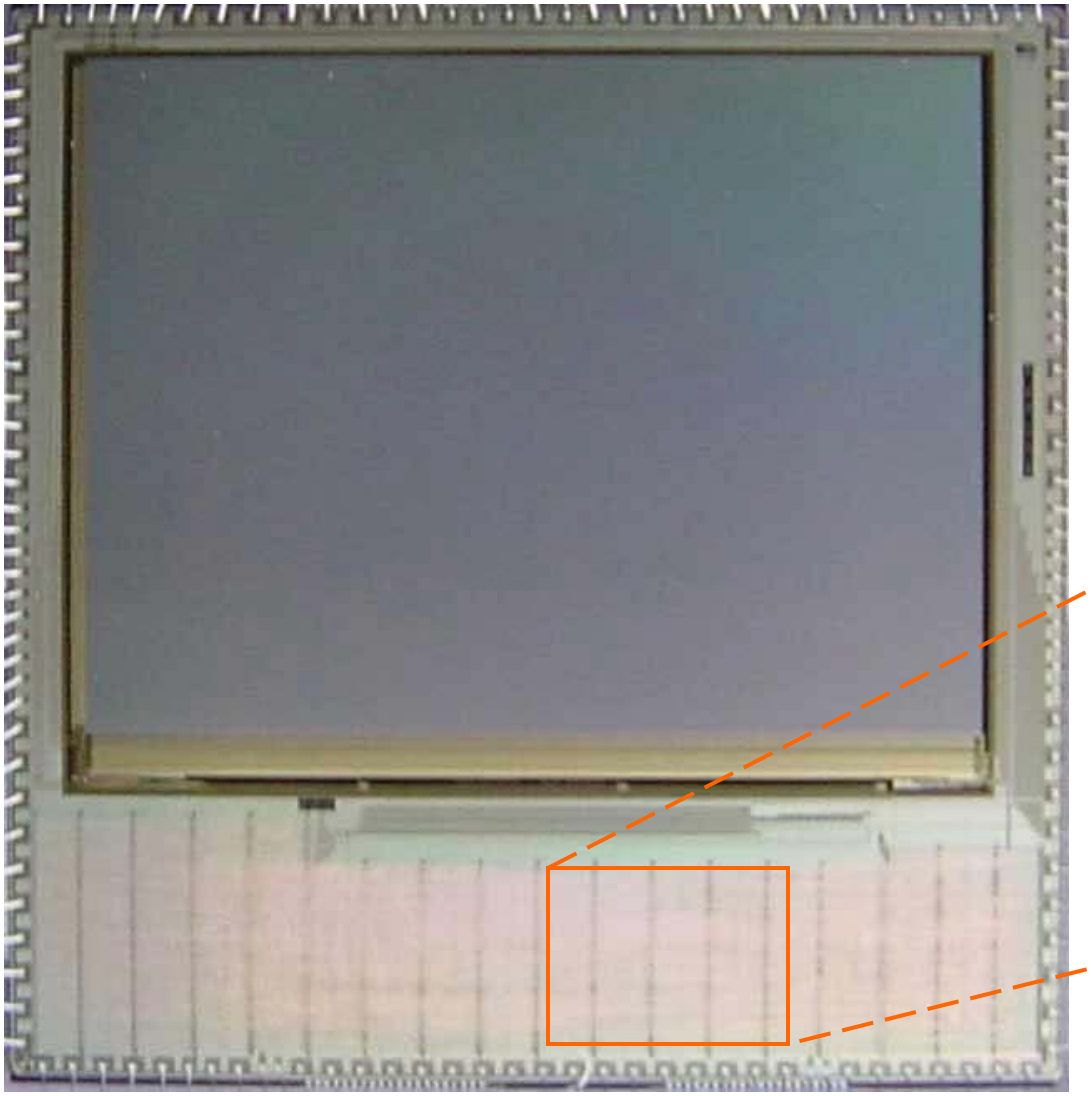
- Focal plane control
- 12.5 Mpixel/s
- Windowed readout
- Subsampling
- …

IRIS3 Block Diagram



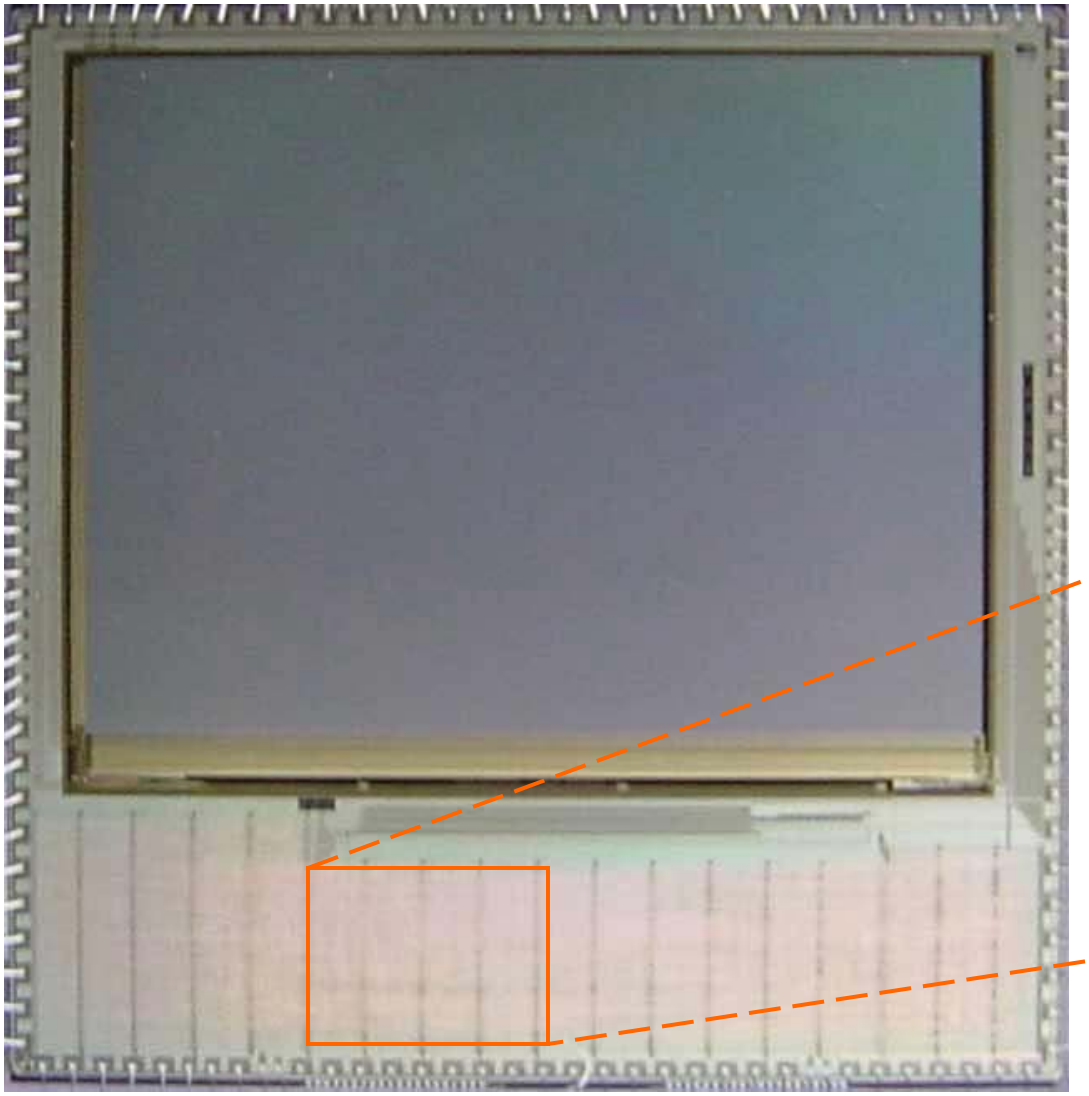
TC/TM interfaces
- PacketWire / TTC-B-01
- Async serial
- Sync parallel
- CCSDS-compliant
- Command gate to processor

IRIS3 Block Diagram



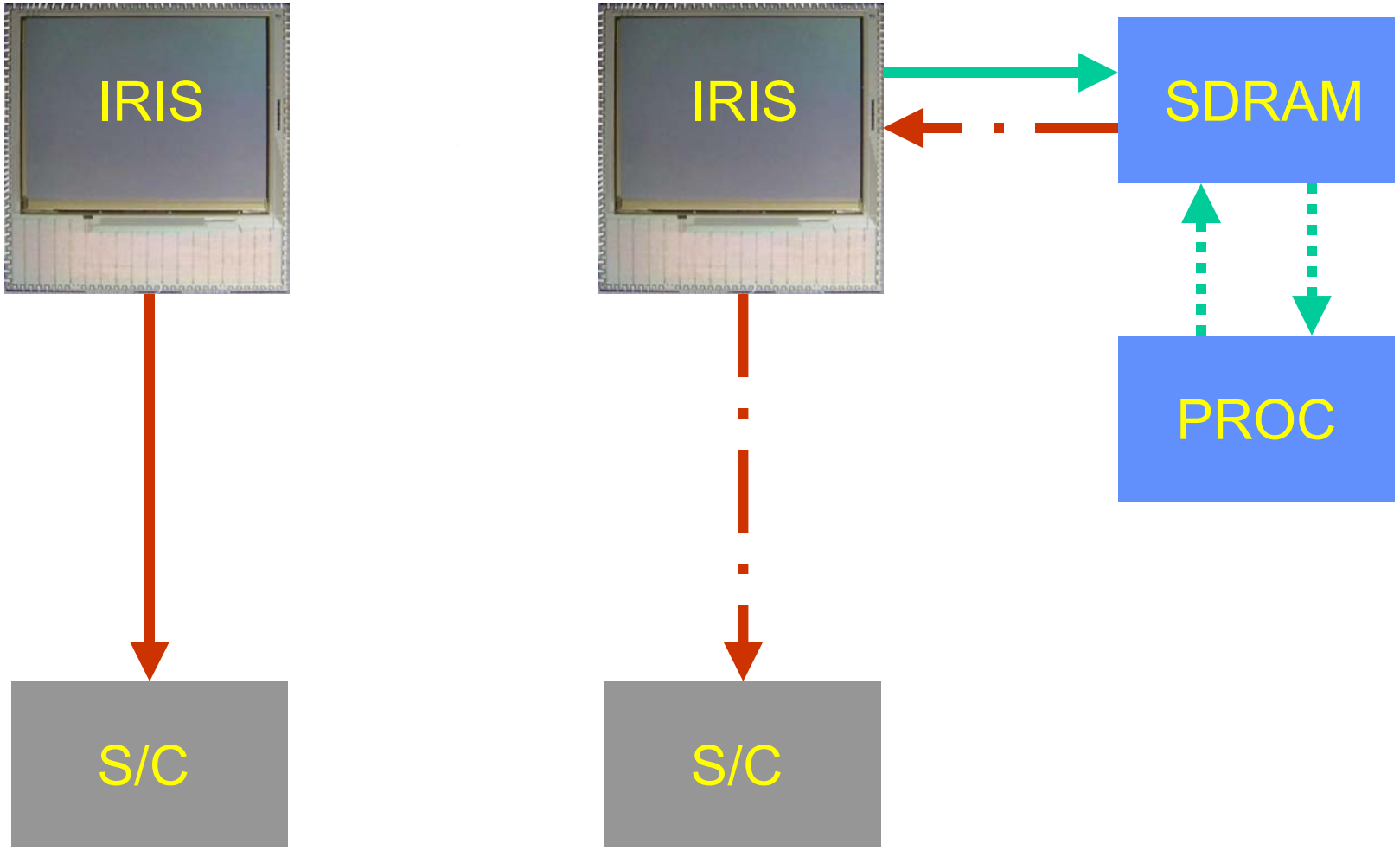
SDRAM IF
- 32 or 64 MWords
- 12 bit + EDAC
- Raw Images
- Compressed images

IRIS3 Block Diagram



Central control
- 36 commands
- Triple registers
- Power-on scenarios

IRIS3 System configurations



IRIS3 Figures

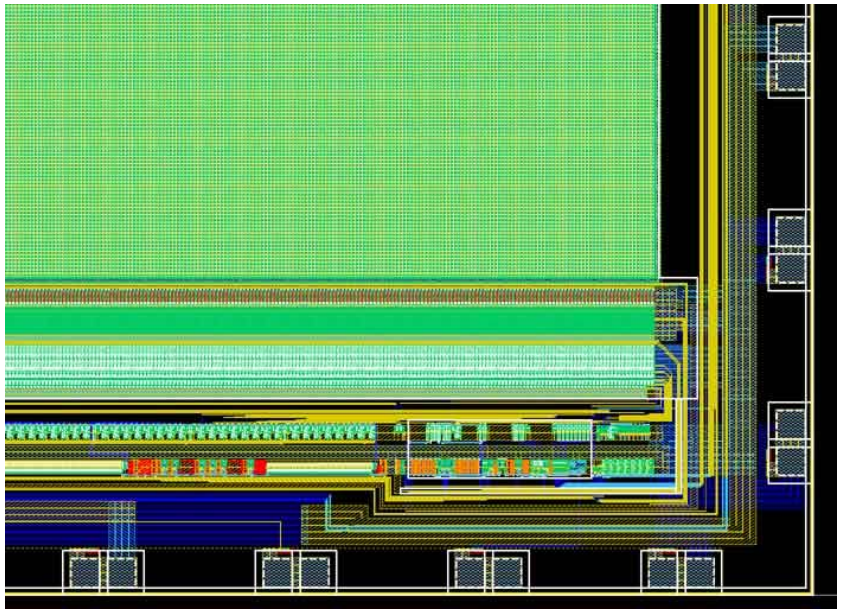
- Format 1024x768 pixels, RH-by-layout
- Pitch 15 um
- Frame rate 12 fps full
  40 fps (512x384)
- SNR 60 dB
- Fixed pattern 0.6 %
- Power 620 mW
- Clock 25 MHz
- Logic ~100 kgates, non-RH

IRIS3 Example

HAS – High Accuracy Star tracker
LCMS – Low Cost low Mass Star tracker

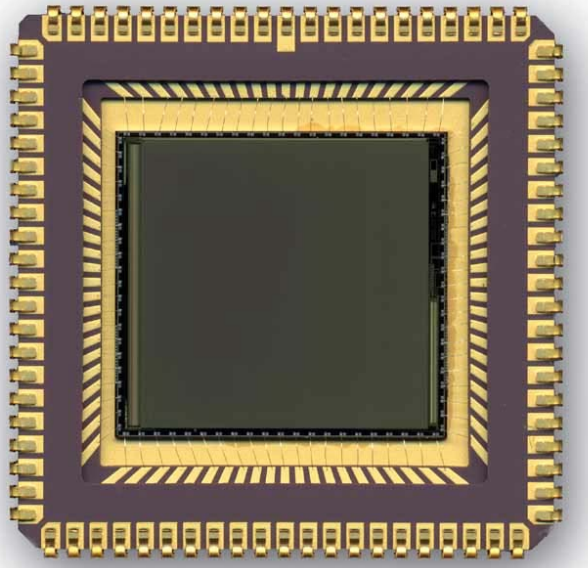
ESTEC contract 17235/03/NL/FM

J.Bogaerts, T.Cools, G.Lepage, W.Ogiers – FillFactory, Mechelen (B)



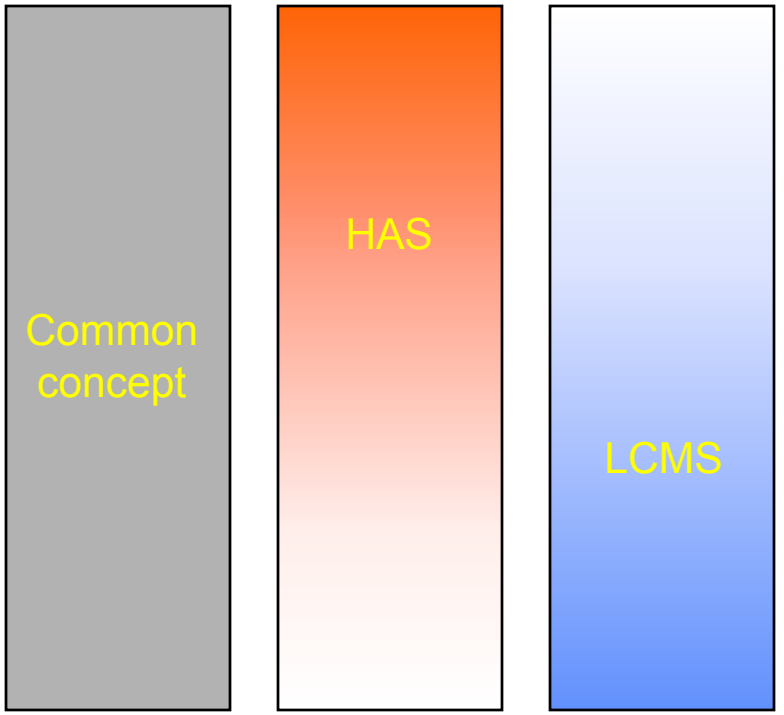
HAS/LCMS Context

- 2000: STAR250/1000 sensors
  - Medium performance generic imagers
  - Radiation-tolerant
  - Star / sun / beam tracking
  - Not application-driven
- 2004: two successors
  - Same look & feel
  - 1024 x 1024 ‘HAS’
  - 512 x 512 ‘LCMS’

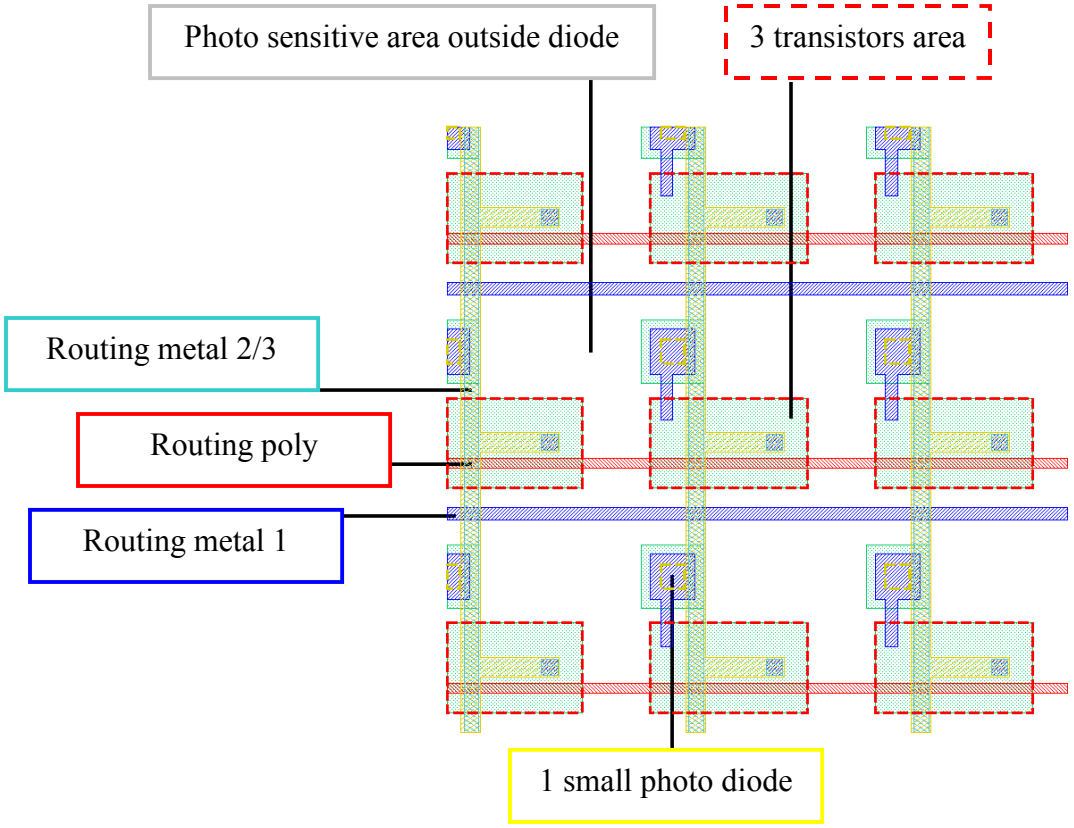


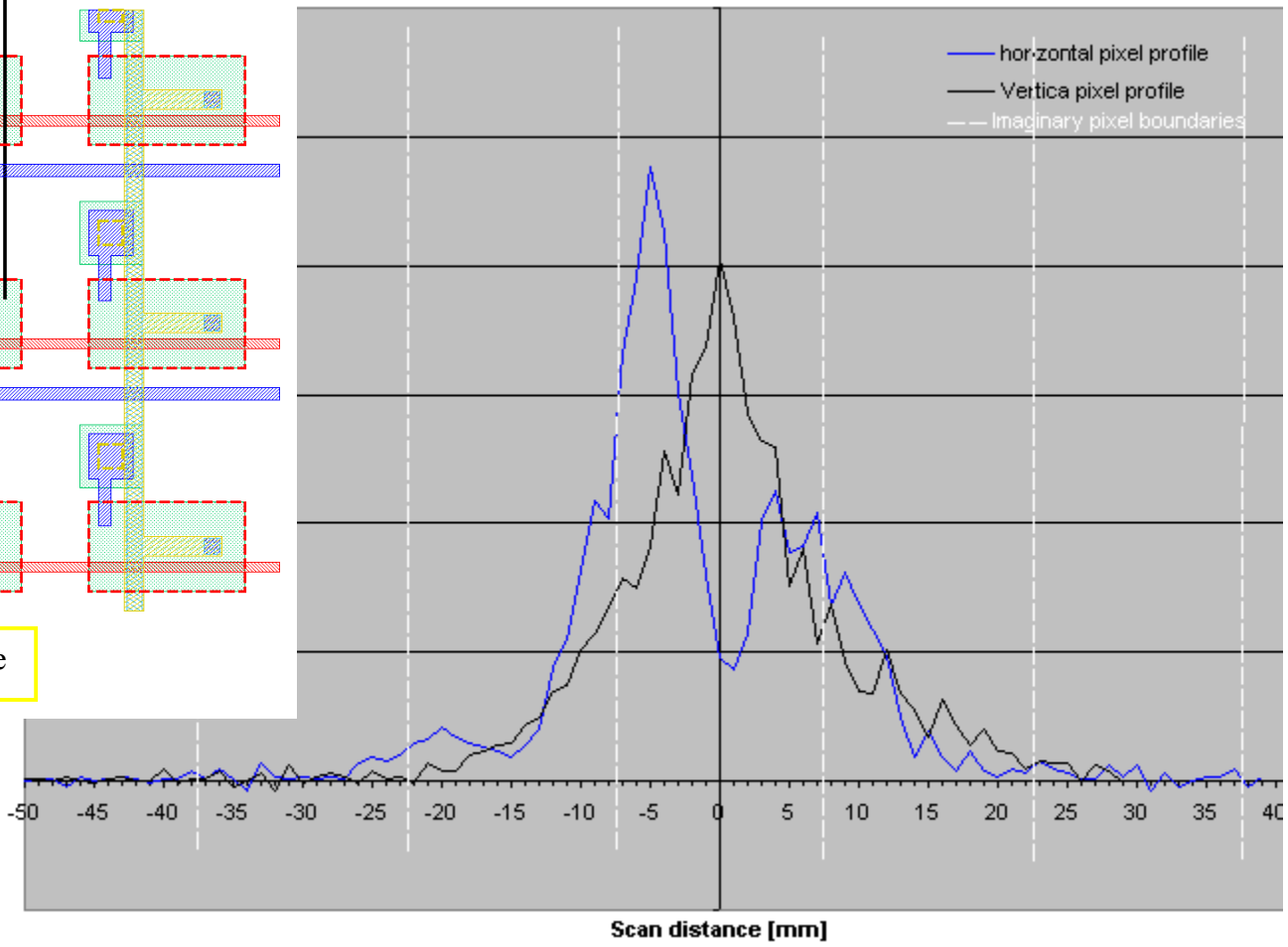
HAS/LCMS Context

- Successor requirements
  - Improve electro-optical performance
    - Noise
    - Fixed Pattern
    - …
  - Fix minor problems of STAR
  - Optimize for tracking
    - Advanced readout
    - Pre-processing

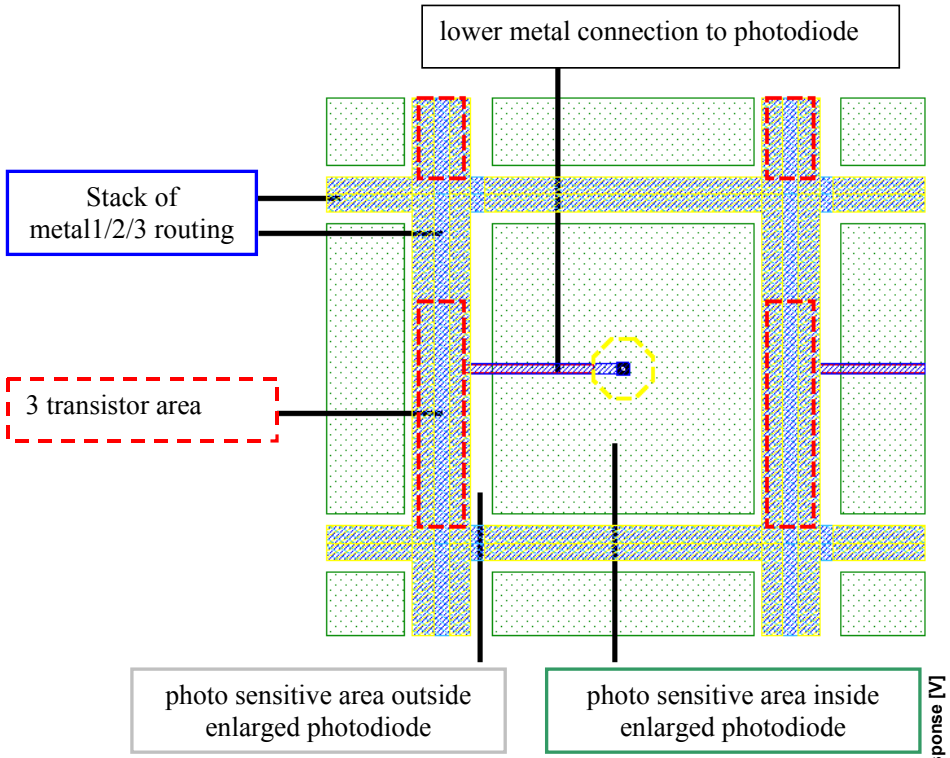


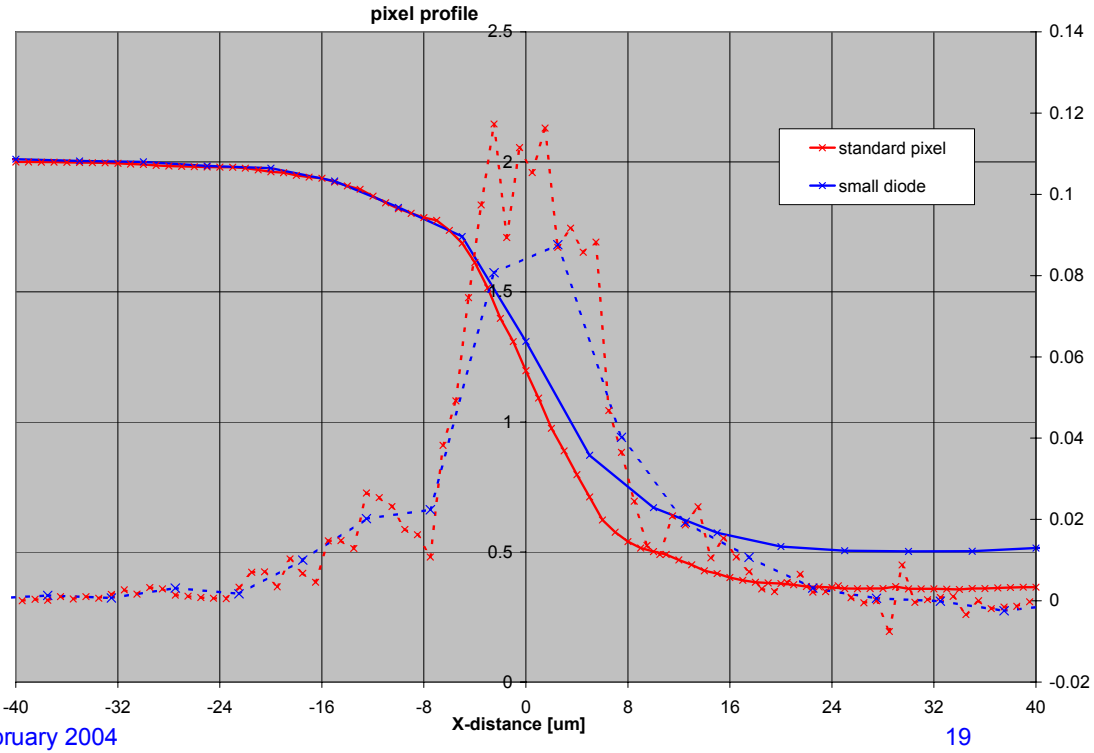
HAS/LCMS Fixing STAR Problems





HAS/LCMS Fixing STAR Problems



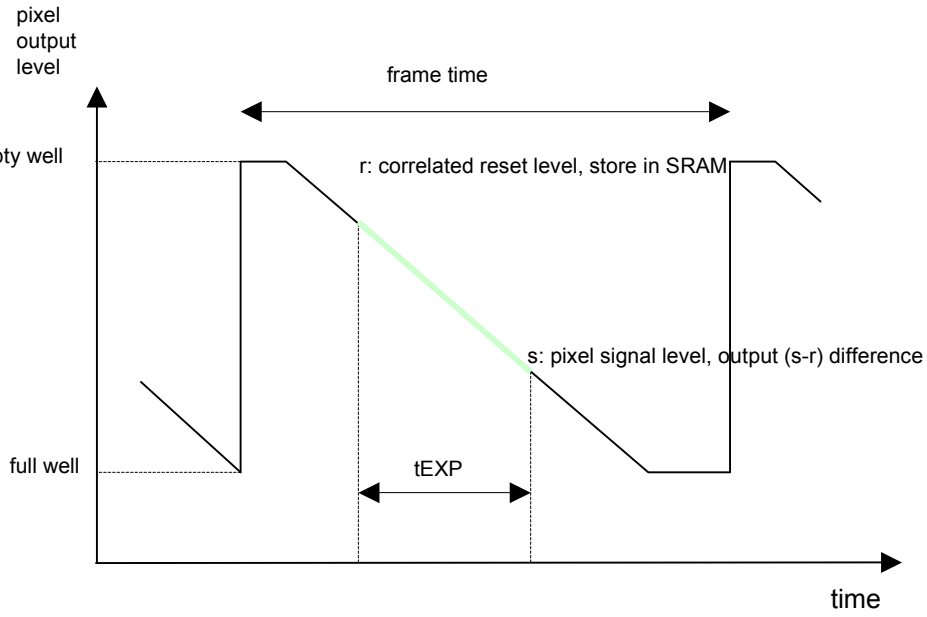


HAS/LCMS Performance Strategy

- Sensitivity
  - 0.5u => 0.35u CMOS
  - 15u => 18u pixel pitch
  - Optional backside thinning
- Dark current
  - Foundry selection
  - Experience with Digital Photography
- Noise and uniformity
  - Double Sampling readout as STAR
    - standard performance
  - Correlated Double Sampling
    - Eliminates kTC noise
    - Eliminates non-uniformities

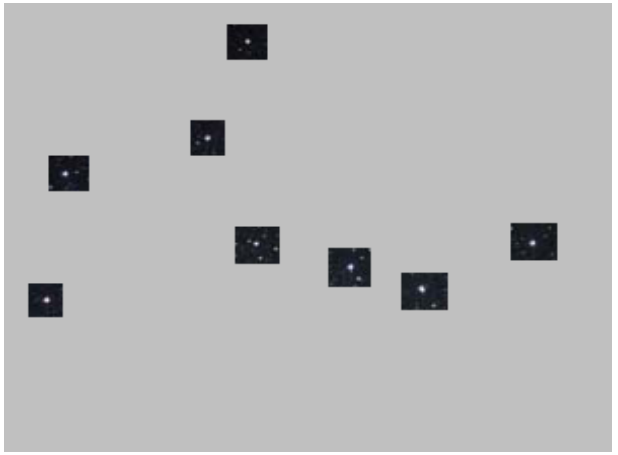
HAS/LCMS Performance Strategy

- Correlated Double Sampling
  - 2-step readout process
    - Reset pixel to ‘black’
      - => contains kTC noise and fixed offset pattern
    - Expose pixel
      - => integrate photo-electrons
    - Read pixel’s ‘signal’ level
    - Difference
      - Output <= (Signal level – Black level)
  - Requires memory for black levels
    - In-pixel
    - External, in system
  - How much memory?
    - Depends on application



HAS/LCMS Operational Requirements

- Star sensor operating modes
  - Acquisition = find reference stars
    - Full frame readout @ 5 frames/s
    - Performance not criticial
  - Tracking = follow stars precisely
    - 40 (20) windows of 20x20 pixels @ 10 ‘frames’/s
    - Each with individual exposure time / gain
    - Performance critical



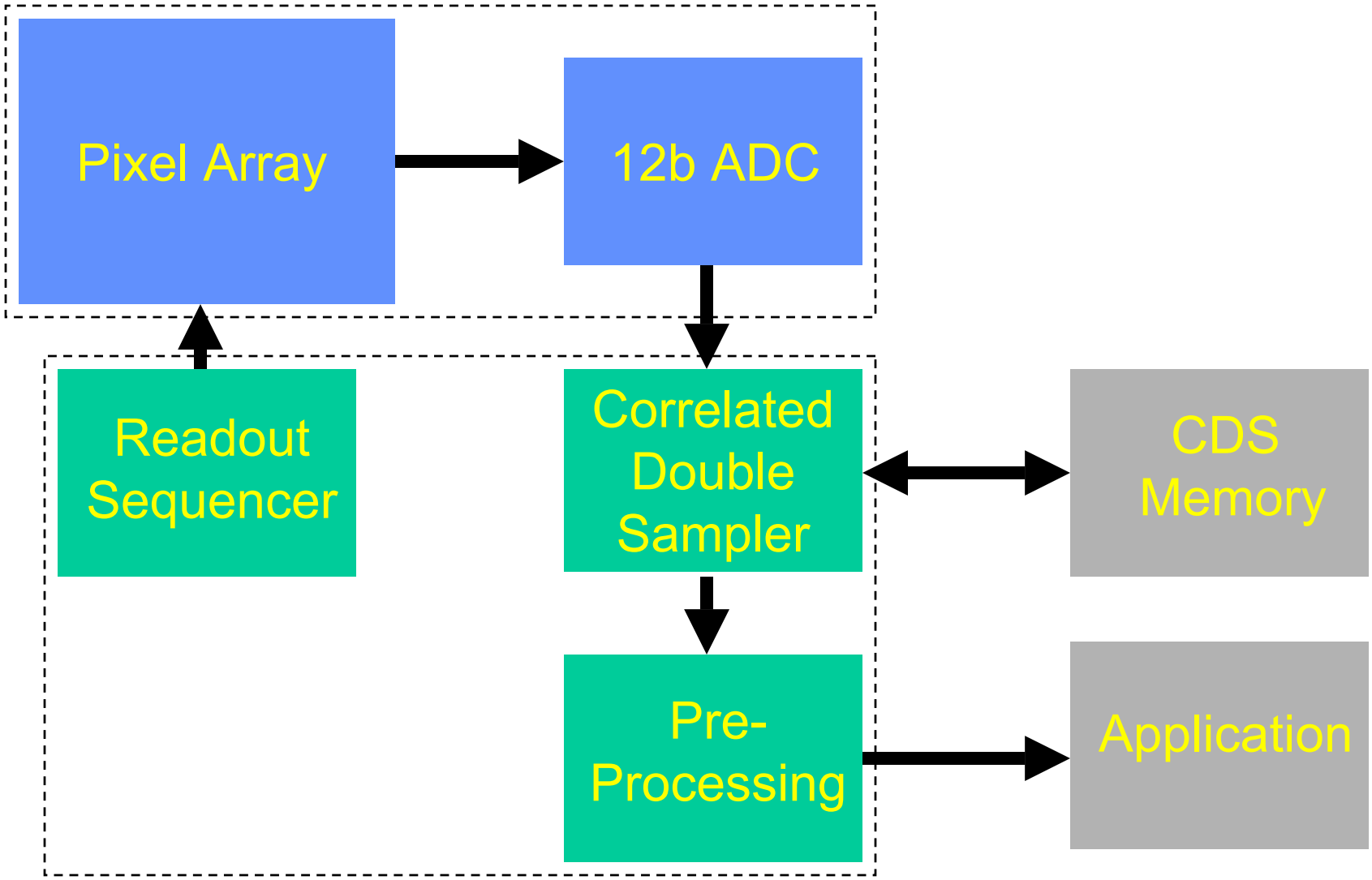
HAS/LCMS Operational Requirements

- Support windowed readout
- Support CDS and CDS memory
  - High-End application
    - CDS for acquisition and tracking
    - 1 Megapixel @ 12-14 bits/pixel memory
    - High performance
  - Low-Cost application
    - CDS only during tracking
    - 20 x20 pixels x 20 windows = 8 kpixels
    - DS during acquisition, ~ STAR1000 performance

HAS Outline

- HAS
  - About accuracy
  - Low integration
  - Complex system
- HAS includes
  - 1024 x 1024 pixel array
  - Address system supports windowing
  - DS/CDS readout amplifiers
  - 12 bit flash ADC

HAS System Architecture



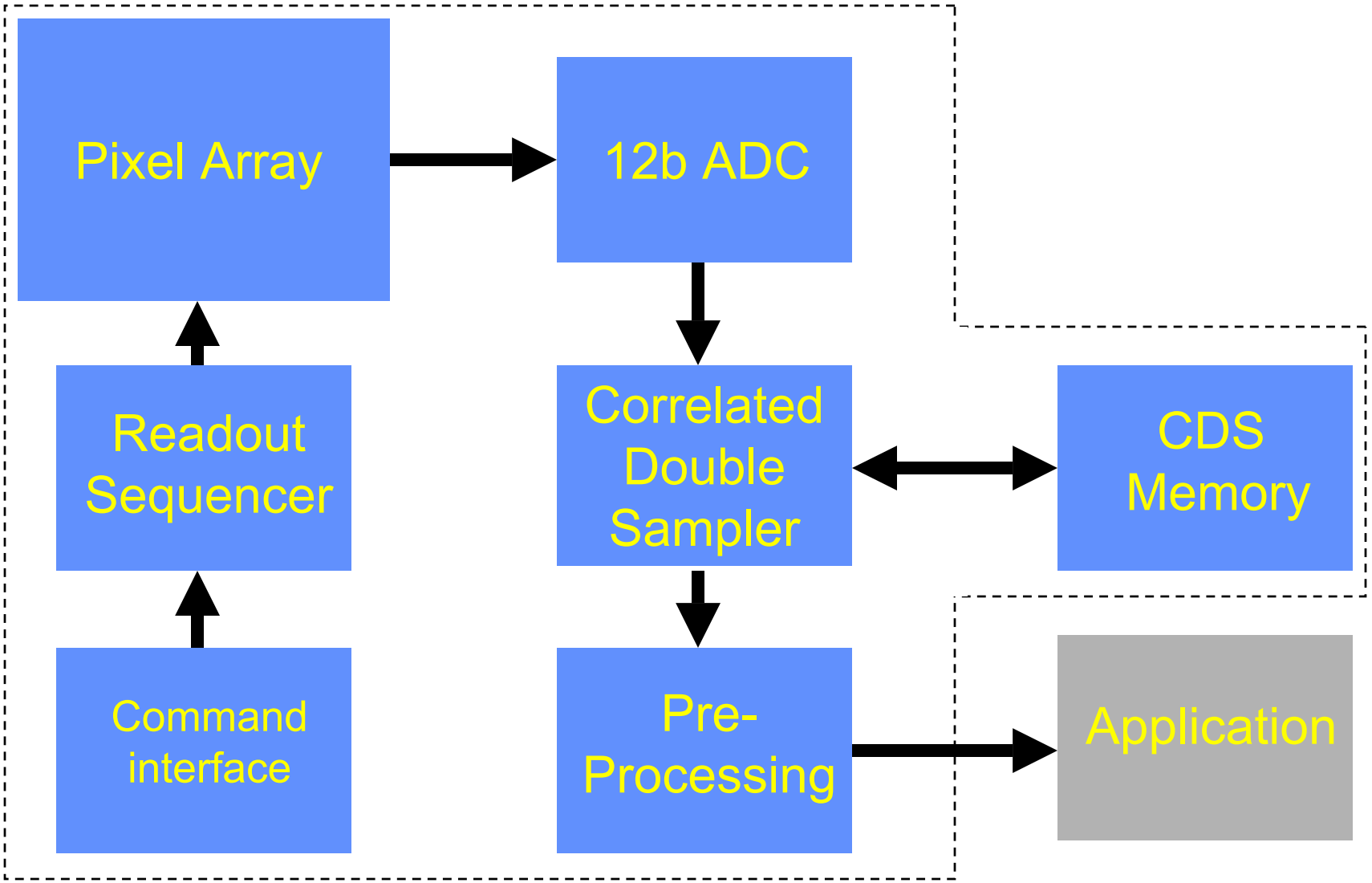
HAS Performance

- Performance
  - BOL Dark Signal: < 2500 e-/s (750)
  - EOL Dark Signal: < 5000 e-/s
  - Readout Noise: < 30 e-
  - Fixed Pattern Noise: < 10 e-
- Radiation-tolerance
  - All parts RH-by-design
  - Expect to meet 100 krad/no LU

LCMS Outline

- LCMS
  - Smallest, smartest star sensor head
  - Without breaking the bank (or our backs)
  - Building on HAS concept
- LCMS includes
  - All of HAS
    - 512 x 512 pixels
    - Up to 20 windows
  - Logic
  - SRAM

LCMS System Architecture



LCMS Operation

- User-controlled
  - Instruction types
    - Reset array
    - Reset window #N
    - Read window #N black level
    - Read window #N signal level and process
  - Operations stored in 12 kbits SRAM
- Window scheduling
  - Impacts application performance

LCMS Pixel Processing

- Correlated Double Sampling
  - On-chip SRAM
    - 20 windows @ 20x20 pixels => 96 kbits + EDAC
  - Output <= Signal level – Black Level
- Background calculation
  - Running average
  - Subtracted from pixel values
- Pixel thresholding
  - Only ‘bright’ pixels pass

LCMS Interfacing

- Command and Data Interfaces
  - SpaceWire
  - Sync/async serial
  - Sync parallel
- SpaceWire
  - Max. 20 Mbits/s (noise!)
  - Point-to-point slave only
  - LVDS and CMOS IO
  - SW based on ESTEC contract IP

LCMS Process

- Technology
  - AMIs .35
  - Analogue
    - RH-by-design
  - Logic
    - Commercial cells
- Rad-tolerance?
  - Process scaling => 30-50 krad

Project Status

- HAS
  - Tape Out — done
  - Samples — May 04
- LCMS
  - Detailed design — … April 04
  - FPGA prototyping with HAS sensor — May 04
  - Tape out — August 04
  - Samples — November 04

Conclusions

- IMEC/FillFactory RH image sensor technology
  - STAR250/1000 sensors
  - Available off-the-shelf
- IRIS3 camera-on-a-chip integration
  - Experiment
- Upgrade & combine
  - HAS low-noise RH star sensor
  - LCMS integrated RT star tracker head
- Available information
  - HAS Detailed Specification: ESTEC, now
  - LCMS Detailed Specification: ESTEC, ~April 2004
  - Contact Stephen.Airey@esa.int