VA64SARA a 64-channel Pre-amplifier ASIC for Superconducting Tunnel Junction Readout

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www.ideas.no

About Ideas ASA

- Located in Oslo, Norway.
- 11 year history in radiation detection.
- World leader in low-noise readout of multi-channel radiation detectors.
- Leading supplier of integrated CdZnTe modules for medical imaging.
- Supplied >200kchannels to astrophysics (AMS, Swift and several smaller projects).
- ASIC, PCB and mechanical design capabilities.
- In-house bonding, probing, packaging and small series production capabilities.
- Small volume and prototype ASIC delivery on our own multi-project wafers.
- Larger volumes on mono-project wafers.
- Complete detector assembly capabilities.
- Strong background in high-energy physics.

Assembly of CdZnTe based gamma camera Prototype for nuclear cardiology. 46000 channels
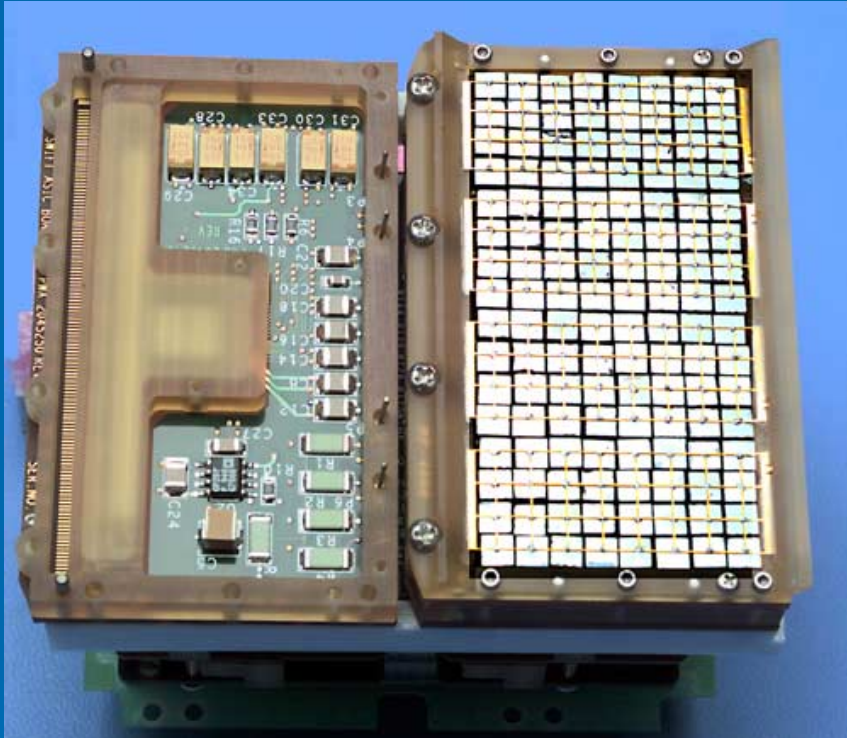Ideas provides complete electronic and mechanical design and assembly.

Detector modules, CdZnTe
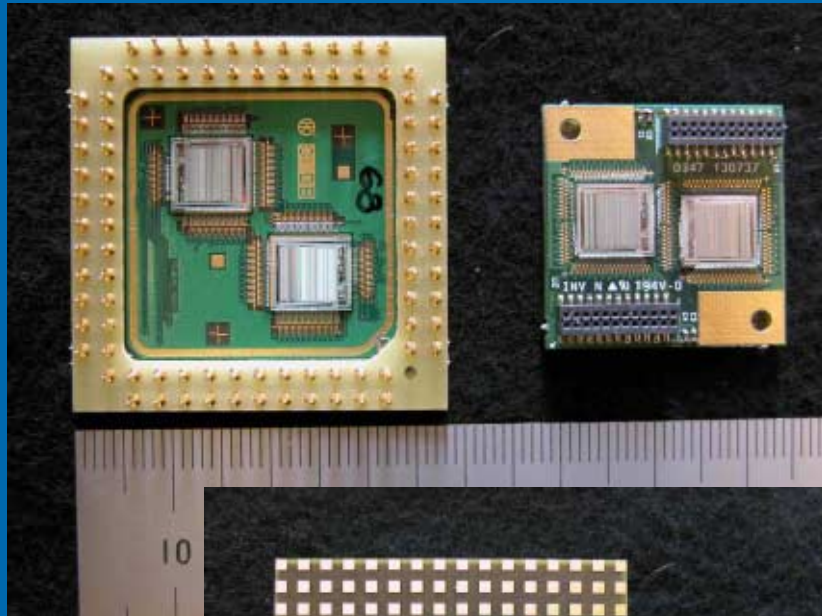
256 channel modules for CdZnTe pixellated detectors, energy range 20-200keV. Pitch 2.46 and 1.6mm. The modules fill the plane without discontinuity in pitch
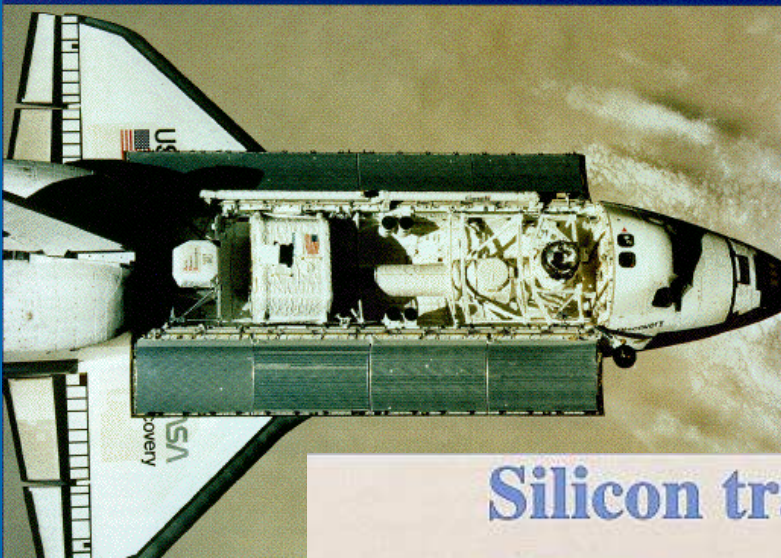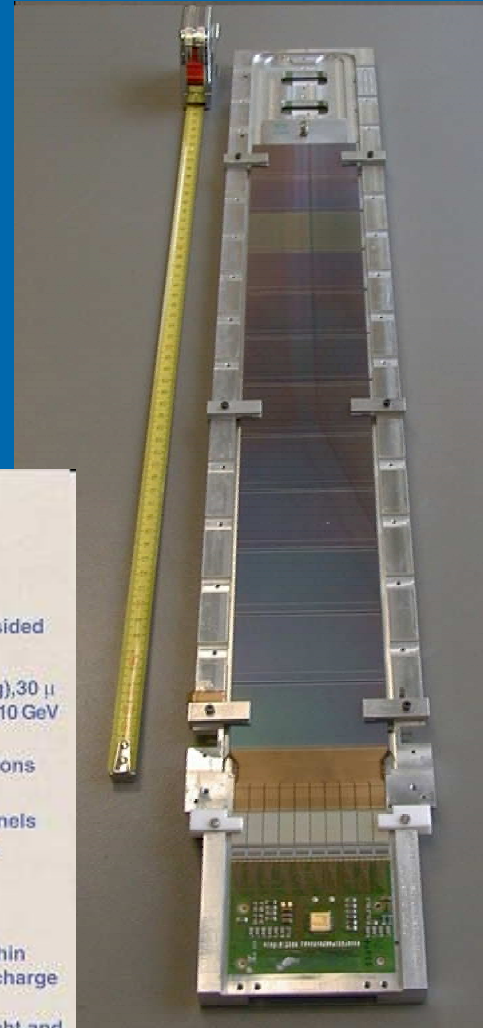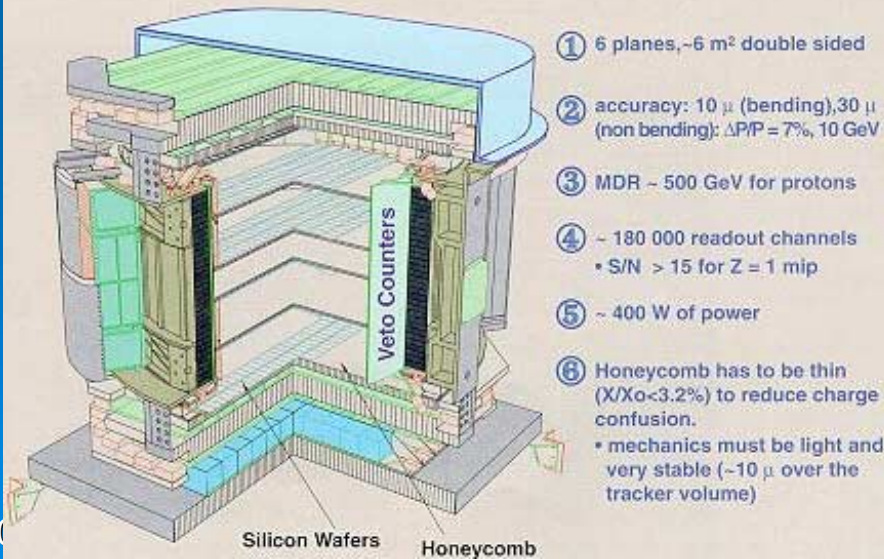Systems from 256 to 46000 channels delivered
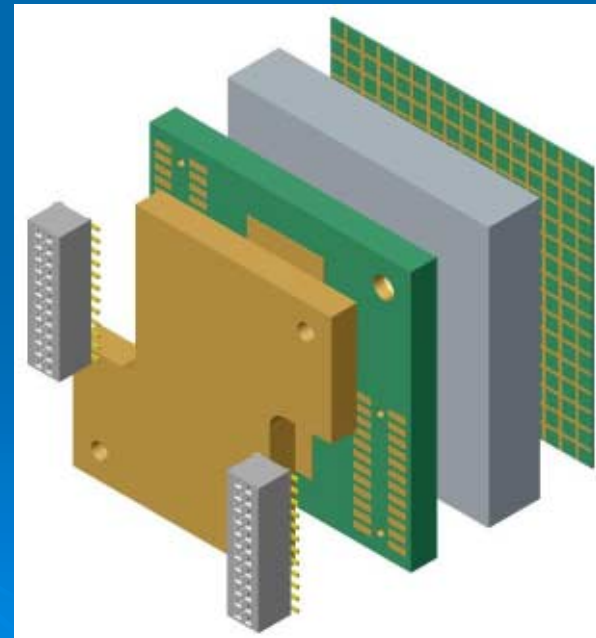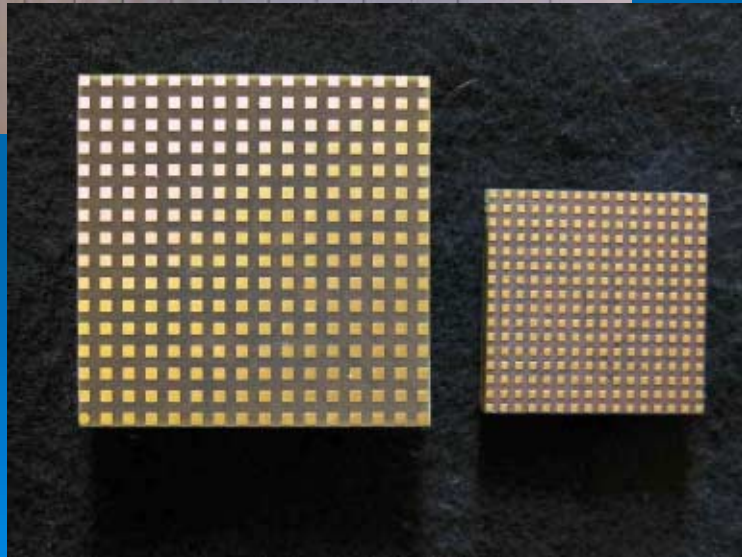
SWIFT

Observation og gamma-ray bursts.
Optical, x-ray and gamma telescope.
Gamma telescope based on 'coded
aperture' CdZnTe and Ideas XA1.2 ASIC
Planned launch mai 2004

AMS antimatter spectrometer

Silicon tracker

① 6 planes,~6 m² double sided

② accuracy: 10 μ (bending),30 μ (non bending): ΔP/P = 7%, 10 GeV

③ MDR ~ 500 GeV for protons

④ ~ 180 000 readout channels
• S/N > 15 for Z = 1 mip

⑤ ~ 400 W of power

⑥ Honeycomb has to be thin (X/Xo<3.2%) to reduce charge confusion.
• mechanics must be light and very stable (~10 μ over the tracker volume)

Veto Counters

Silicon Wafers   Honeycomb

STJ Background

- Superconducting Tunnel Junctions have been extensively investigated as photon detectors covering the range from near-infrared to X-ray energies.
- STJ detector developments now focus on the integration of many devices into large imaging arrays.
- However, current state-of-the-art preamplifier electronics for these detectors still rely on circuits build from discrete components.
- We are reporting here on a first attempt to integrate such circuits into an ASIC
- Very high risk project.
- Two ASICs have been developed. One consists of 64 low-noise, low-offset pre-amplifier channels, while the other contains the same number of shaping filters and threshold detection circuits.
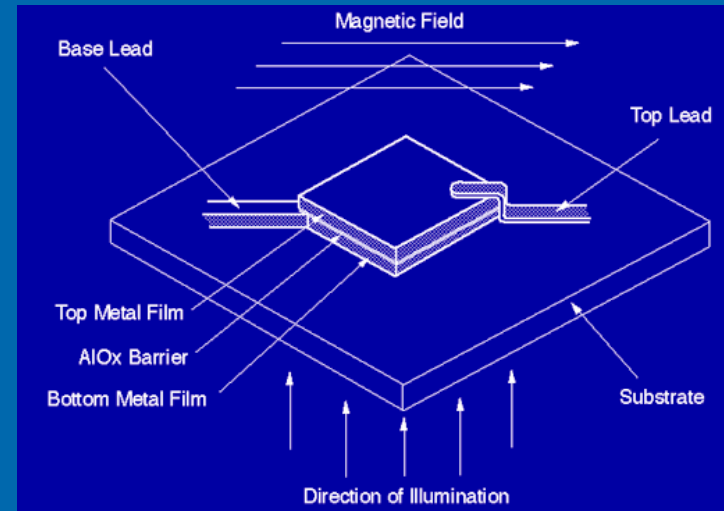
STJ principle of operation

➢ The energy gap of a superconductor, is very small i.e. For tantalum only 0.7meV

➢ Absorption of photons in the superconductor leads to creation of free charge carriers, so-called quasiparticles.

➢ By applying a smal voltage across two superconducting layers isolated by a thin film the quasiparticles may tunnel between the layers and create a photocurrent

➢ The quasiparticles may tunnel several times across the junction and give a larger effective number of charge carriers.

➢ A responsivity of 10e3 to 10e4 is thus observed making it possible to measure the charge with conventional electronics.

photon

Superconducting layer

V

Superconducting layer

insulator
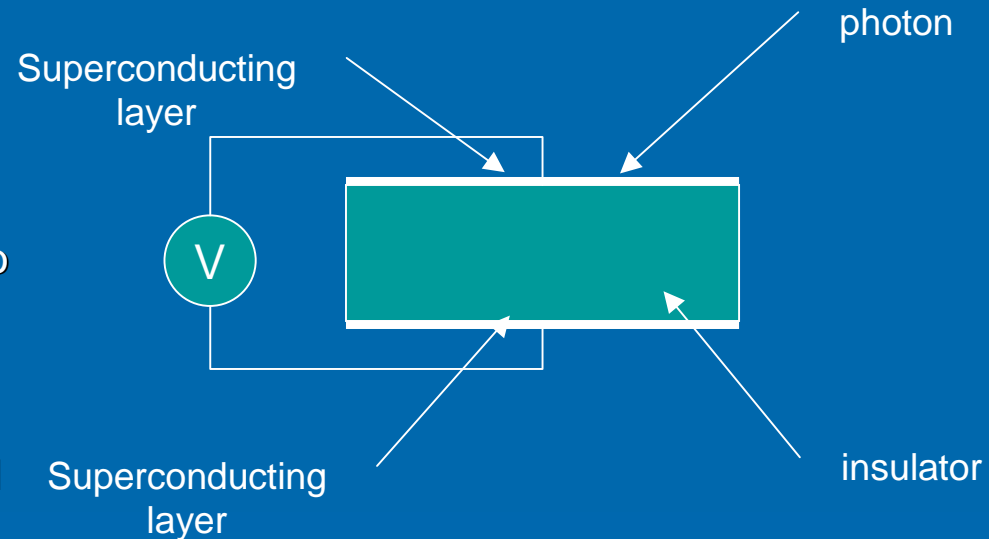
STJ operation

- Cryogenic operation at 0.3K
- Bias voltage in the range from a few μV to <1mV
- Individual biasing for each pixel

Magnetic Field
Base Lead
Top Lead
Top Metal Film
AlOx Barrier
Bottom Metal Film
Substrate
Direction of Illumination

STJ features

- Single photon sensitive imaging spectrometer at optical and x-ray energies
- The three (or four)-dimensional data cube (x,y position, energy and time) output by the instrument can be binned in wavelength a posteriori, eliminating the need for conventional photometric filters.
- STJs have exceptional quantum efficiency and energy resolution in the UV and soft x-ray range
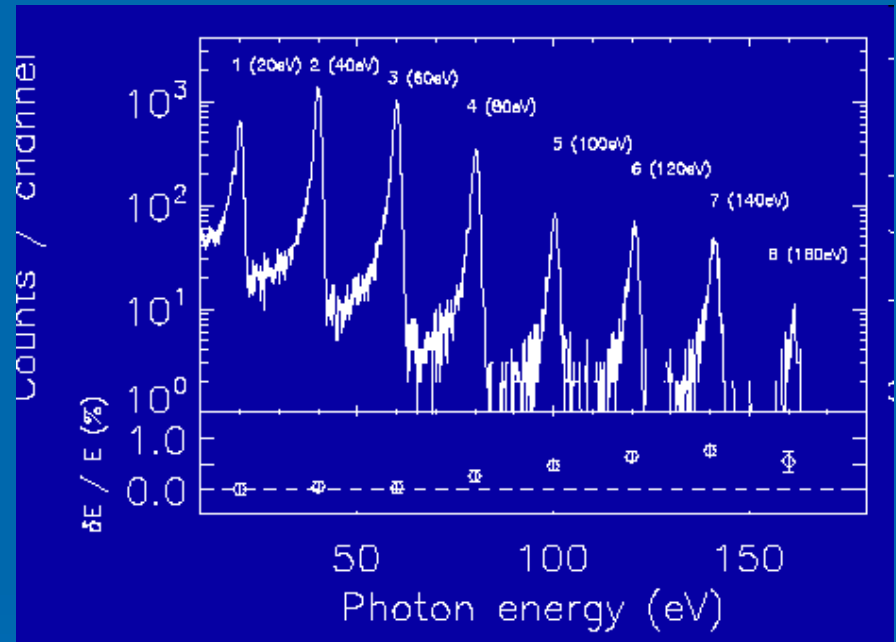
Spectrum obtained with monochromatic 20eV synchrotron radiation from the BESSY I storage ring in Berlin. The multiple peaks are from higher grating orders that were not suppressed.

Biasing of STJ devices

➢ Peaks in the I/V curve complicates biasing

➢ Each pixel has its own characteristics

➢ Required resolution <10µV

➢ → the input offset of each amplifier channel needs to be adjustable
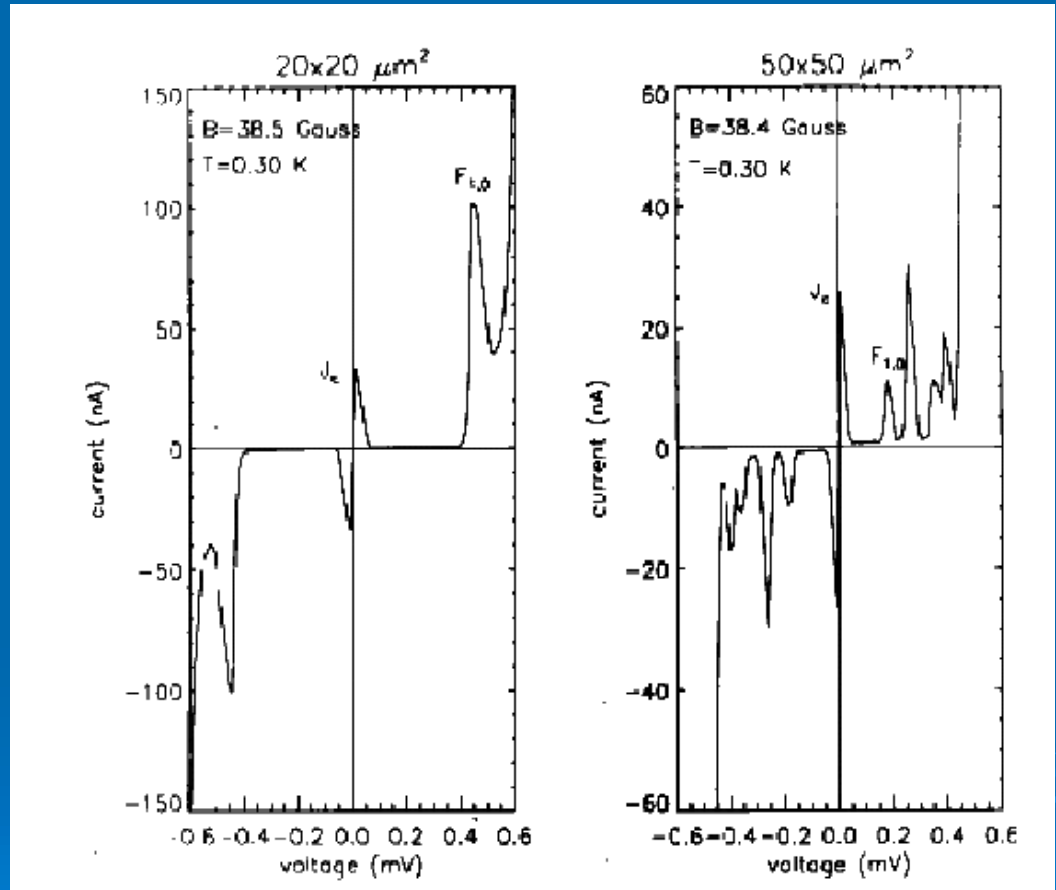
STJ array electronic characteristics

- Pixel size (typical) 50 x 50 mm^2
- Pixel size (range) 20 x 20 - 50 x 50 mm^2
- Pixel capacitance (typical) 0.09 pF/μm^2
- Wiring capacitance to ground 100 pF
- Cross wire capacitance between pixels 80 pF
- Signal rise time (typical) 0.1 μs
- Signal decay time 5 - 40 μs
- Range of bias currents 0.1 - 2 nA
- Maximum residual current 100 nA
- Photon energy range 0.5 - 10 eV
- Responsivity (gain) 5 x 10^3 to 5 x 10^4 e/eV

System specifications

➢ read-out system shall include the following functions:

➢ Programmable biasing and bias measurement of STJ detectors;

➢ Charge Sensitive Amplifier (CSA);

➢ Anti-Aliasing Filter (AAF);

➢ Low Level Discriminator (LLD) with programmable detection threshold;

➢ Sample and hold (S/H), Multiplexing (MUX) and Analogue to Digital Conversion (ADC);

➢ Continuous buffering of digital samples;

➢ Event detection and datation, transmission of qualified samples;

➢ Digital filtering and parameter extraction, performed with software in a Digital Signal Processor (DSP);

➢ Provisions for post-processing of extracted parameters;

➢ Personal Computer (PC) interface for data acquisition and control of parameters such as biasing, gain settings etc.

ASIC features

VA64SARA

➢ 64 input channels

➢ 4 dummy channels for stabilization

➢ 64 10 bit DACs for input offset adjutments

➢ 64 outputs with drivers

➢ Selectable test channel

➢ Selectable feedback for + and – input charge

➢ Leakage current compensation for both polarities (input bias servo with threshold)

TA64SARA

➢ 64 input channels

➢ 1 common trigger out

➢ 12 address outputs

➢ Selectable trigger polarity

➢ External common threshold

➢ 3 bit individual channel threshold adjutment.
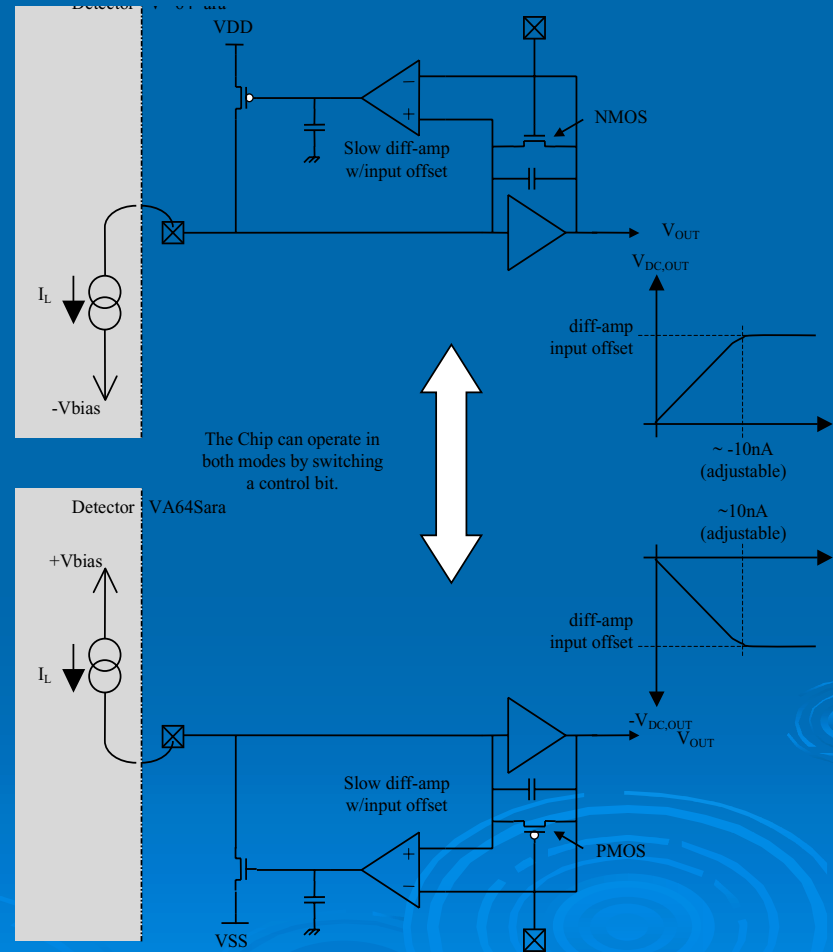
Va64SARA architecture
1 channel

short   calibrate   RegIn

10 bit DAC
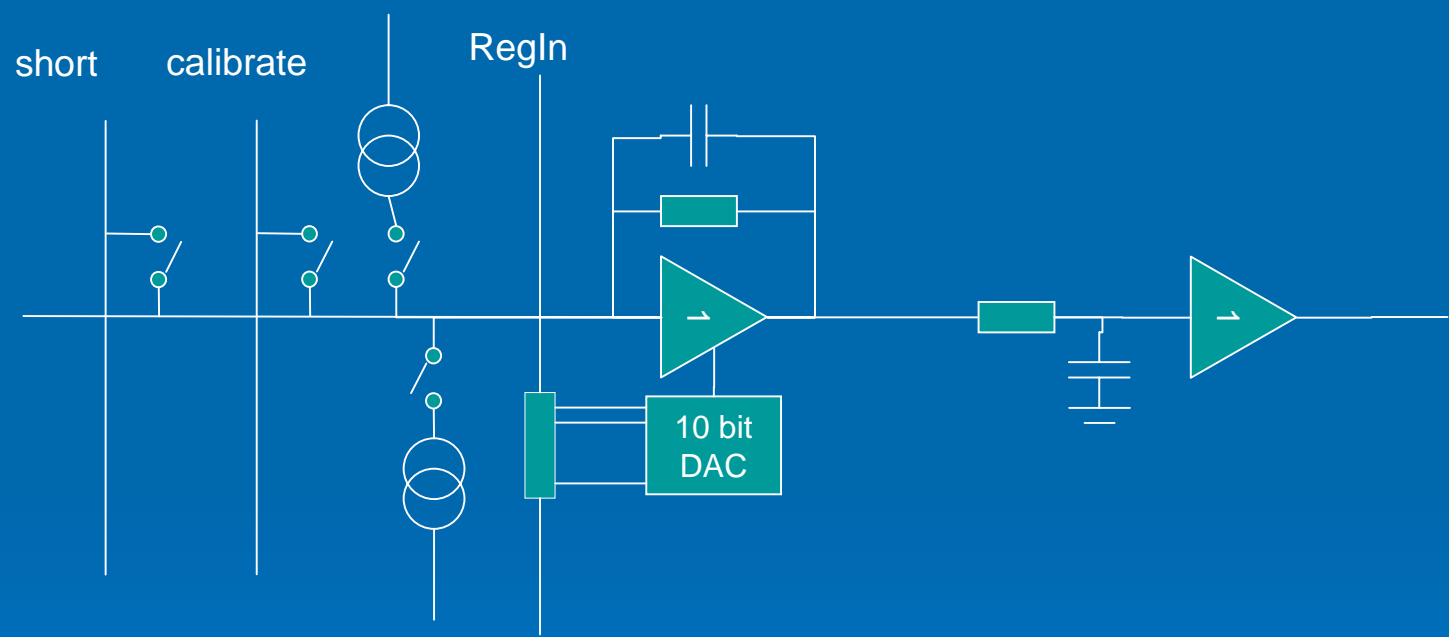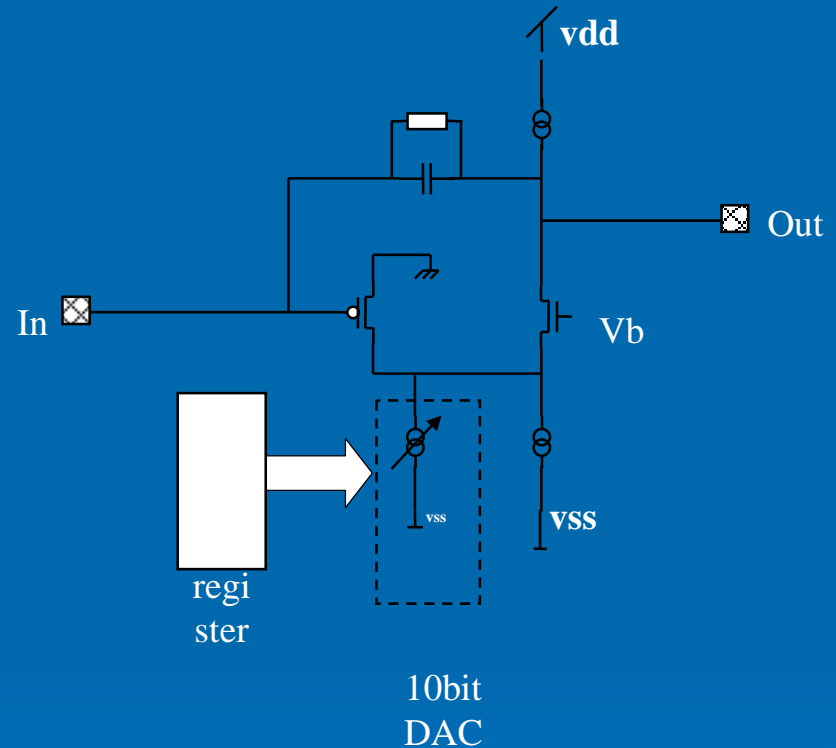
VA64SARA architecture Complete chip
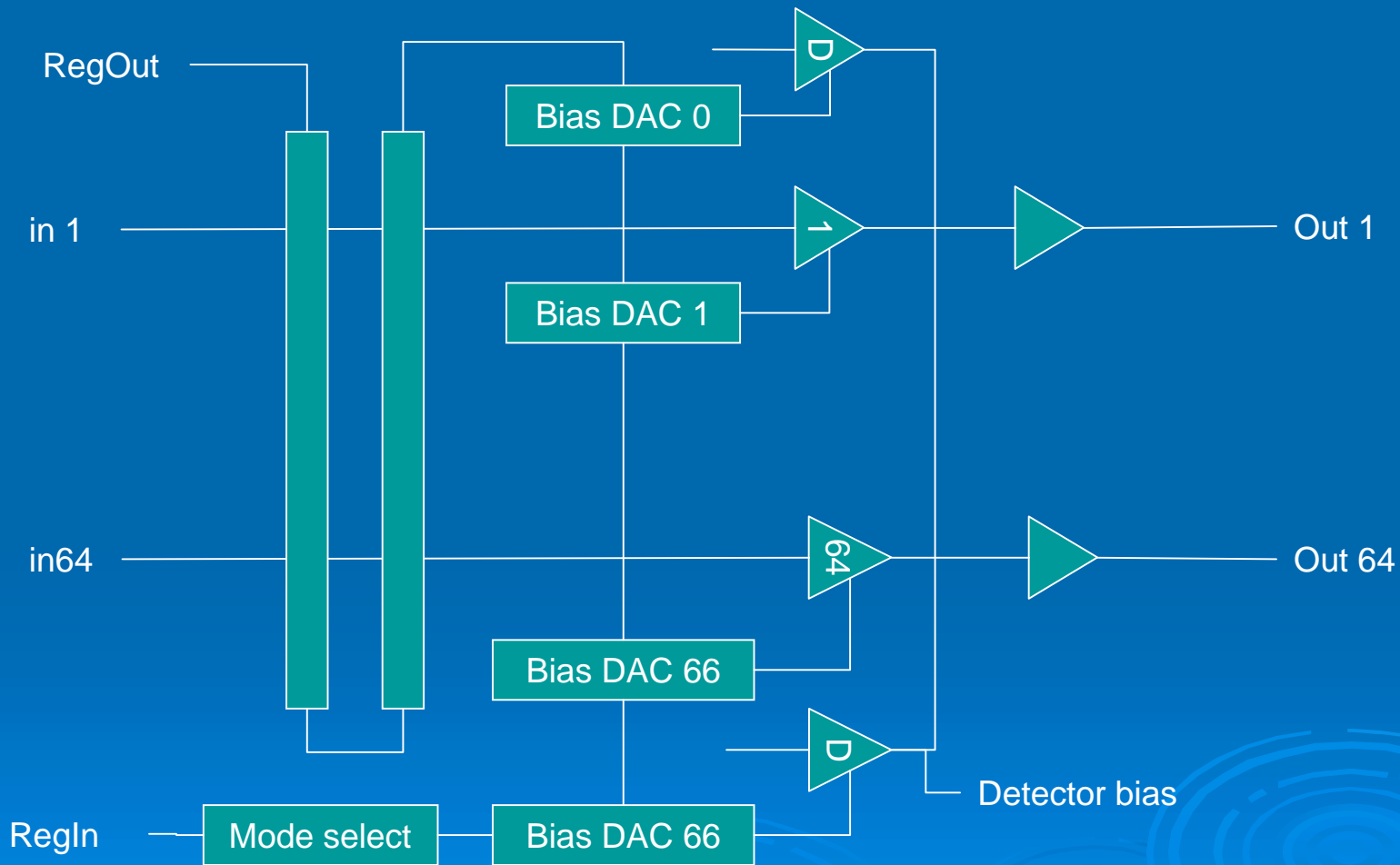
VA64SARA
Leakage current compensation

- Turns on only after exceeding of threshold
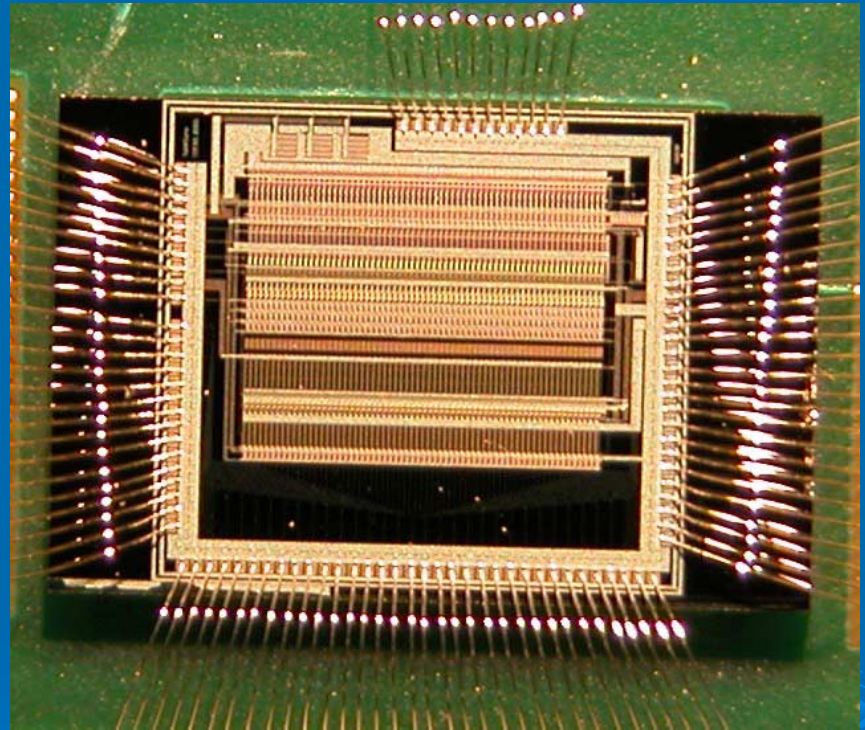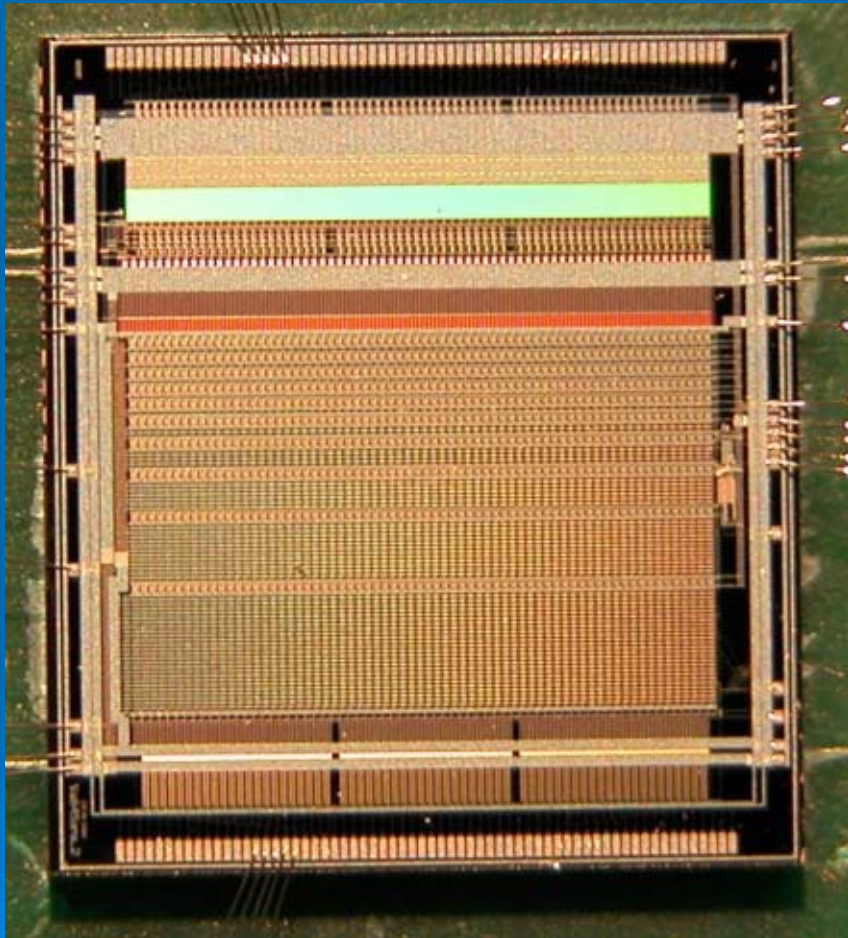- Bi-directional (handles both current polarities)
- Stable up to 10nA

ASIC implementation

- Folded cascode charge-sensitive preamplifier
- Low noise, low power
- Implemented in 0.8μm CMOS process
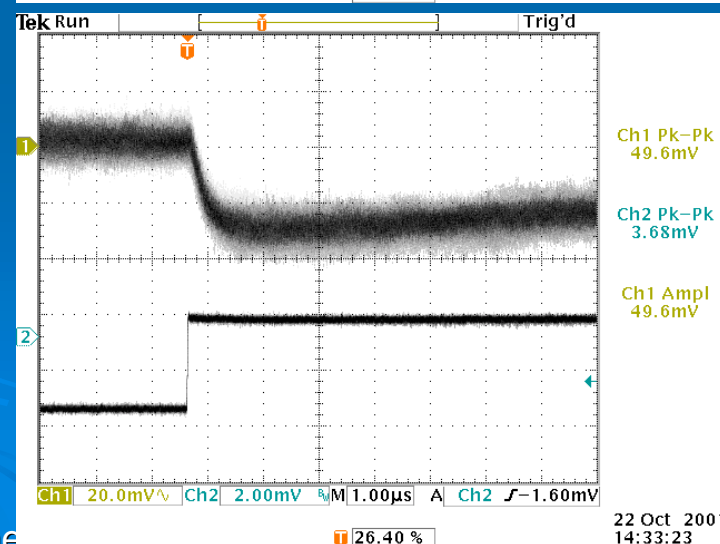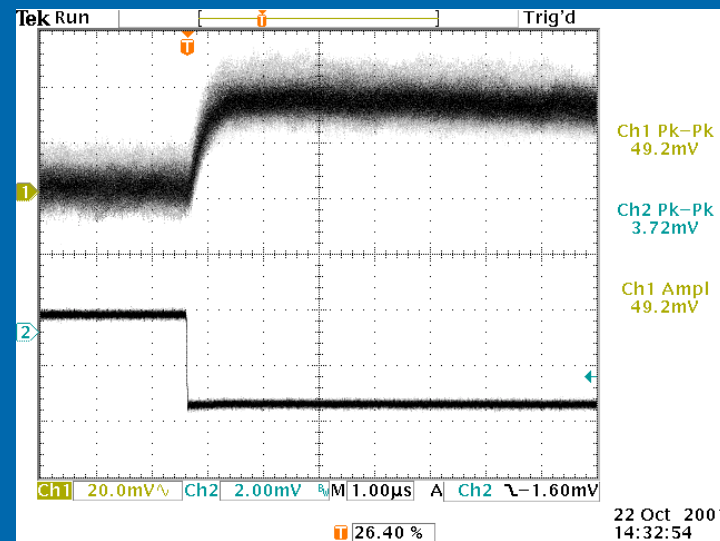- AMS Austria

Final chips

![ideas logo]

Above: TA64SARA
Left: VA64SARA

# Asic performance 1: Gain & noise

> Preamplifier response to 6.6fC input charge

> Measured gain:

-13.5mV/fC for negative charge
13.4mV/fC for positive charge

ASIC performance 2
Noise with digital filtering

➢ A digital filter was implemented in LabView

➢ Gain with shaper was measured to ±1.5mV/fC with no input load and 1.2mV/fC with 330pF input load

➢ Standard deviation w.o. Input signal was measured to 0.06mV and 0.23mV respectively

➢ Equivalent noise charge of 250e+2.9e/pF
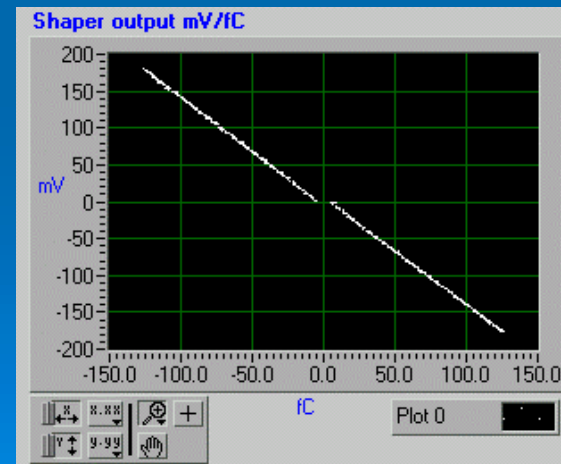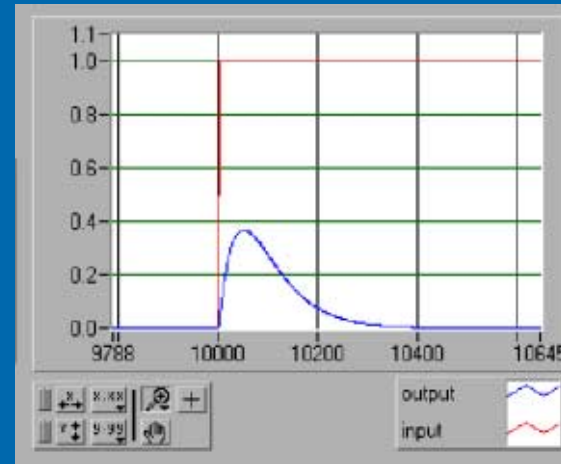
ASIC performance 3: stability
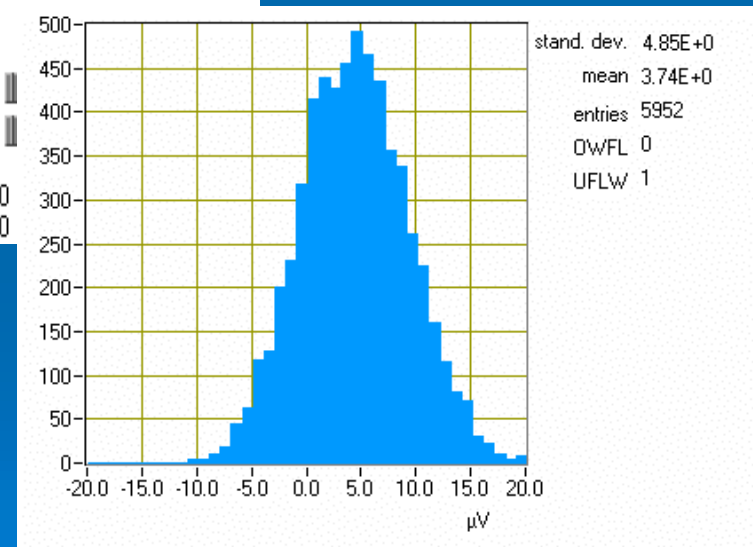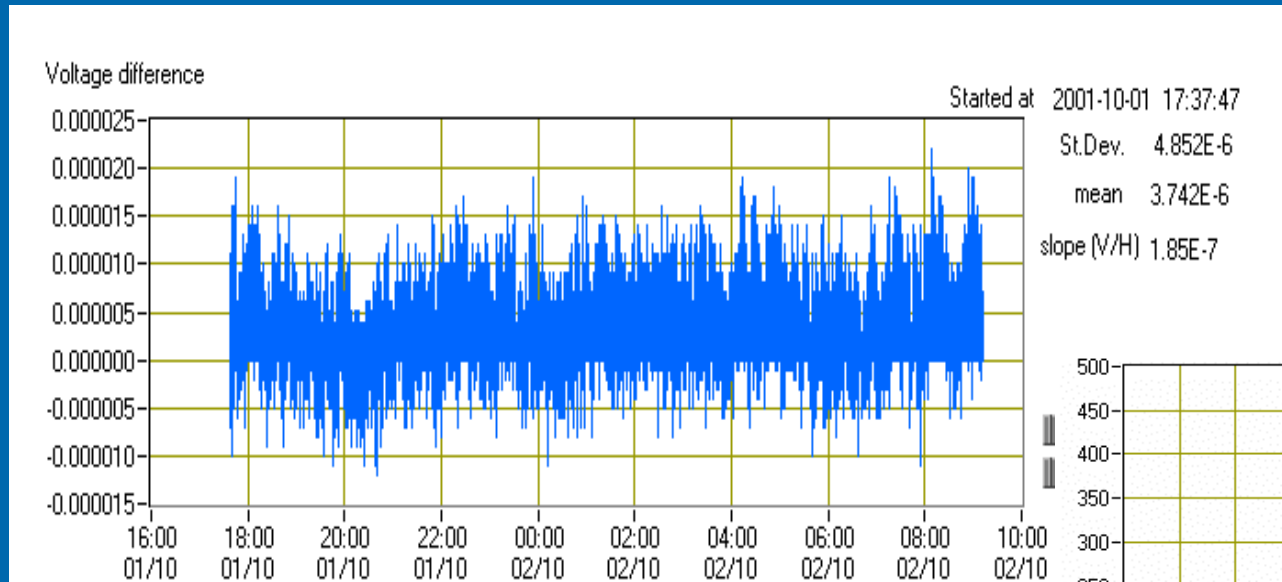
➤ St.dev. Of input bias measured to be <5µV over a 15 hour periode.

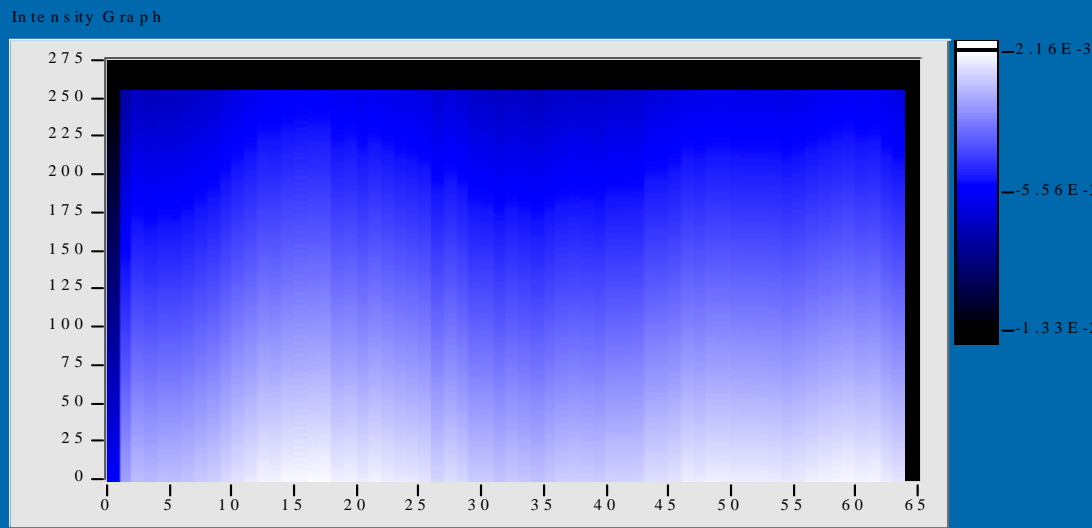# ASIC performance 4: DAC

- ➢ Simple current DAC
- ➢ DAC range adjustable using external current
- ➢ Problems with linearity and channel-to channel variation. Process and design limited
- ➢ DAC performance may be improved in future versions

DAC_bias (µV)	Full range (mV)	Resolution (range/1024)(µV)
10	3.8	3.75
50	7.8	7.63
100	14.9	14.6

VA64SARA DAC
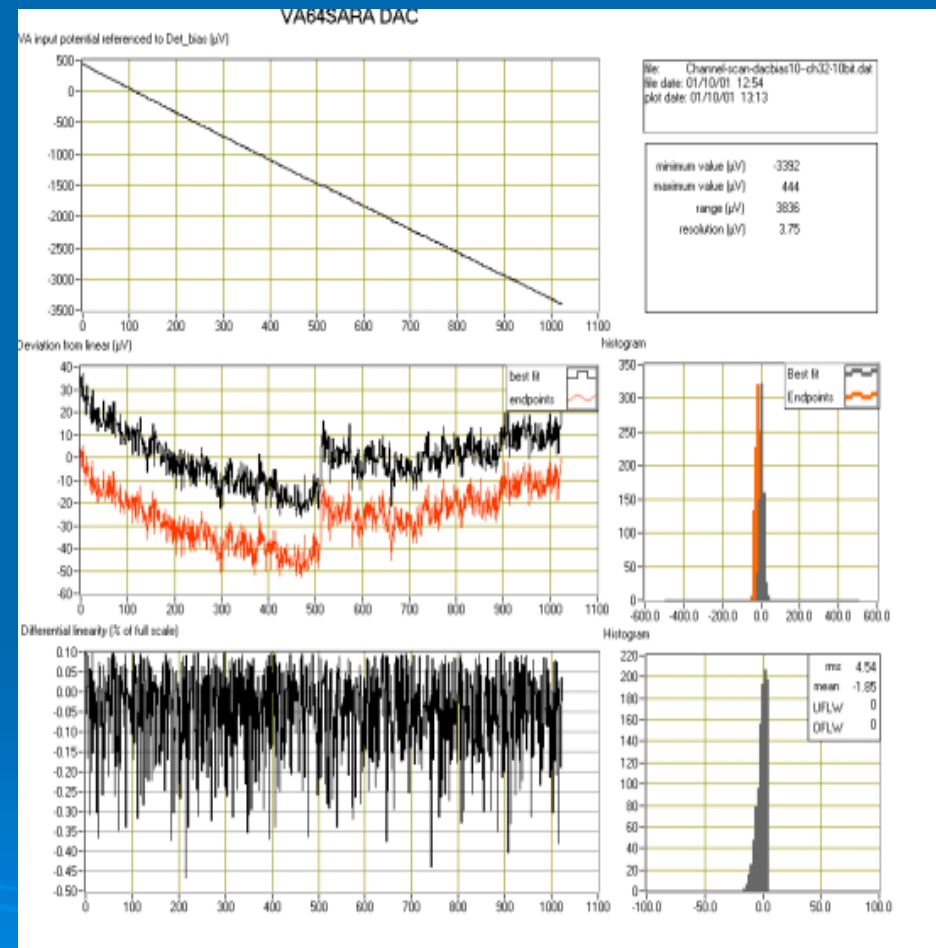
ASIC performance 5: DAC

Intensity Graph

> Map of voltage differentials measured for 256 DAC values spanning the range 0-511 which is half of the full range. Horizontal axis is channel number.

> Residuals due to geometry or process variations across the chip

ASIC performance 6: input bias results

➢ It turned out not to be possible to get all channels in one chip within specifications

➢ One chip set was added to the system and it was decided to select 128 best channels from the 196 available.

Offset distribution

R/O system architecture

Front-end card

Fast trigger

cPCI crate

12 address lines

Patch panel

VA64SARA

VA64SARA

VA64SARA

Patch panel

TA64SARA

TA64SARA

64 →16 multiplexer

16 ADC

12 DSPs AD SHARC

Pentium PC

DACs & Power

64 analogue lines

Desktop PC

Digital control

Ideas developed

COTS
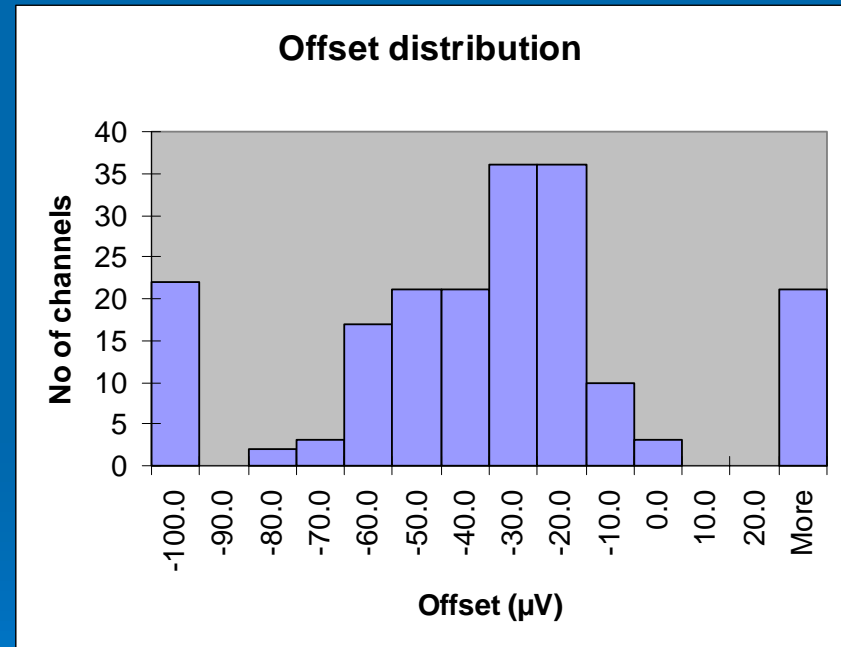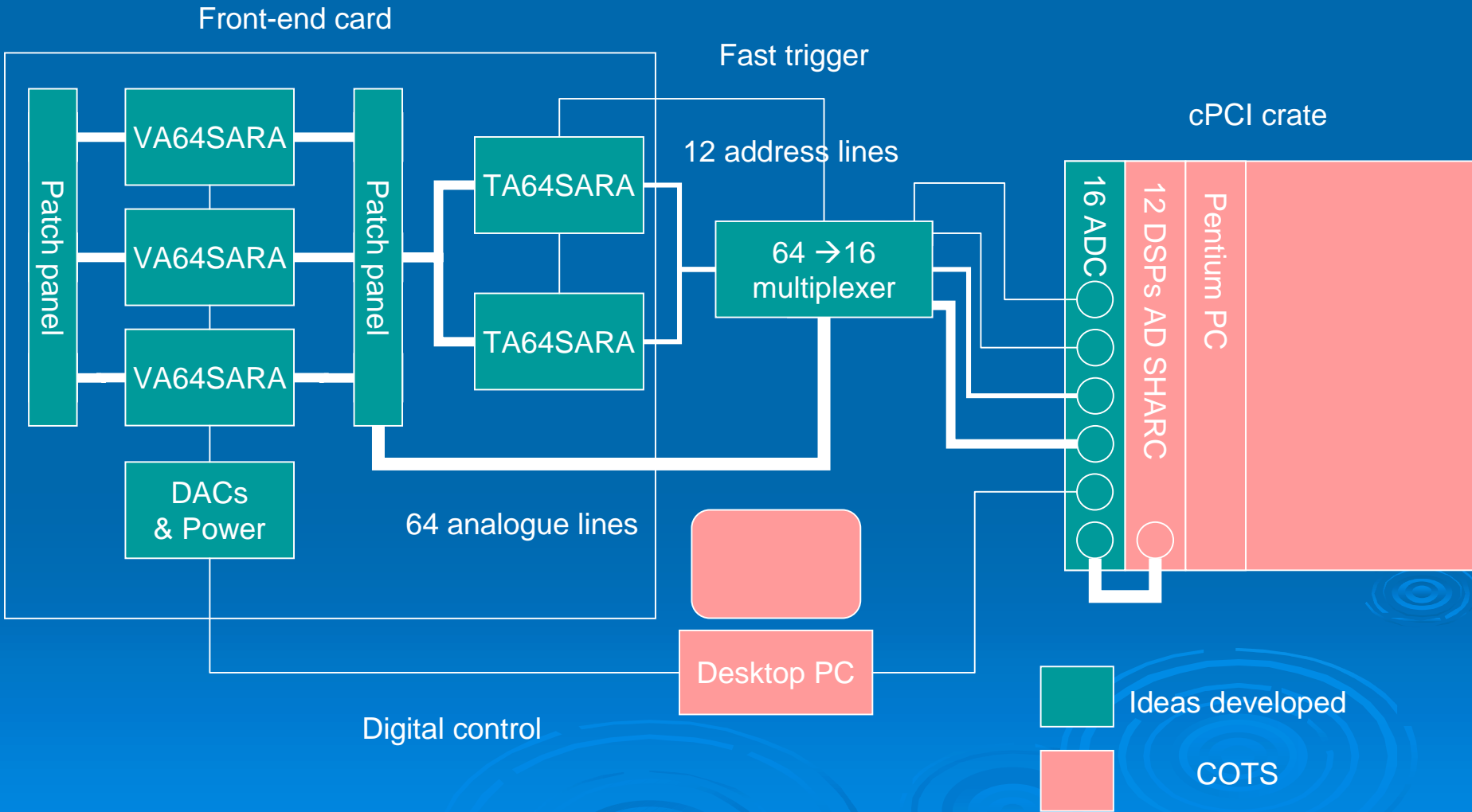
R/O system implementation Front-end cards

- ➢ 1 VA motherboard with 3 ASICS
- ➢ 1 TA motherboard

  with 2 ASIC
- ➢ Each in separate shielded enclosure with cable interconnects
- ➢ Very high stability power supply
- ➢ Controlled turn-on
- ➢ DACs for ASIC biasing

R/O system implemetation Analogue multiplexer card

- 128 analogue inputs
- 16 analogue buffered outputs
- 20MHz switching frequency
- Isolation between analogue and digital part
- Address line buffering
- Multi-trigger rejection

R/O system implementation ADC card

- 16 transformer isolated inputs
- 12 address line inputs
- 1 fast trigger input
- 16 20MHz ADCs
- 640MByte/s data rate
- 0 suppression and event formatting in FPGA
- Serial data outputs for DMA into multi-DSP card
- Subcontracted to Mikrokrets AS, Oslo (www.mikrokrets.no)
- cPCI form factor.

Conclusions

➢ A chip set has been designed, produced and tested which can be used for reading out large STJ arrays. This has never been done before.

➢ The front-end combines variable input biasing with exceptionally low noise under large capacitive loads

➢ An accompanying data aquisision and control system has been developed.

➢ Problem areas has been identified and a road-map to further development can be made.

➢ Future developments pending further requests from ESA

Future possibilities

➢ Smaller feature sizes leads to higher transconductances

➢ biCMOS process for high speed devices

➢ Recent results:

- CMOS 0.8µm:<200e noise at 80ns shaping time. Device made for medical applications
- biCMOS 300e at 20ns shaping time also lower power
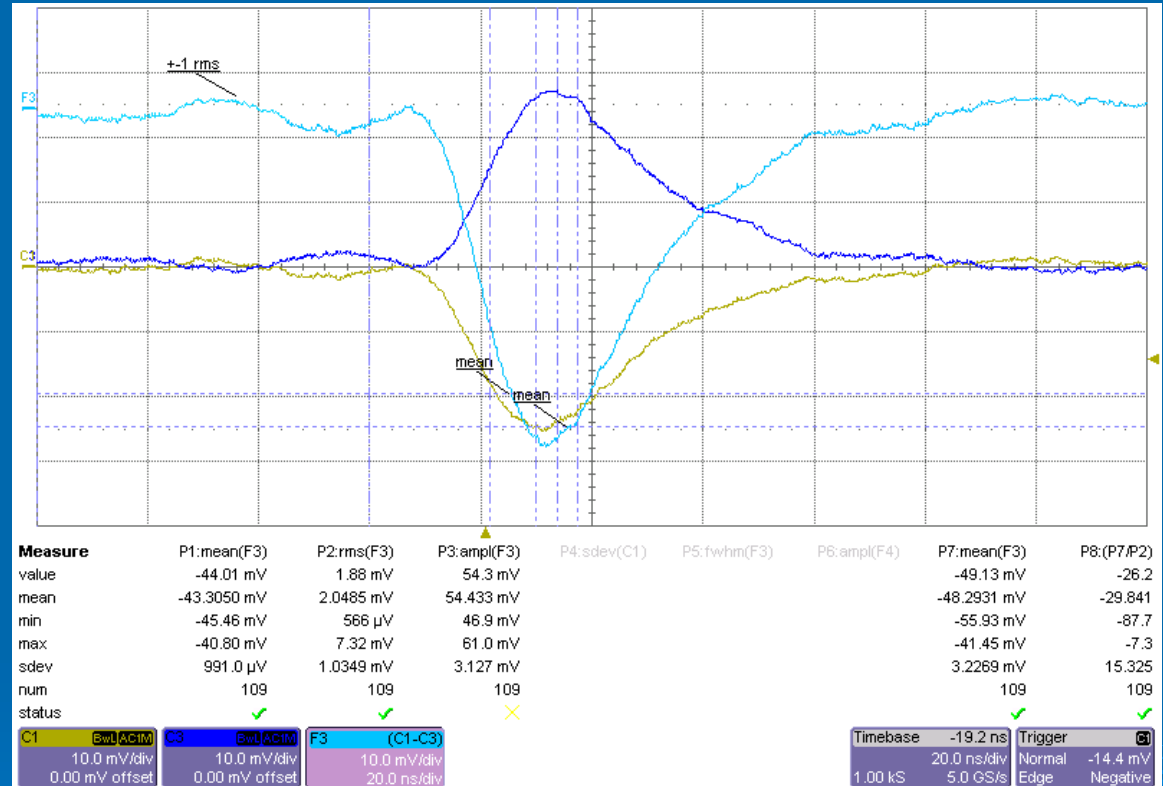- CMOS 0.35µm 40e+10e/pF 200µW/channel rad hard to >10MRAD

CMOS 0.8μm

- test device
- About 6mW/channel
- 1fC test pulse
- S/N 35:
- →<200e noise
- Shaping time 80ns
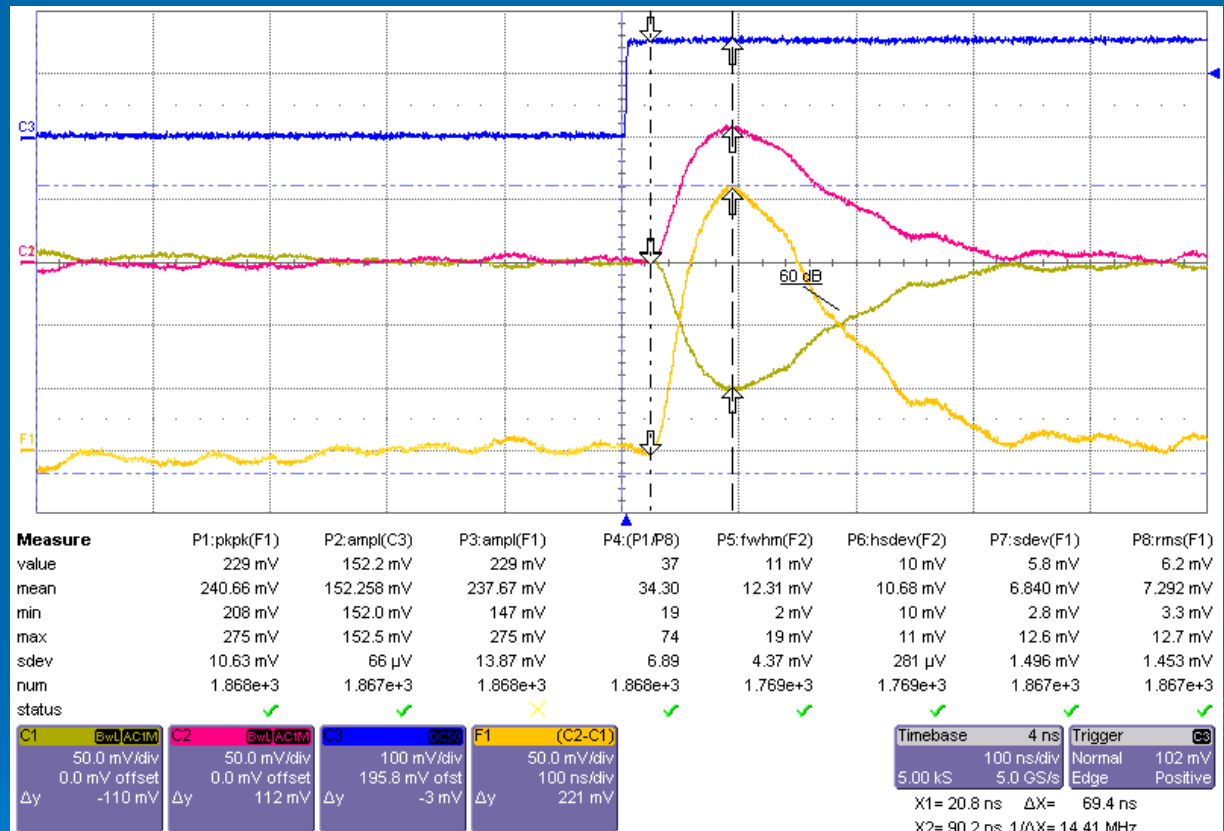
BiCMOS

- Test device
- Bipolar input transistor
- About 200µW power/channel
- 2fC test pulse:
  - S/N 30
  - → ENC 400e

CMOS 0.35µm

- 32 channel preamplifier and trigger chip
- Serial readout of analogue signal
- Fast trigger output
- 4µs peaking time
- 40e noise @ 4µs
- 200µW/channel