T@MPO

Turbocoding at Minimum Power

ESTEC Contract nr 1378199/NL/FM

ESA MPD, Feb 5th, 2004

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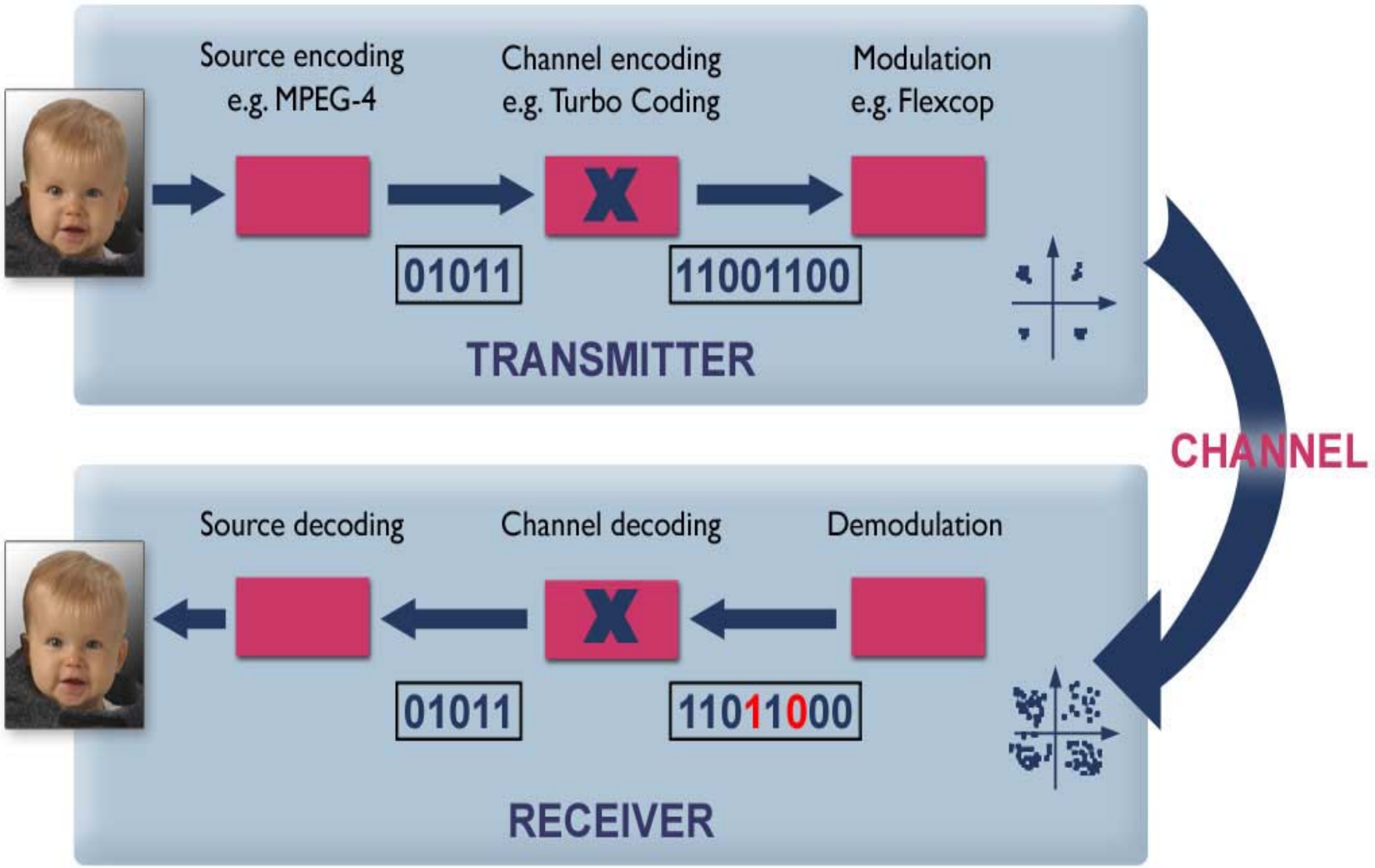
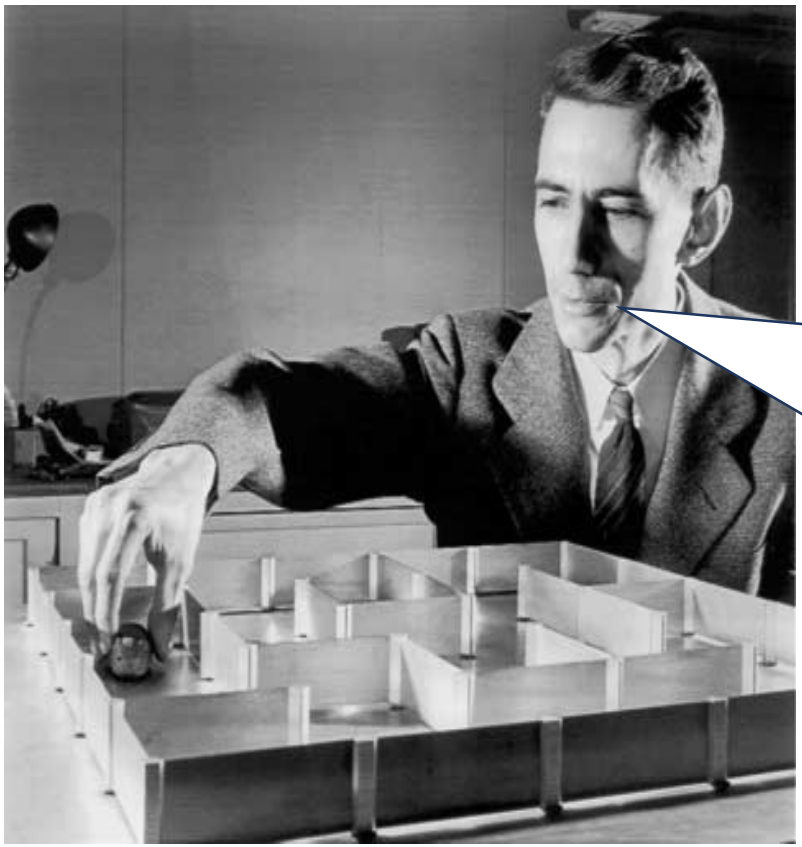
on behalf of the T@MPO-team

SEEDS FOR TOMORROW'S WORLD

Transmission errors can be corrected using channel coding



Channel coding: towards the limit



There is a limit to the transmission rate of reliable data over an unreliable channel

Claude Shannon
1948

The efficiency of forward error correcting codes is ever increasing

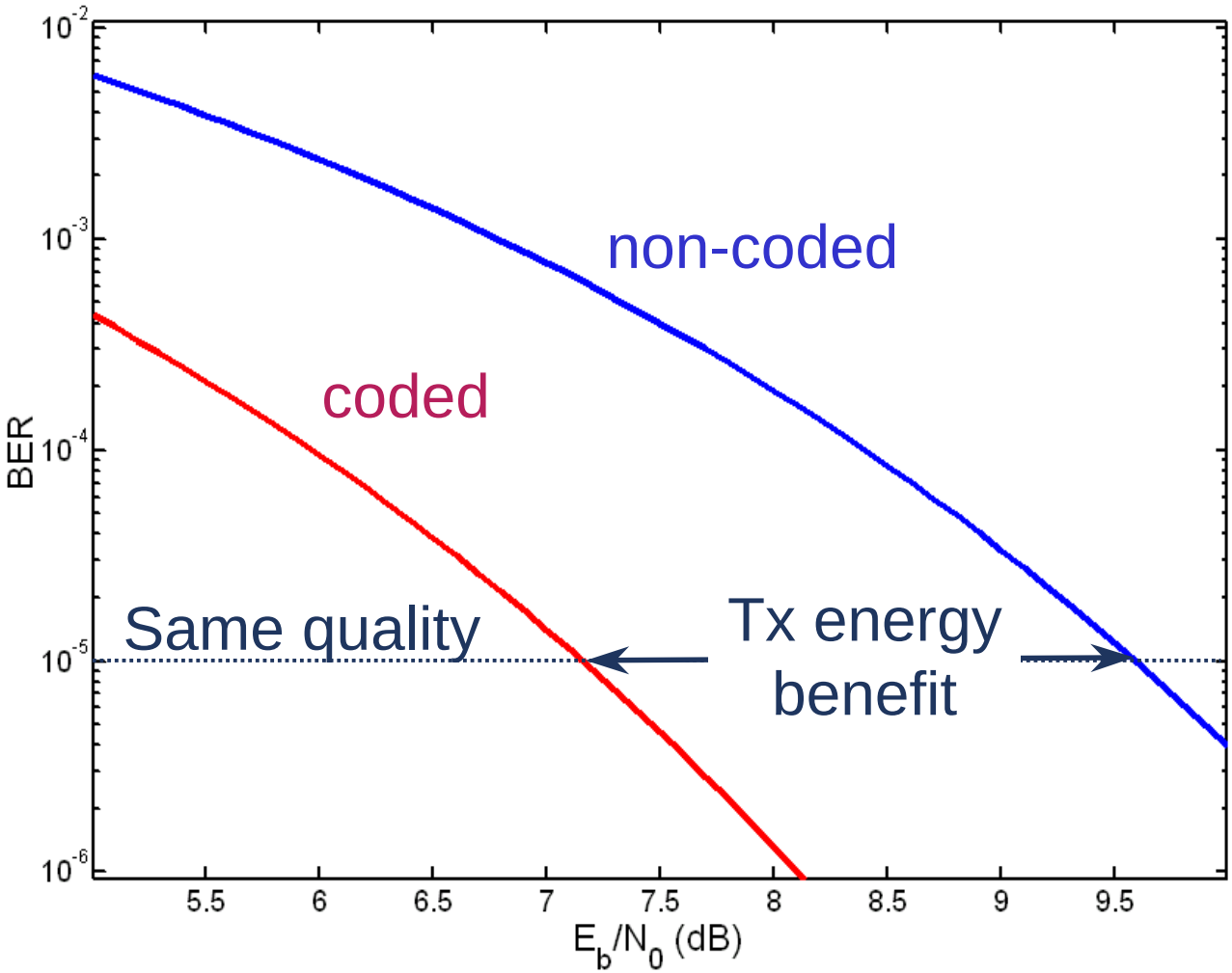
Classic existing forward error correcting codes

- Reed-solomon
- Convolutional codes

More powerful codes gain interest

- Turbo codes
- LDPC codes

Channel coding modifies the power budget distribution



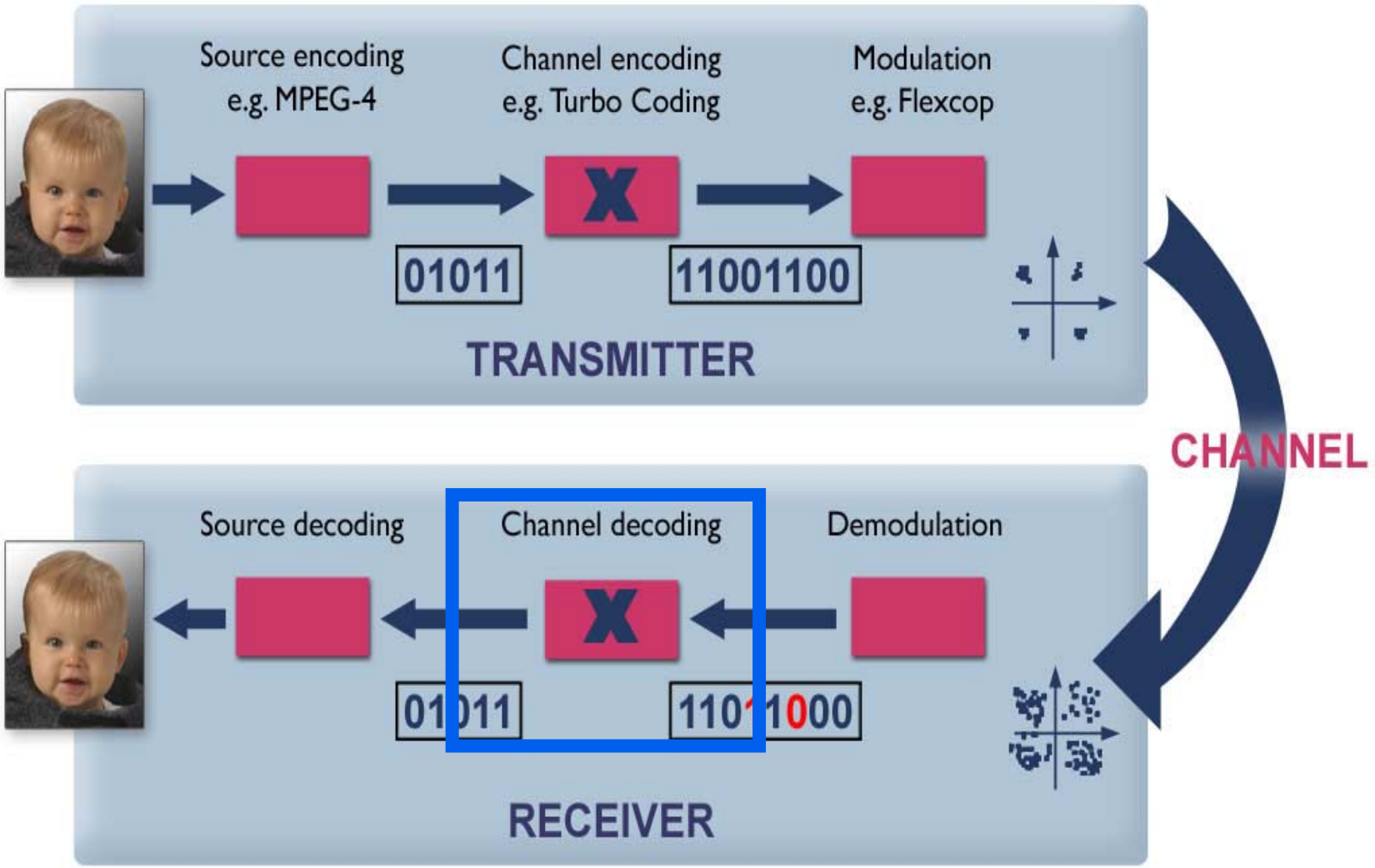
↓ front-end consumption ↑ base-band consumption

Turbocoding allows approaching Shannon's limit

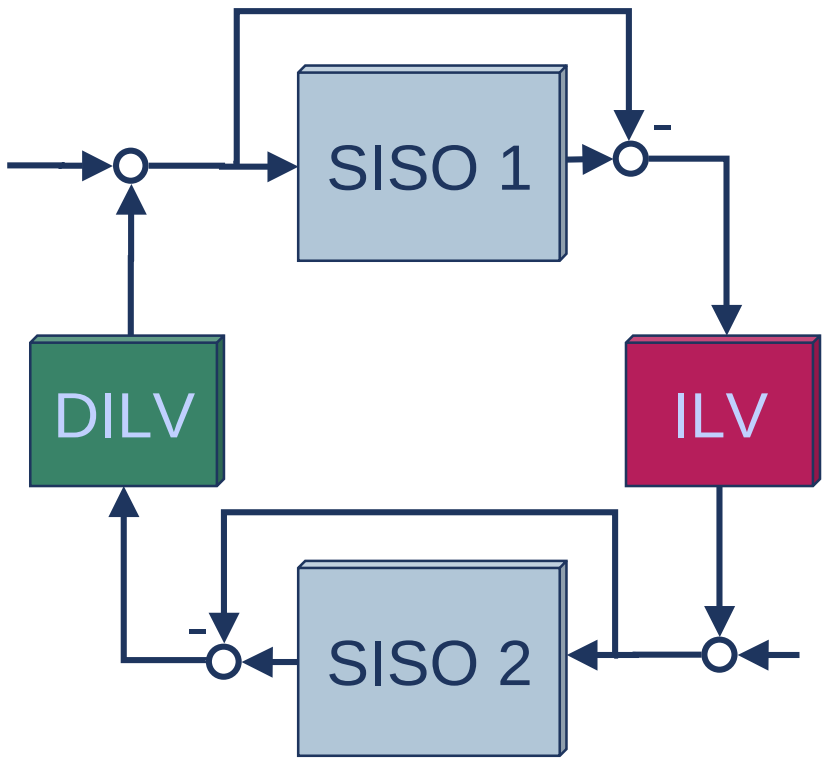
The obtained coding gain can be used to:

- Reduce the power consumption in the RF blocks
- Transmit a higher modulation over the same system (increase throughput)
- Increase the operating range of the system

Turbocoding uses an innovative decoder architecture



Iterative decoding is the key



The decoding

- requires a whole block
- is iterative
  - → high latency
  - → low throughput
- is data intensive
- is complex (SISO)
  - → high power consumption
  - → high cost (Si area)

We applied IMEC's design methodology to turbo coding

This allows making an ASIC that implements the complex decoding algorithm

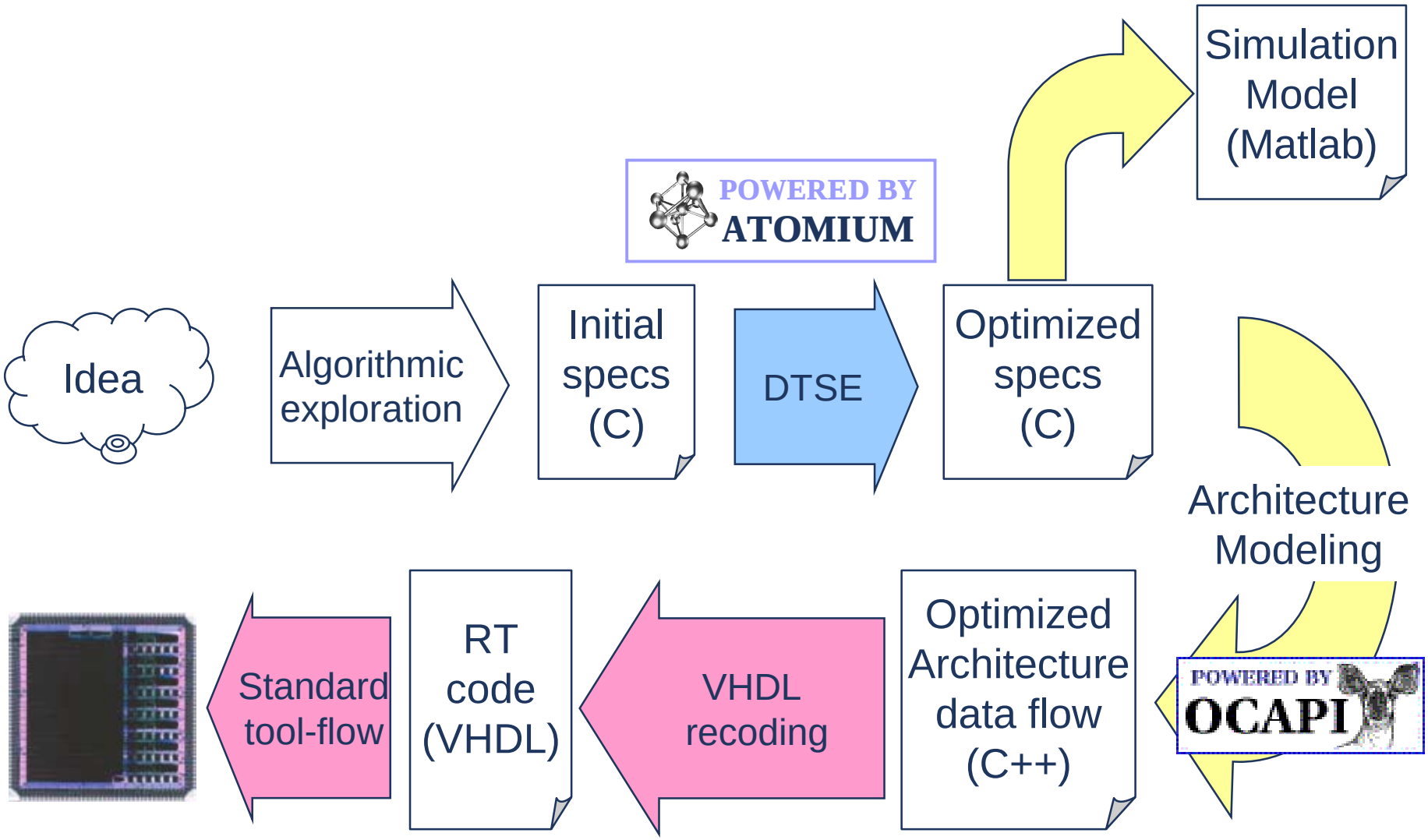
- At high speed (high throughput)
- At low power
- With low latency
- While maintaining high performance

Project goal: a state of the art codec

T@MPO	Others
■ Flexible PCCC	■ TPC
■ Up to 80 Mbit/s	■ 36 Mbit/s (155 Mbit/s)
■ Low latency (< 10 µs)	■ High latency
■ Low power (< 10 nJ/bit)	■ No info available

Designing T@MPO was quite a challenge

Our structured flow speeds up the design process



Both algorithm and hardware have been optimized

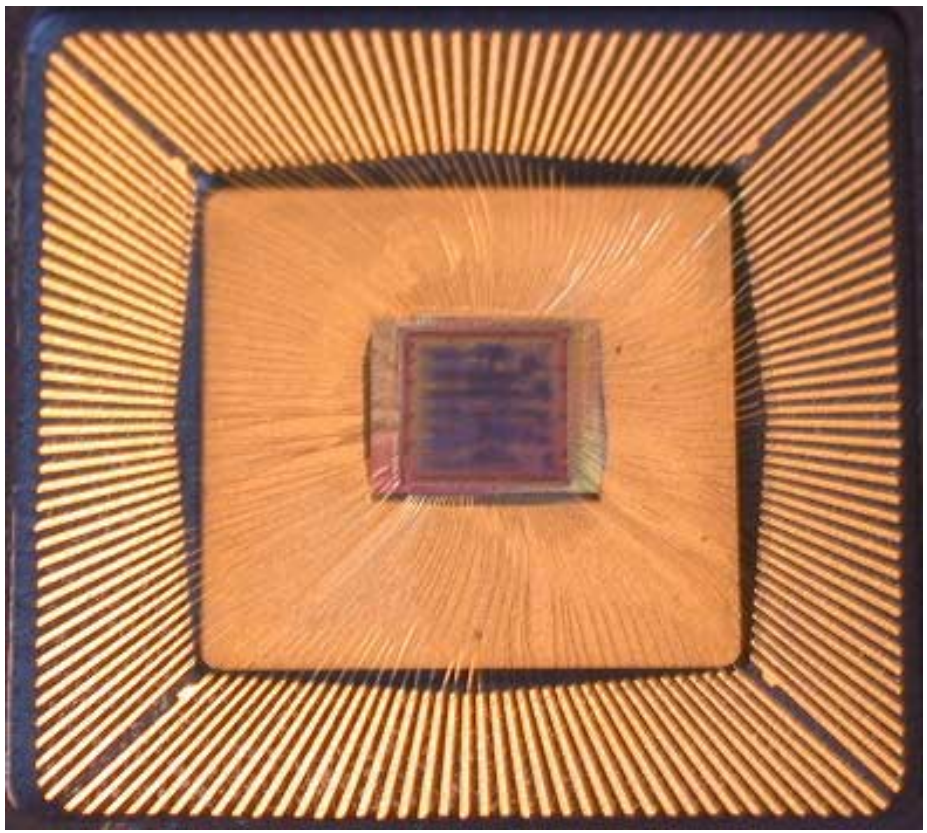
Maximal throughput is obtained through:

- optimized collision-free interleaver units
- 7 parallel worker units
- interleaved decoding process

Minimal power consumption through:

- a separate gated clock for every worker
- optimized memory hierarchy
- early stop criterion

The T@MPO is implemented in .18 CMOS

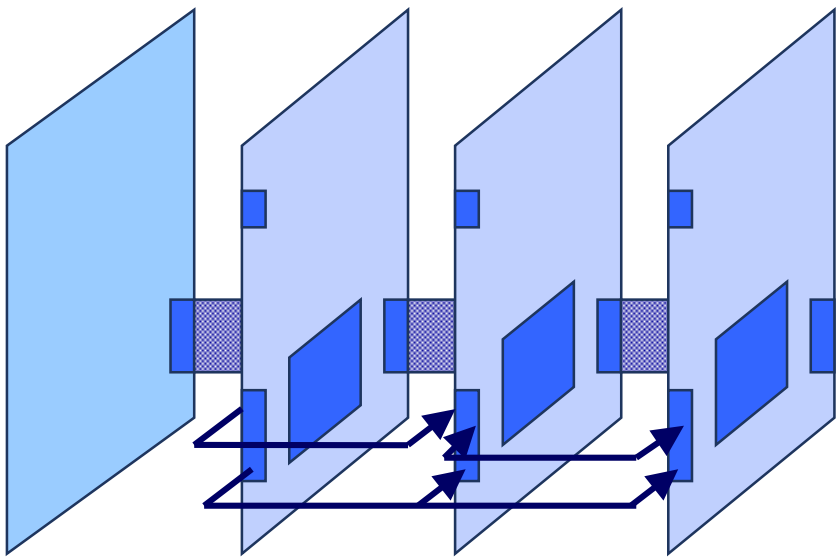


- 400 k gates
- 7 mm^2
- 36 kBit RAM
- on-chip PLL

The PICARD system allows for real-time evaluation

The test setup is based on a generic platform

- Modular system based on standard pc
- Add-in board houses the T@MPO
- Software library gives access to the board over the PCI bus
- Standard C software used to assess the performance



T@MPO provides minimal latency and high throughput

The decoder has a fixed latency for all block sizes

5.7 µs @ 6 iterations

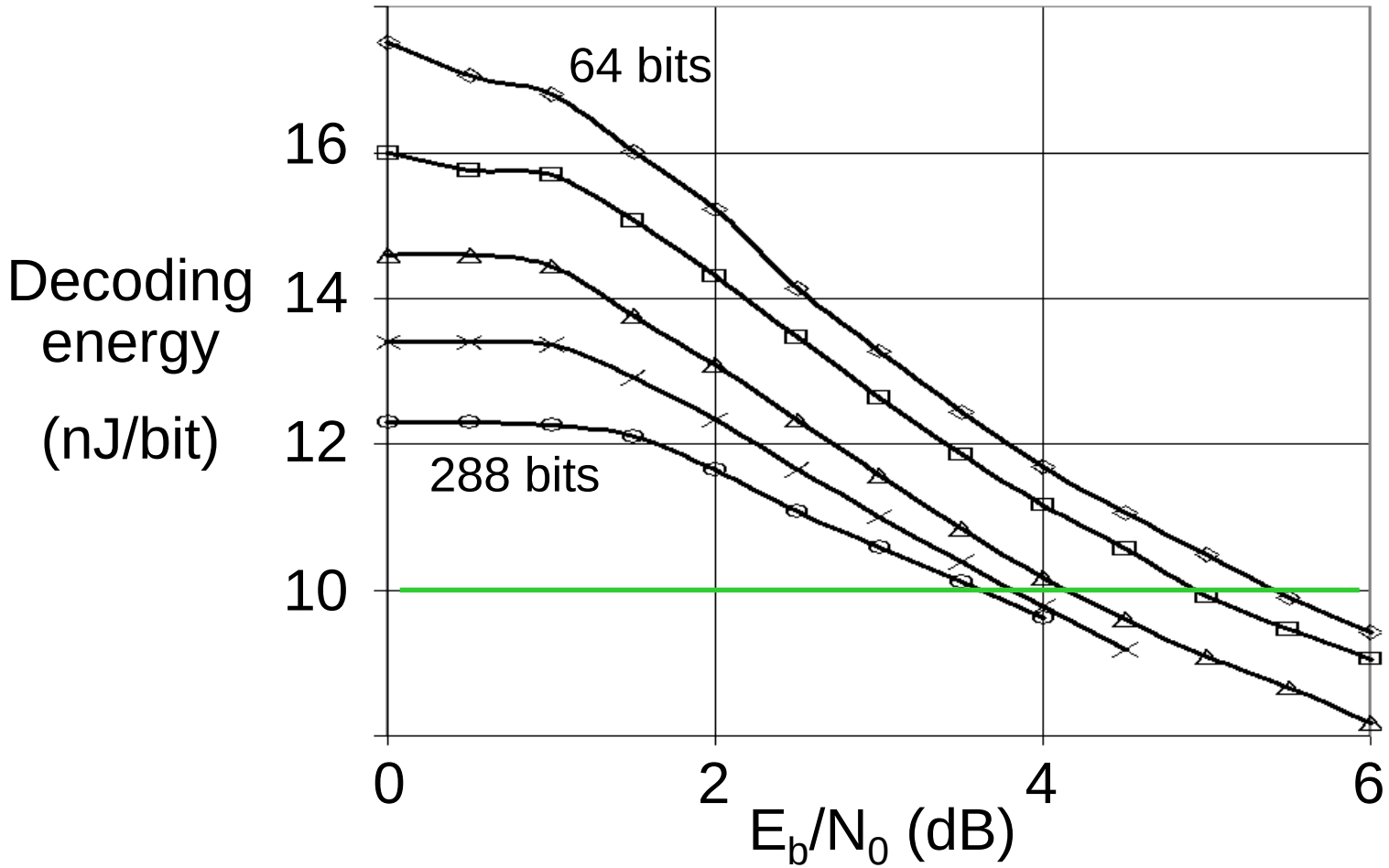
The throughput, at 40 MHz clock, is maximum

76 Mbit/s

code rate	block length	throughput, calculated (Mbit/s)	throughput, measured (Mbit/s)
1/3	32	6.0	6.0
1/2	96	17.9	17.9
2/3	256	47.8	47.8
3/4	432	75.6	75.8

Decoding energy is less than 10 nJ/bit

As the number of iterations decreases, the energy consumption drops.



Performance measurements match the dataflow simulations

Full tests have been performed for

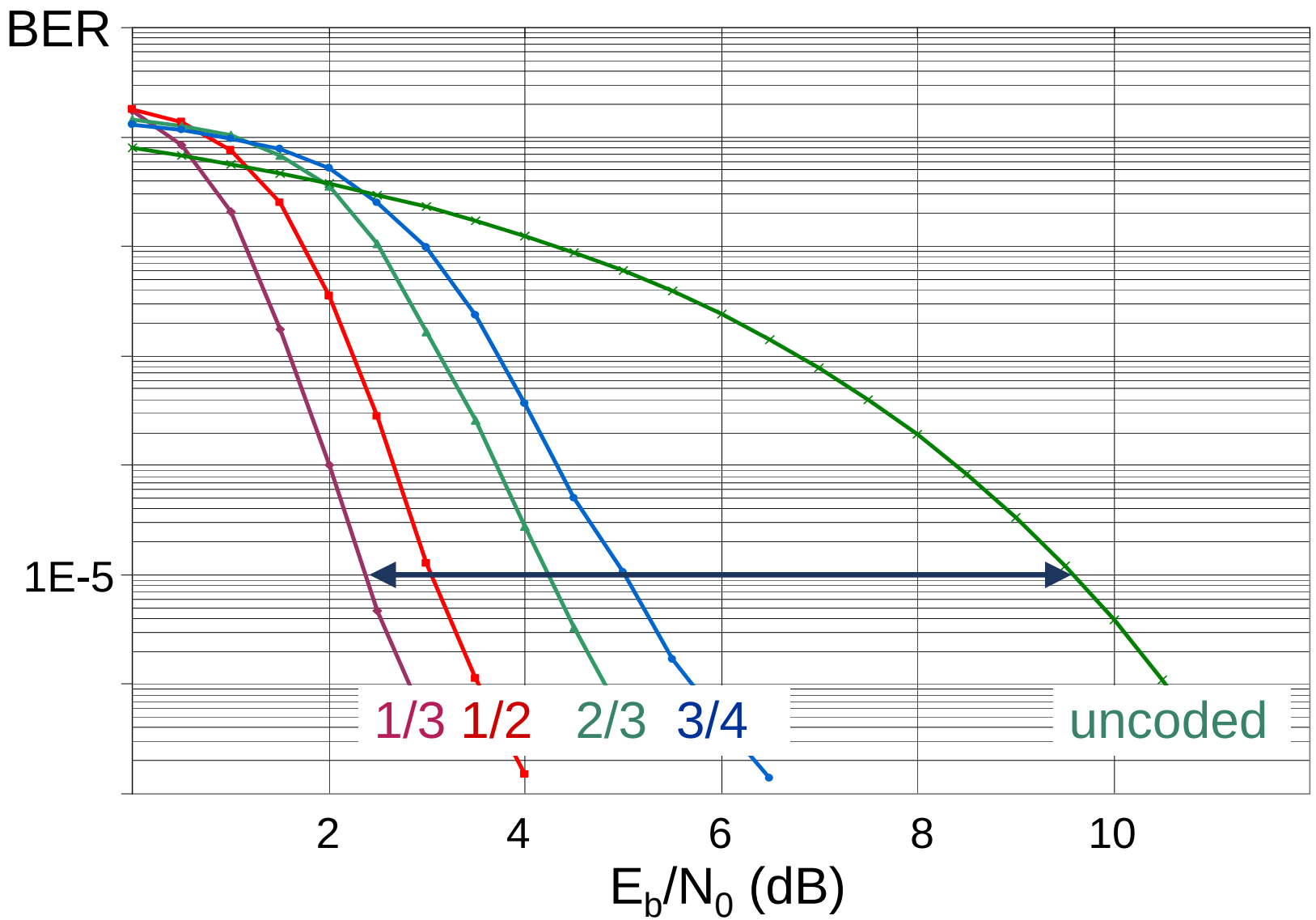
- all supported code rates and block lengths
- all modulations (BPSK, QPSK, QAM16, QAM64)

Supported code rates: 1/3, 1/2, 2/3 and 3/4

12 supported block lengths between 32 and 432 bits

On-the-fly configuration of the working mode is possible

Coding gain at BER 10^{-5} ranges from 4.5 to 7 dB for QPSK



ESTEC contract nr 13781/99/NL/FM

T@MPO performs well compared to other turbocoders

Coder	**T@mpo**	**Bell Labs**	**KAIST**	
Throughput	76	24	5.5	Mbps
Clock speed	160	145	?	MHz
Latency	5.4	?	?	us
Power	1.6	10	7	nj/bit/it
Cost (area)	7	14.5	?	mm2

Tempo performs better in throughput, latency, power consumption and area!

All design goals are met

With our methodology, we obtain

- High throughput
- Low latency
- Low power

- Expected performance for most operation modes

In our first-time right T@MPO ASIC

Live demo!

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