SpaceWire Router

Microelectronics Presentation Days

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Outline

- Introduction
- Motivation
- Router Description
- Router Functionality
- Tools
- Project Description
- Project Schedule
Introduction

SpaceWire

- SpW is a standard for high-speed data handling
- SpW is based on two existing commercial standards, IEEE-1355 and LVDS
- SpW is developed for use in space applications
- SpW Networks consists of links, nodes and packet switching routers
- Interconnected through bi-directional point-to-point high-speed (>100Mbps) digital serial links
Introduction

SpaceWire Network

Additional Links:
- more bandwidth
- more redundancy

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Motivation

Situation:
- SpaceWire standard is becoming increasingly important
- SpaceWire developed for space missions
- A large number of modules need to be interconnected

SpaceWire Router Goals:
- sufficient input / output ports
- compliant to the latest SpaceWire standard
- radiation tolerant
Router Description

SpaceWire Routing Switches

- Link Interfaces connected via a routing matrix
- SpaceWire packet:

  | Destination | Cargo | End of Packet Marker |
  | Header      | Data  |

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Router Functionality

Addressing Packets

• **path addressing**
  - direct specification of the path through a network
  - leading character of a packet gives the output port number of the router
  - leading character is removed after output port is determined
  - passing through several routers is done by multiple destination characters

• **logical addressing**
  - indirect specification of the path through a network
  - usage of routing tables in the router
  - leading character gives logical address
  - leading character is not removed
Router Functionality

Routing Table

- holds the logical-physical mapping

Example (4Port Router):

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Address</th>
<th>Port 0</th>
<th>Port 1</th>
<th>Port 2</th>
<th>Port 3</th>
<th>Port 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Addressing</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>Logical Addressing</td>
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<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<tr>
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<td></td>
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<td>0</td>
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<td>0</td>
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</tr>
</tbody>
</table>
Router Functionality

Group Adaptive Routing

- If 2 or more output ports lead to the same destination, they can be configured as a group

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Address</th>
<th>Port 0</th>
<th>Port 1</th>
<th>Port 2</th>
<th>Port 3</th>
<th>Port 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Router Functionality

Group Adaptive Routing

Advantages:

- **Bandwidth sharing**
  - if 2 or more links are organized in a group the data can take either way
  - this leads to twice the bandwidth of a single link

- **Fault Tolerance**
  - if 2 or more links are organized in a group and one link fails, the information can flow via the other links
  - no network management needed
  - automatic and immediate fault recovery
  - only packet which was transmitted when the fault occurred is lost
Router Functionality

Priority Packet Delivery

- if two input ports have to use the same output port, an arbitration scheme is used
- the arbitration scheme can include a priority scheme
- no priority flag available in packet header
- priority scheme is included in routing table assigned to logical addressing
Router ASIC

Features:

- Fully SpaceWire Compliant
- 8 SpaceWire ports
- 2 External ports
- Internal Configuration port
  - accessible through SpaceWire or External ports
  - logical address routing table
  - Control registers
  - status registers
- Time Code interface
  - receiving time-codes
  - generating time-codes
- External pins for status/error monitoring
Router Description

SpaceWire Router (ASIC)

SpaceWire Interfaces

SpaceWire Port 1
SpaceWire Port 2
SpaceWire Port 3
SpaceWire Port 4
SpaceWire Port 5
SpaceWire Port 6
SpaceWire Port 7
SpaceWire Port 8

Control Logic
Routing Table
Status/Error Registers
Control Registers
Configuration Port
Tick Counter

External Input/Output
External Input/Output

Input FIFO
Output FIFO
External Port

Status Outputs

Time-Code Inputs/Outputs

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Router ASIC

**SWR ASIC**
- implemented in an Atmel MH1RT gate array (max 519k Gates)
- package 196 pin ceramic Quad Flat

**Radiation tolerance**
- 0.35μm CMOS process: 300k rad
- SEU free cells up to 100MeV (for critical memory cells)
- latch up immunity up to 100MeV

**Maximum baud-rate:** 200Mbit/s
**Power consumption:** ~4Watt (at max data rate)
**Single supply voltage:** 3.3V
SpW CODEC

SpaceWire CODEC
- Encodes and decodes bit-stream on physical medium, SpaceWire cable.
- Part of the data-link layer for SpaceWire systems to communicate
- Implemented in RTL level VHDL code.
- Compliant with ECSS-50-12A SpaceWire standard

Goals
- Technology independent
- High speed operation, Low area footprint
- Configurable to users requirements and target technology
SpW CODEC
SpaceWire Monitor

- Monitors traffic on a SpaceWire link
- Two banks of LEDs show
  - connection state, Data flow, EOPs / EEP, NULLs, FCTs, Errors
- Logic analyser connections
- Both directions monitored simultaneously
Tools – SpaceWire Monitor

SpaceWire Enabled Equipment → SpaceWire Monitor → SpaceWire Enabled Equipment

Logic Analyser
SpaceWire PCI-2

- Fully SpaceWire compliant
- New SMCS 332SpW FPGA
- Board currently being designed
- Functions as SpaceWire node
Tools – SpaceWire PCI-2 Card

SpaceWire Interfaces

SMCS FPGA

DUAL-PORT MEMORY

PCI INTERFACE

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Teaming: EADS Astrium GmbH (prime)
   University of Dundee (subco)
   Austrian Aerospace GmbH (subco)

Work:
- Router Specification, Design
- FPGA implementation
- Development of Validation Tools
- Validation Exercise
- ASIC Design / Manufacturing
- ASIC Test
Schedule

Project KO: January 2002

Router FPGA: February 2004

Validation Exercise completed: Q3 2004

Router ASIC: Q2 2005