The new SpaceWire compliant SMCS332 / SMCSlite ASIC

Microelectronics Presentation Days

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Outline

- Introduction
- Motivation
- New SMCS332SpW
  - New Features / Functions
- New SMCS116SpW
  - New Features / Functions
- Project Team
- Planned Schedule

Introduction

SMCS (Scalable Multi-channel Communication Sub-system)

- communication controller ASIC
- for space applications (radiation tolerant)

Tasks:

- hardware supported execution of major parts of the inter-processor protocol
- provide a fast interface to serial protocol

Introduction

SMCS332/TSS901E

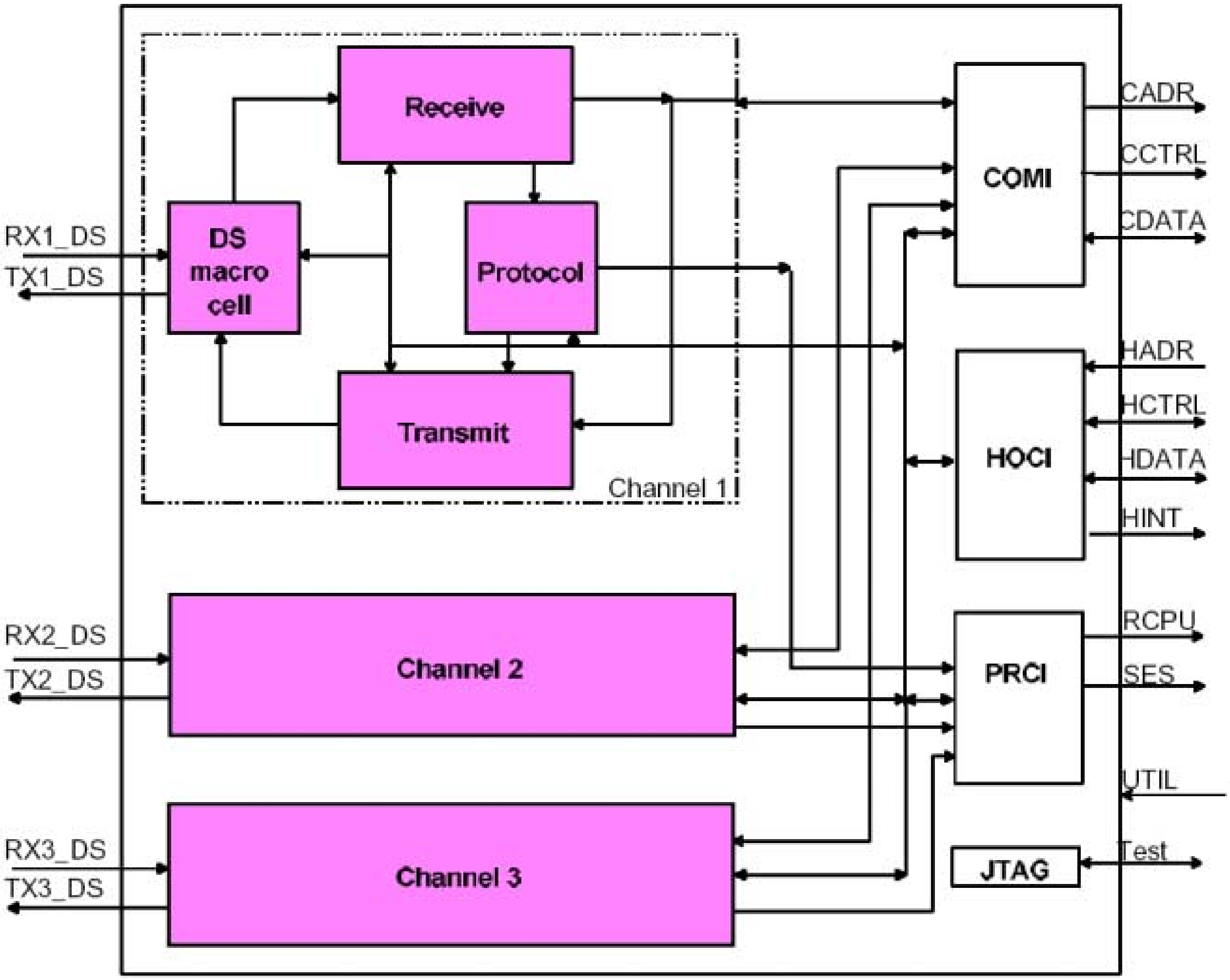
- bases on IEEE-1355 protocol
- 3 IEEE-1355 links with up to 200 Mbit/s data transmit rate
- each parallel interface can be configured to 8, 16 or 32 bits
- checksum generation/check at packet level

SMCS116/T7906E (SMCSlite)

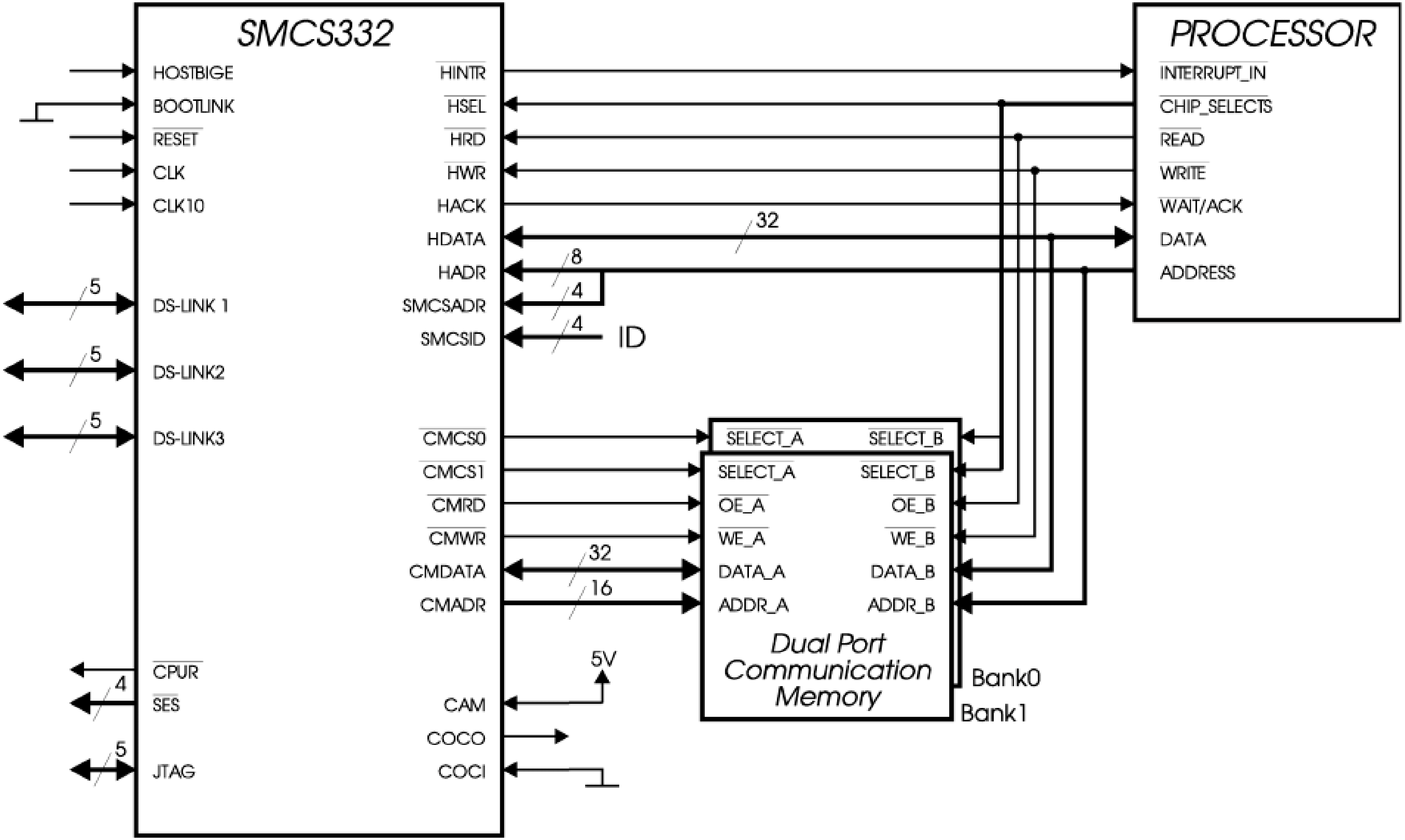
- bases on IEEE-1355 protocol
- 1 IEEE-1355 link with up to 200 Mbit/s data transmit rate
- parallel interface can be configured to 8 or 16 bits
- checksum generation/check at packet level

Introduction SMCS332

- 3 bi-directional link channels
- each with DS macro cell, receive, transmit section, protocol processing unit
- COMI: Communication Memory Interface
  performs autonomous accesses to the communication memory
- HOCI: Host Control Interface
  gives r/w access to config reg and to DS channels for the CPU
- PRCI: Protocol Command Interface
  collects commands from protocol units
- JTAG: Test Interface



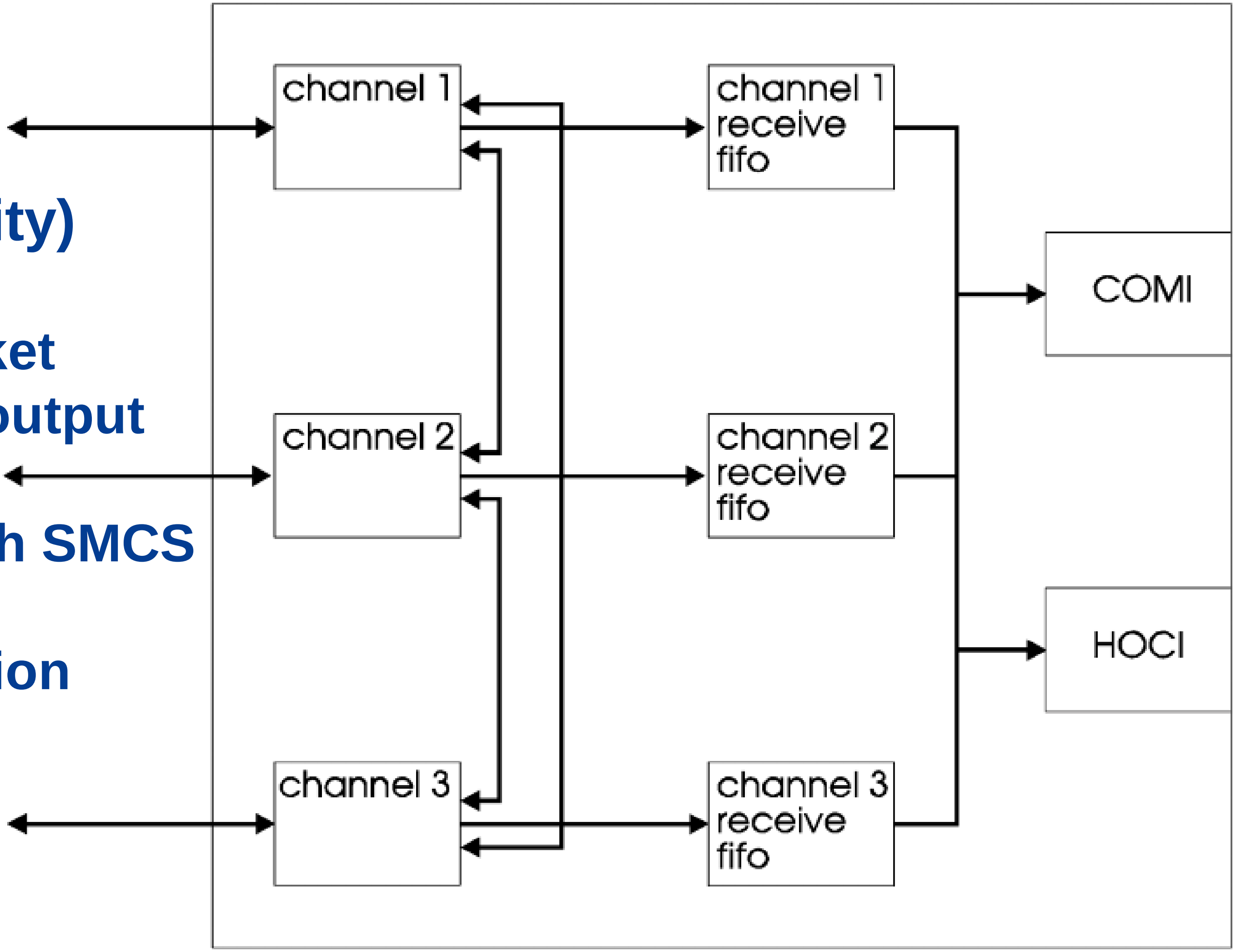
SMCS332 in typical module environment



Application of the SMCS332

Wormhole Routing (Router functionality)

- SMCS receives packet
- header determines output port
- packet flows through SMCS
- EOP marker terminates connection



Introduction SMCS116

Link Interface: Interface to serial IEEE-1355 link

Host Interface: Chip can be programmed & controlled by a local host

ADC/DAC I/F: allows the read (write) from an AD (DA) converter

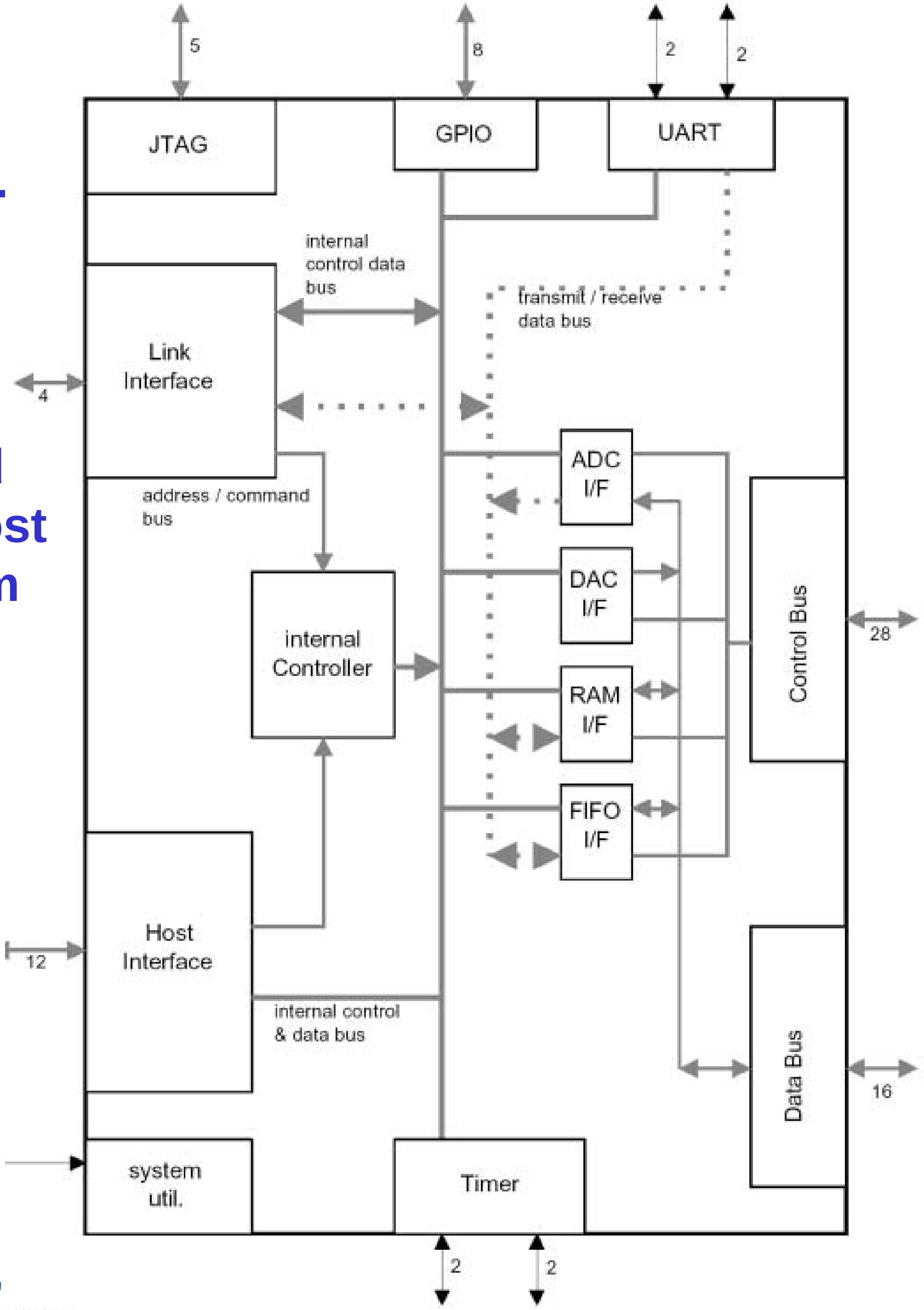
RAM IF: 4 different banks of memory are addressable

FIFO I/F: provides control signals (full, write, empty, read)

GPIO: General Purpose Interface

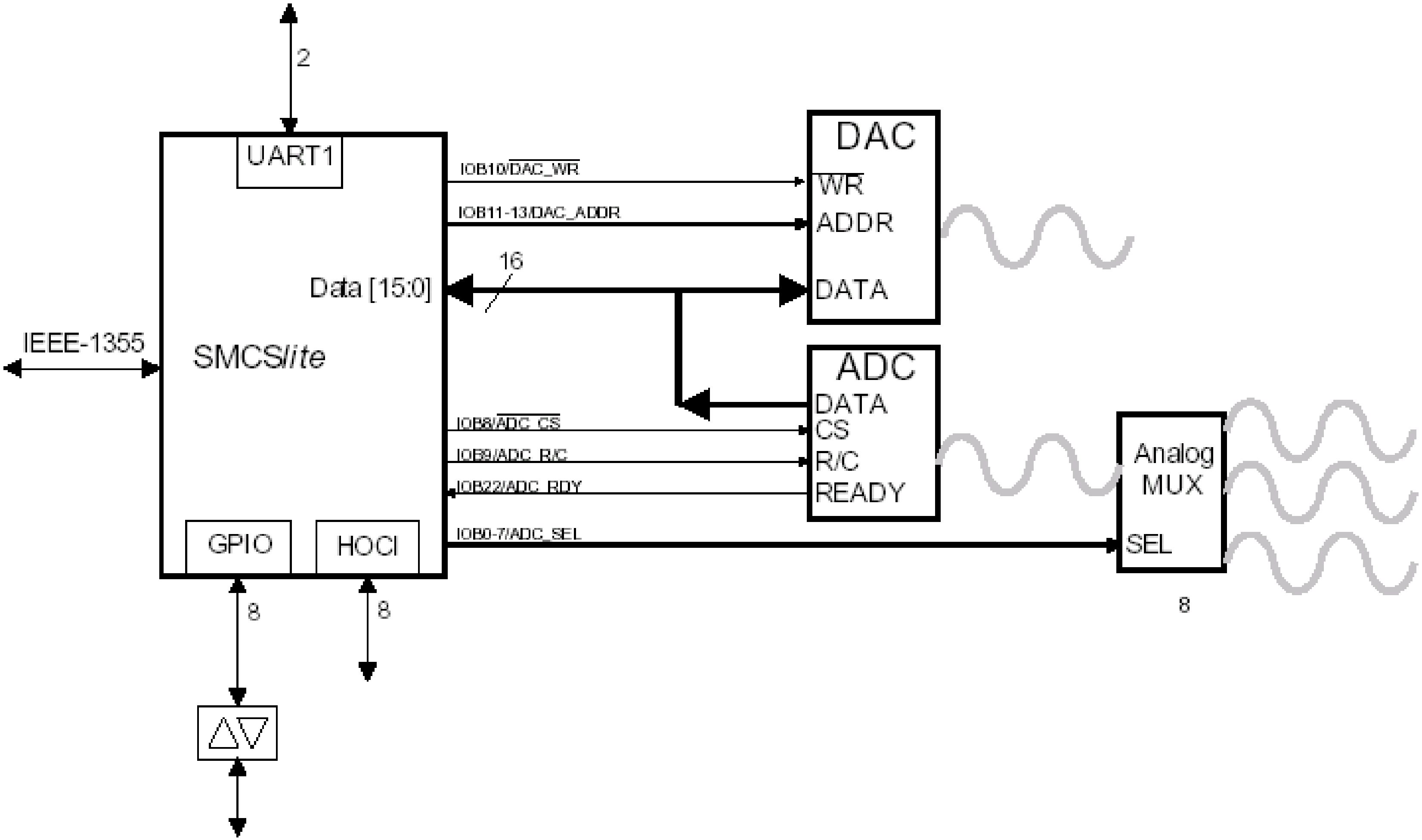
UART: 2 independent UARTs

JTAG: Test Interface



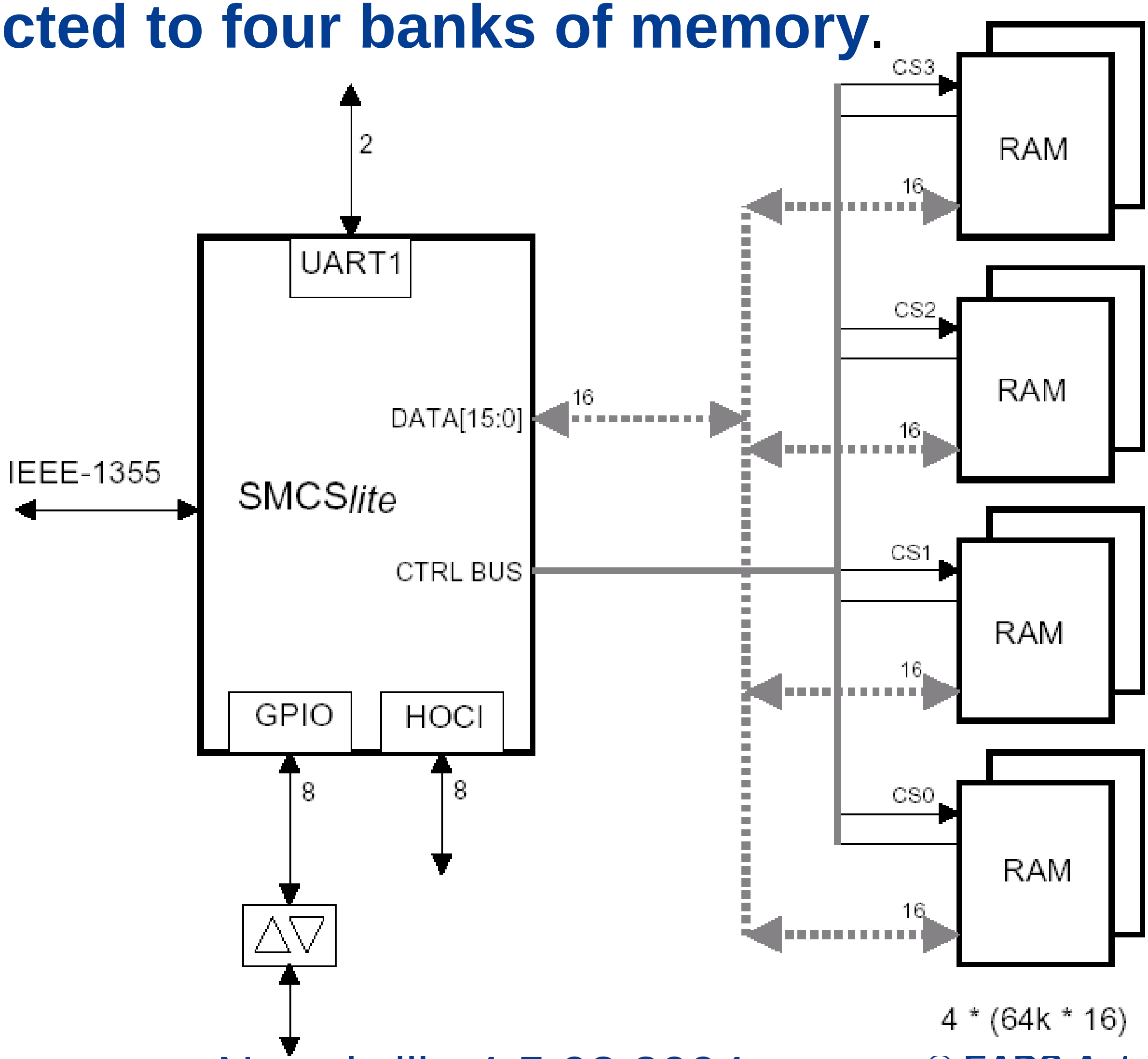
SMCSlite Applications

SMCSlite as communication and system controller on an interface node consisting of an ADC and DAC.



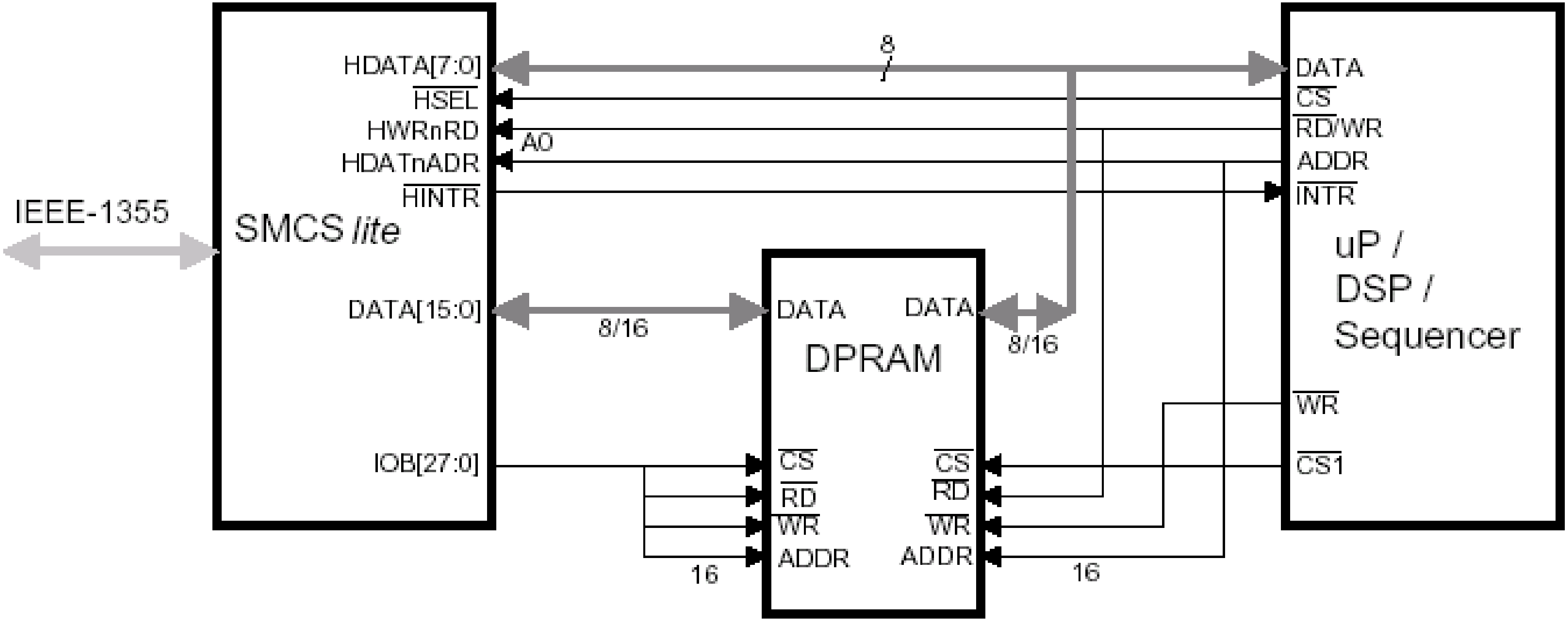
SMCSlite Applications 2

SMCSlite connected to four banks of memory.



SMCSlite Applications 3

Communication device for microprocessors



Motivation

Motivation for new SMCS ASICs

- SMCS ASICs are often used communication controllers
- SpaceWire standard is becoming increasingly important

Requirements for the new SMCS SpW

- SpaceWire compliant
- Pin compatible to existing SMCS332 / SMCSlite
- radiation tolerant
- correct known anomalies of the existing SMCS332 / SMCSlite
- Goal: Backward compatibility concerning software

SMCS332SpW - New Features

New Features:

- **The new SpaceWire interface is resistant against simultaneous switching on the D, S inputs**
- **It is 'hot' plug able (no master-slave situation has to be arranged)**
- **The SpaceWire Interface transmits / receives the new time code characters**
  - Therefore 2 additional registers are used
- **The new SpaceWire Interface has no EOP2 token**
  - EOP is End Of Packet marker (former EOP1)
  - EEP is End of Error Packet marker (former EOP2)

Anomaly Correction:

- **All known anomalies (#B.1 – #B.5) will be corrected.**

SMCS332SpW - New Functions

New Functions :

- **Time code**
  - The SMCS332SpW can send Time Code characters
  - The SMCS332SpW can be used as Time Code master
- **New header field control bit**
  - more flexibility for packet generation
- **Two different checksum formats**
  - the checksum format of the existing SMCS332
  - a checksum format suggested for SpaceWire

SMCS332SpW - New Functions

- **Arbitrary packet length**

  SMCS332:

  - the difference between end address and start address gives the packet length
  - each packet is automatically completed with an EOP

  SMCS332SpW:

  - an additional bit prevents from the automatic EOP
  - this allows arbitrary packet lengths

  Attention: Finally the packet should be completed with an EOP!

- **No EOP2**
  - EOP1 is now EOP (for user usage)
  - EOP2 is now EEP (reserved for Error Conditions)

SMCS332SpW - New Functions

Removal of packet size restrictions

- **Receive data over HOCI FIFO**
  - SMCS332: maximum 4 bytes packets (if host interface is operated in 16 or 32 width mode)
  - SMCS332SpW: no restriction for the packet size

- **Transmit data over COMI**

  SMCS332:
  - COMI in 8 bit modes: only packets of size n*4+4 (or n*4+3) bytes should be sent
  - COMI in 16 bit modes: only packets of size n*4+4 bytes should be sent.

  SMCS332SpW: no restrictions for the packet size

SMCSlite-SpW - New Features

New Features:

- **The new SpaceWire interface is resistant against simultaneous switching on the D, S inputs**

- **It is 'hot' plug able**

- **The SpaceWire Interface transmits / receives the new time code characters**
  - Therefore 2 additional registers are used

- **The new SpaceWire Interface has no EOP2 token**
  - EOP is End Of Packet marker (former EOP1)
  - EEP is End of Error Packet marker (former EOP2)

Anomaly Correction:

- **The known anomaly (#A.1) will be corrected.**

SMCSlite-SpW - New Functions

New Functions :

- **Protocol**
  - the protocol engine will be modified that it tolerates and executes commands of any length
  - rest of a packet (read beyond 1 byte; write beyond 2 bytes) will be ignored
- **Two different checksum formats**
  - the checksum format of the existing SMCS116
  - a checksum format suggested for SpaceWire
- **Time code**
  - The SMCS116SpW can send Time Code characters
  - The SMCS116SpW can be used as Time Code master

SMCSlite-SpW - New Functions

- **FIFO**
  - support of 16 bit data bus in active and passive mode
- **UART**
  - implementation of an additional interrupt which is set if the transmit FIFO is empty
- **ADC**
  - the timing/ sequence during the use of an external analogue multiplexer will be modified
  - EOP2 can not selected to terminate a packet, EOP has to be used

Project-Team

The SMCS332SpW / SMCS116SpW will be developed and tested by EADS Astrium GmbH.

The ASICs will be manufactured by Atmel who also provide the customer support for the chip.

Additional support for applications (boards, drivers, test equipment) will be provided by University of Dundee through STAR-Dundee.

Schedule (planned)

Planned Schedule:

Project KO:	**April 2004**
Prototype manufactured:	**Q4 2004**
ASIC available:	**Q1 2005 (TBC)**