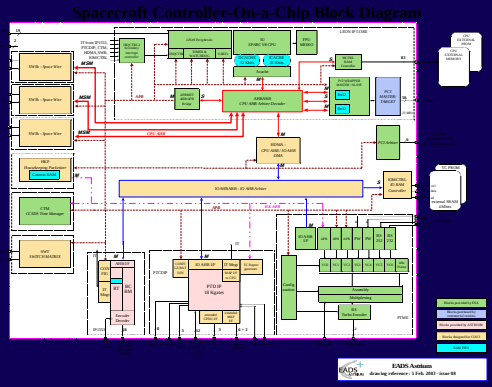
Building Blocks For System on a Chip
Spacecraft Controller on a Chip

ESTEC contract 13345 – COO3



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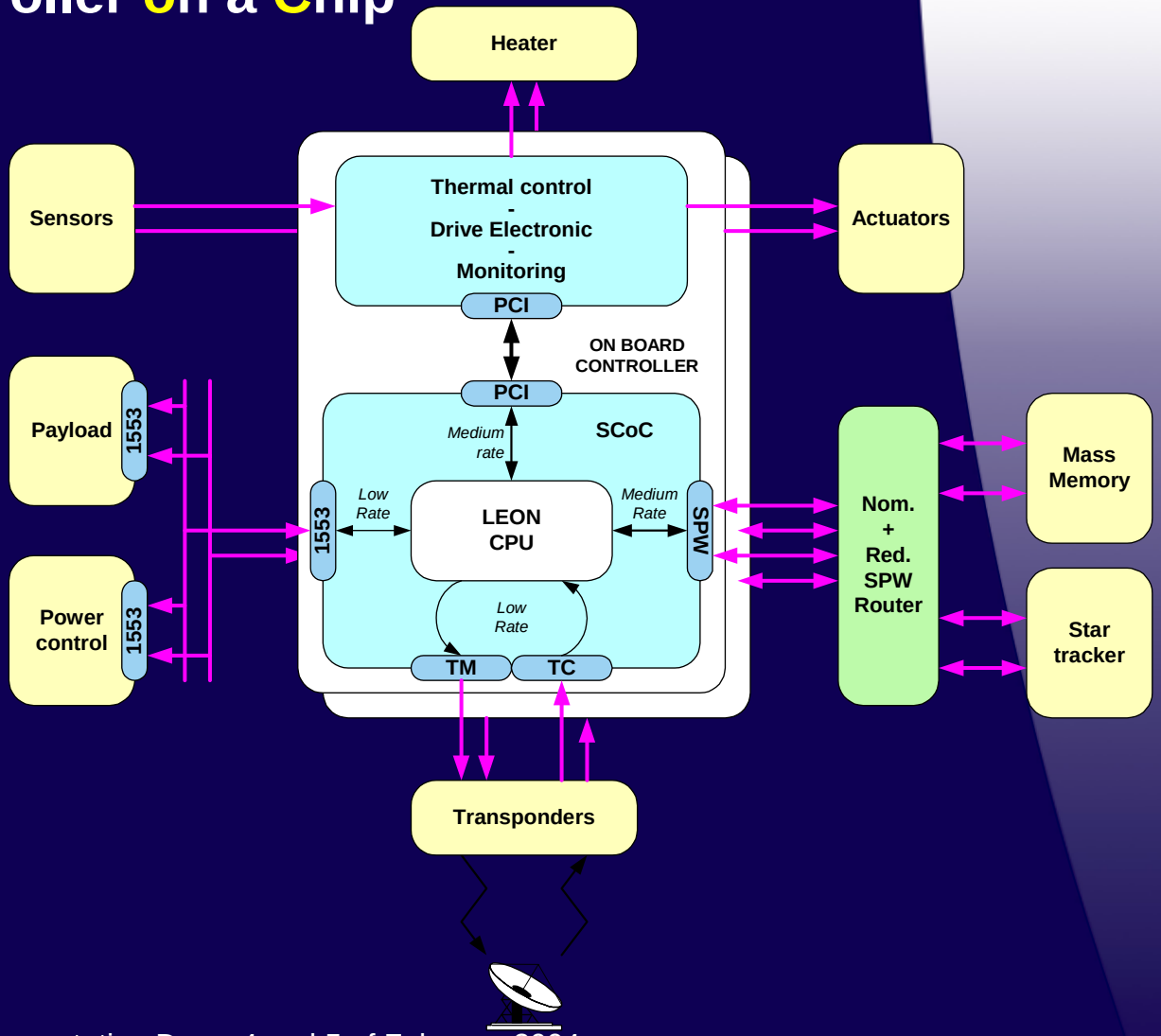
Contract and study presentation

- COO3 is phase 3 of ESA 13345 contract called “Building Blocks for System on a Chip”.
- Development of a modular architecture
  - Based on a standard bus : AMBA™ AHB and APB
  - Based on standard services : interrupt, synchronization
- Development of re-usable IP cores
- Use of existing IP cores from different sources :
  - Company internal IP cores
  - ESA provided IP cores
  - Re-use of previous VHDL ASIC developments

Development Plan

- Classical development approach of an ASIC
  - Architectural design with full VHDL RTL simulation
    - IP core interconnection study
    - Adaptation of the previous ASIC design
    - Global simulation of the SoC
  - Detailed design performed targeting a XILINX FPGA
- But with specific methodology for SoC design
  - Modular approach of the SoC : progressive integration of the IP cores
  - Validation of the IP core at block level
  - Validation of the interconnection scheme at upper level

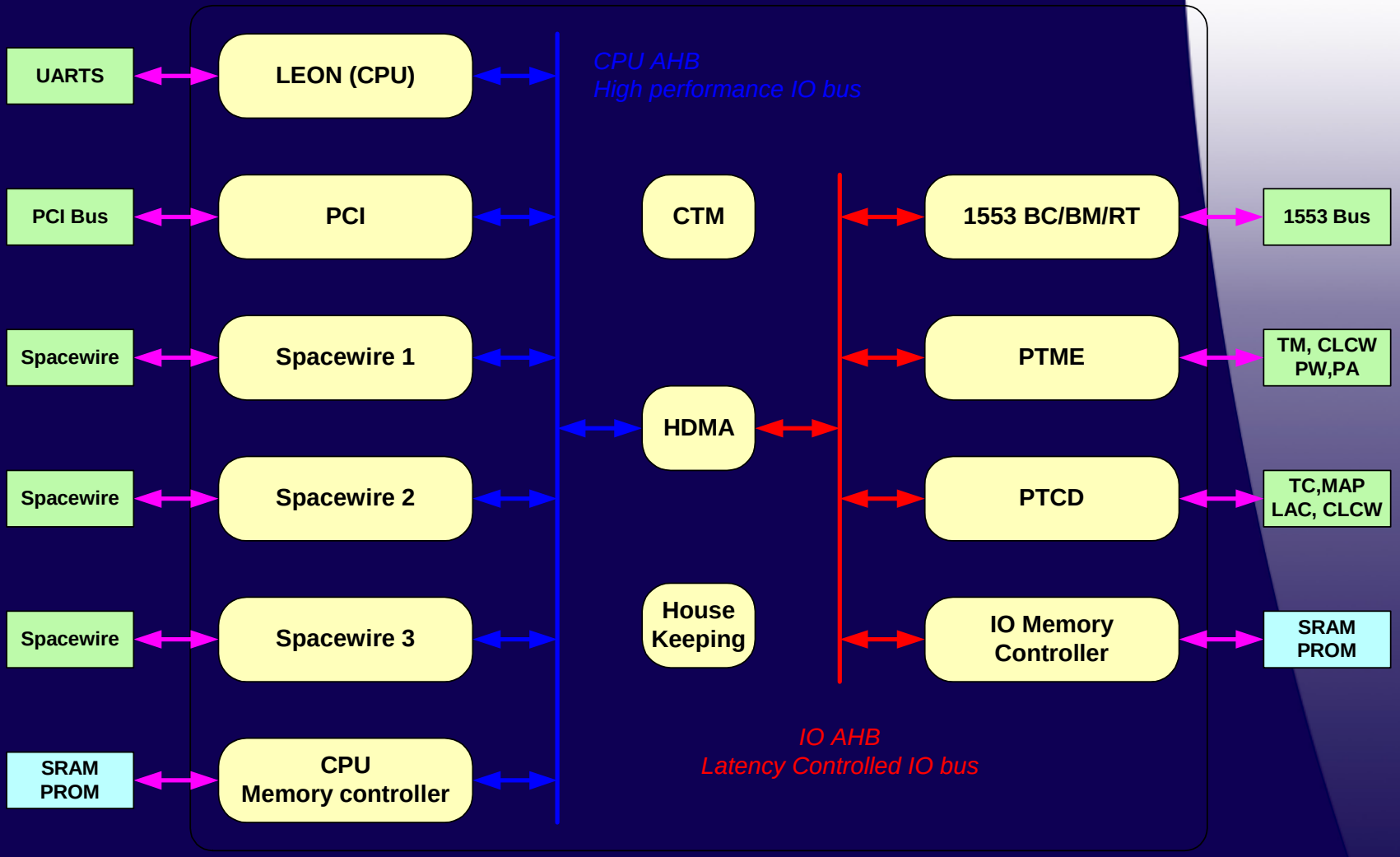
Environment of the SCoC
Spacecraft Controller on a Chip



IP cores integrated into the SCoC

- Includes the main digital functions able to perform the Data Handling of a Spacecraft :
  - The processor based on LEON with its FPU
  - A parallel bus at board level : PCI
  - A fast serial link : SpaceWire Link
  - A CCSDS Time Management function
  - A serial bus for control of remote equipments : 1553
  - A Telecommand function based on PTCD design
  - A Telemetry function based on PTME IP
  - Automatic housekeeping generation

SCoC Simplified Architecture



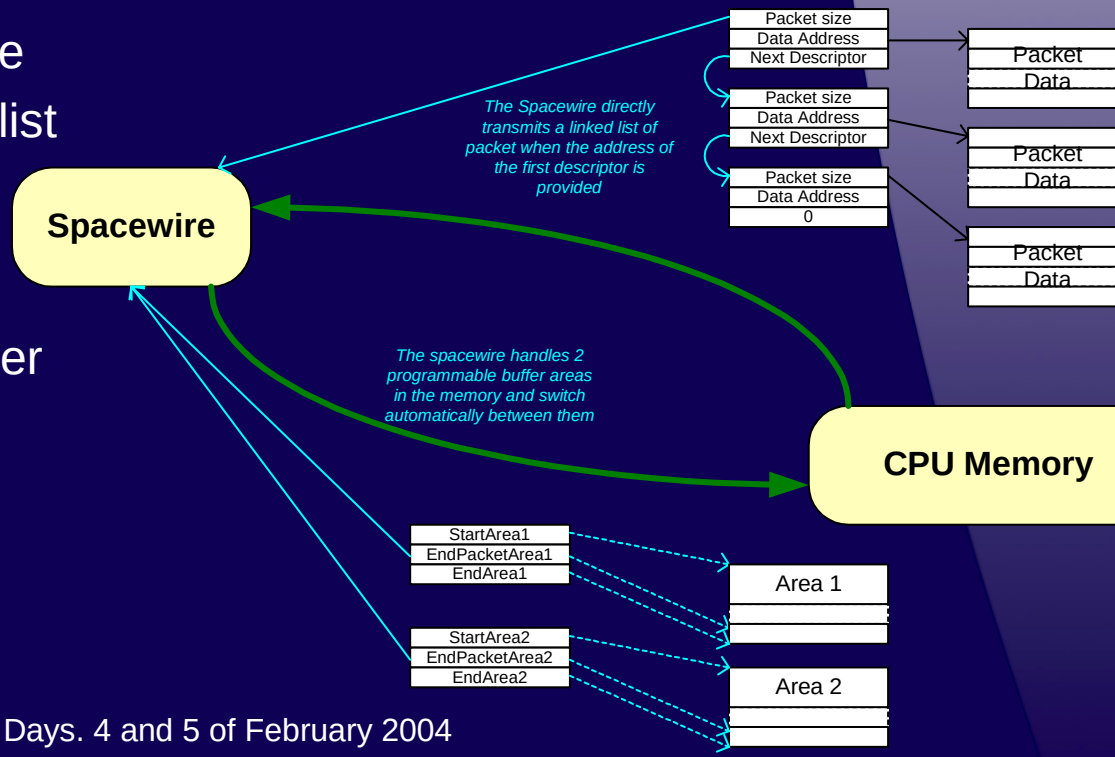
Distributed DMA control

- DMA controller are integrated at IP core level in order to have Core specific capabilities

  –Into the PCI interface : burst access, prefetch …

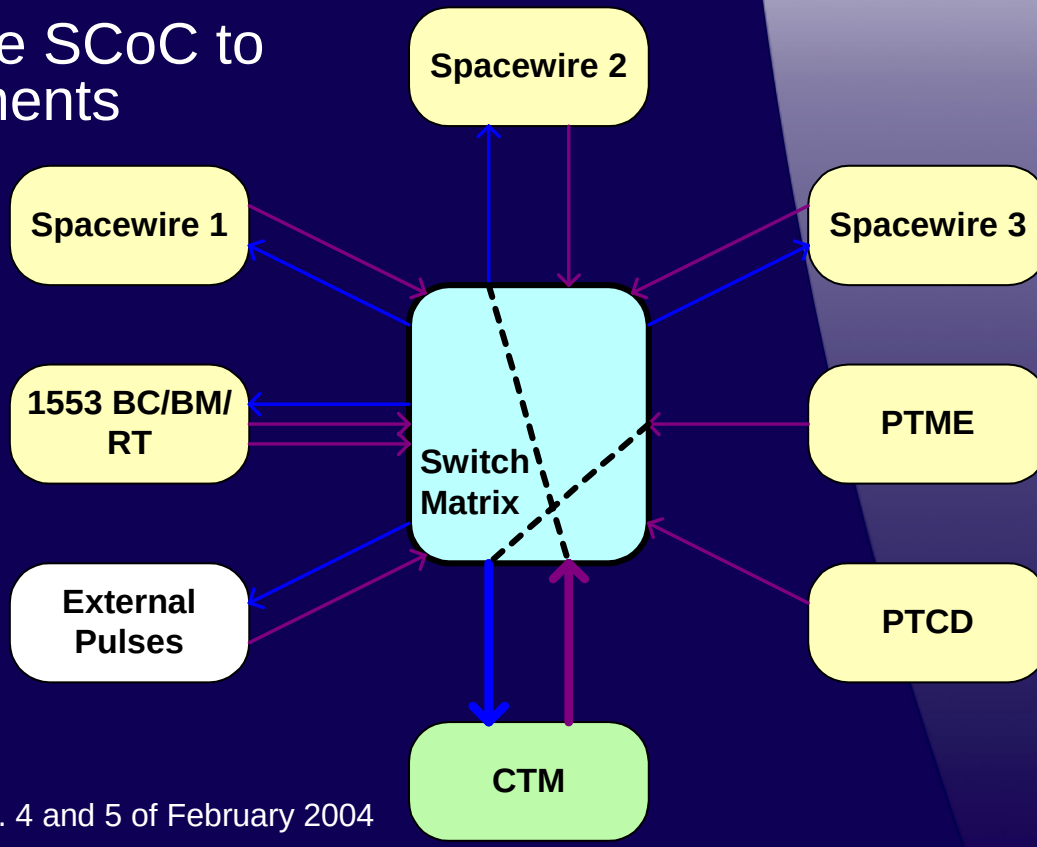
  –Into the Spacewire : double buffer management, linked list of packets

  –Into the Mil-Std-1553 : programmable Bus Controller …



IP Core synchronisation

- Most of IP core can receive or distribute synchronisation signals : spacewire, PTME, 1553, CTM …
- Modular time distribution implemented to adapt the SCoC to specific system requirements



Performance of the system

- The SCoC presents limitation
- Bottleneck identified at CPU SRAM level and AHB bus
- Reduces maximum performances

COMPUTATION OF PERFORMANCES ON CPU AHB BUS

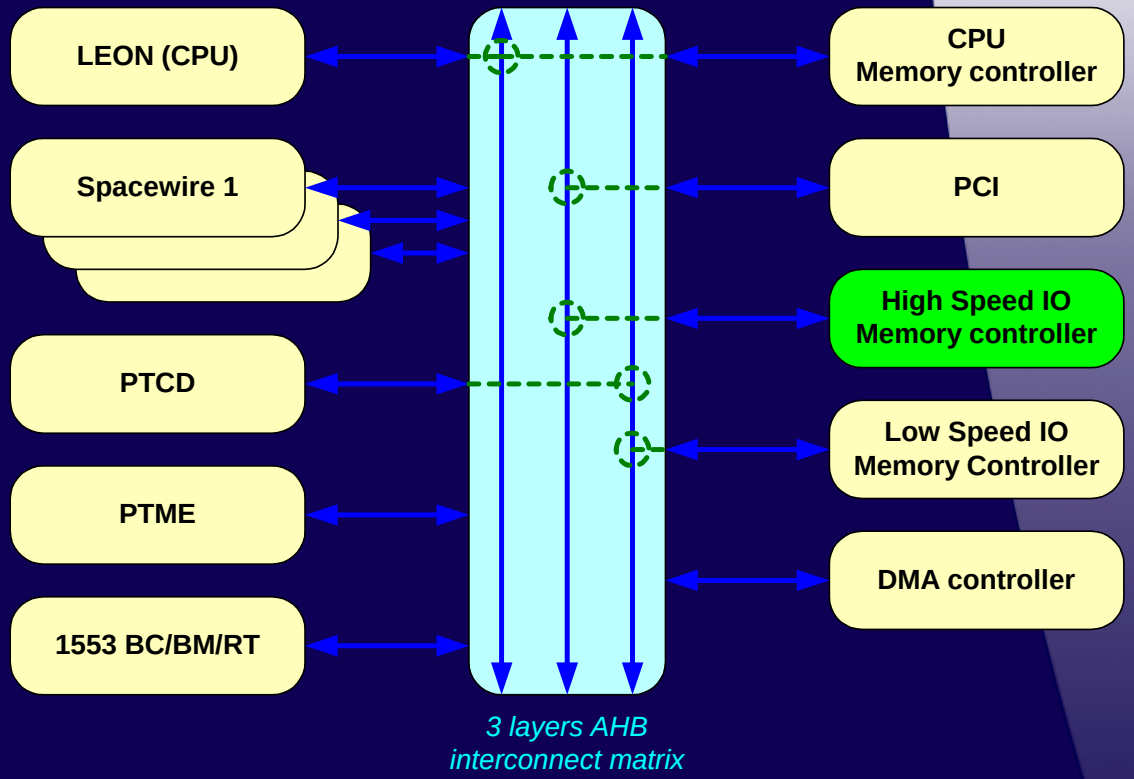
Global Hypothesis	
Maximum allowed bus load	80%
Bus Frequency	100 MHz

Slaves Hypotheses	
Memory controller	
RAM Read Wait states	0
RAM Write Wait States	0
MCTRL AHB WS on first read access	3
MCTRL AHB WS on next read access	2
MCTRL AHB WS on first write access	3
MCTRL AHB WS on next write access	2

Masters Hypotheses	
Processor	
CPU usage ratio	**65,5%**
Instruction cache hit ratio	80%
Data cache hit ratio	80%
Load instruction ratio	10%
Store instruction ratio	5%
Instruction cache fill burst length	4
Spacewire	
overall Spacewire TX bit rate	100 Mbits/s
overall Spacewire RX bit rate	100 Mbits/s
PCI	
PCI write rate	0,5 Mwords/s
PCI read rate	0,5 Mwords/s

Possible Performance Enhancement

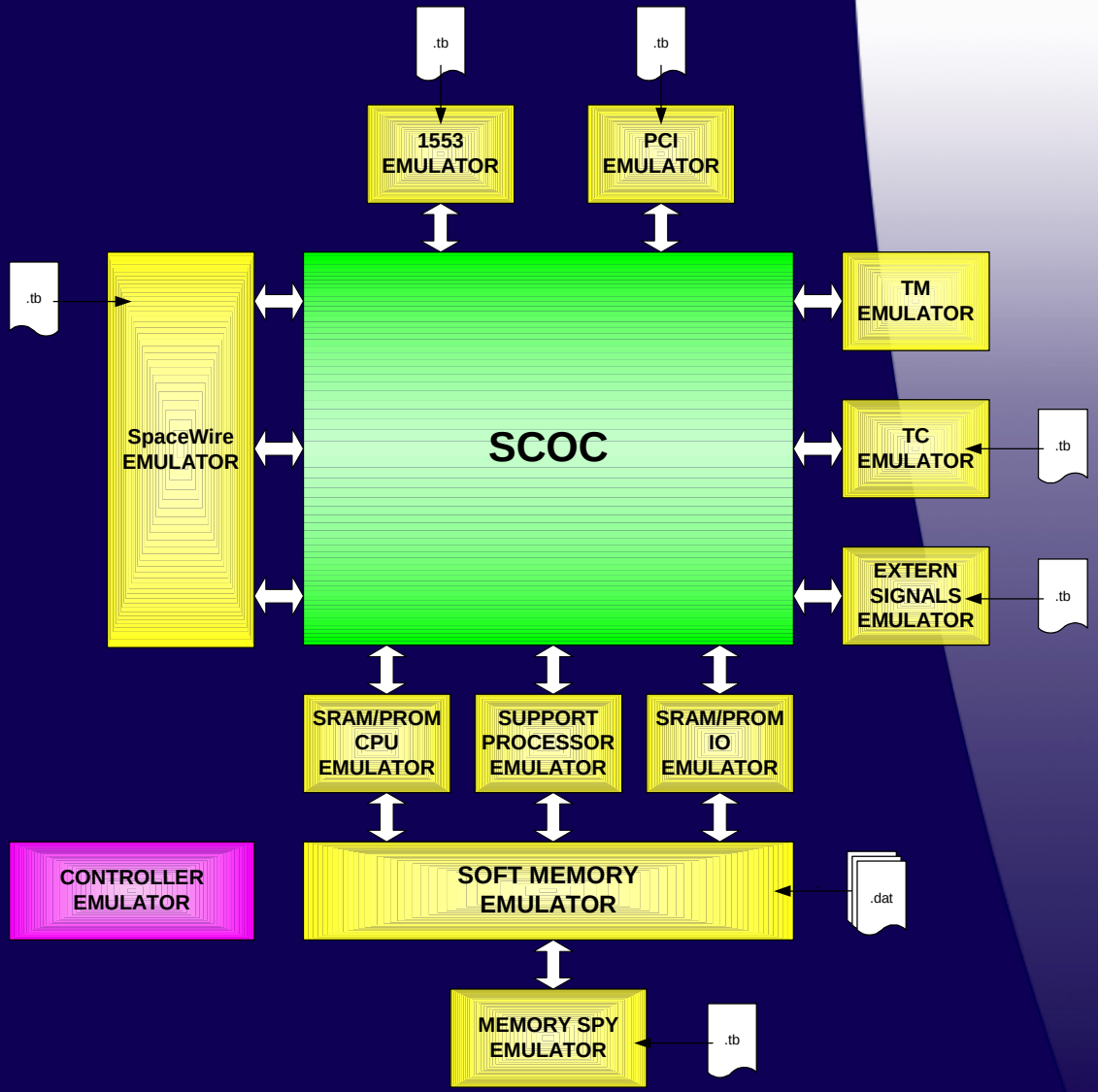
- Use of Multi-layer AHB and a second external RAM interface



Increases the number of external I/O (which is already high)

Modularity in simulation environment

- Each IP core is associated to an emulator handling the protocol and verification of the external I/Os



Detailed design targeting XILINX XCV2000-E

- Full SCoC design does not fit into the selected FPGA
- Modular approach of SCoC allowed targeting reduced SCoC definitions
  - Configuration 1 : PCI, 1553 and Spacewires
  - Configuration 2 : with PCI, TM/TC and housekeeping

Configuration	Max Frequency	Resource usage
PCI, 1553, SPW	23.7 MHz (WC path in IU of LEON1)	97 % of slices
PCI, TMTC	20.8 MHz (WC path in PTME)	96 % of slices

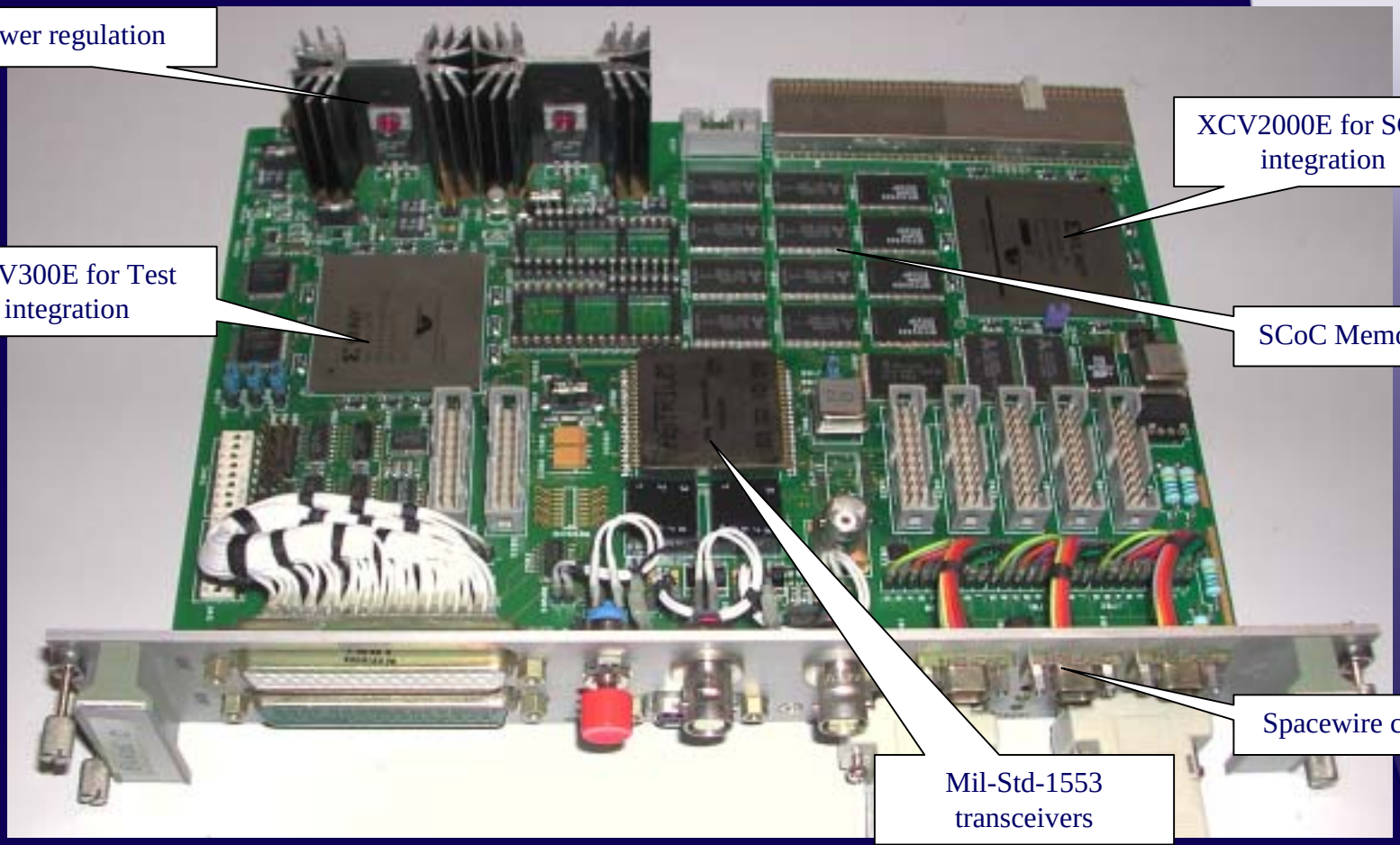
Prototyping of the SCoC – BLADE Board

- Board developed for the evaluation of the SCoC
- Design implemented in XILINX VIRTEX-E FPGA
- CompacPCI 6U standard board

- Specific interfaces implemented on the board
  - 1553 transceiver
  - Spacewire interfaces
  - TM/TC interfaces (RS232, RS422)

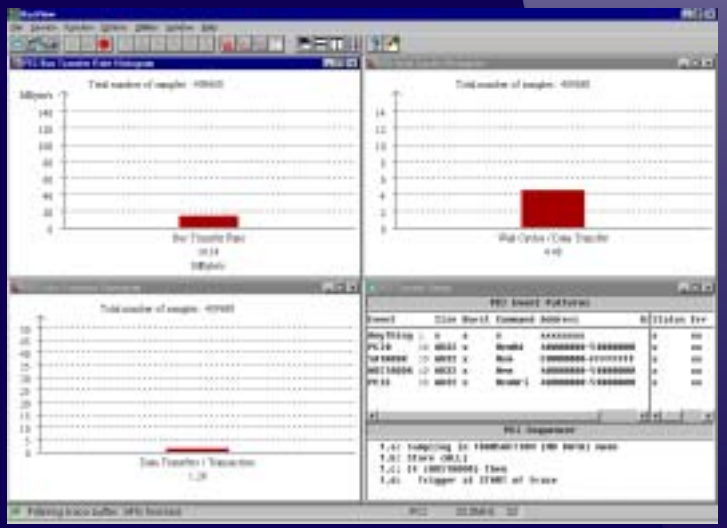
- Embedded FPGA to conduct test without need of specific external hardware (EGSE)

BLADE board description



Test results

- All functionalities of the SCoC are activated
- Test of performances for PCI and Spacewire interfaces :
  - Spacewire :High efficient DMA controller allow high speed transfer with little CPU usage
  - PCI : The system clock limits the performances reached on the PCI bus



COO3 Study results

- This study permit to :
  - Evaluate the methodology of the design of a large ASIC based on the use of IP core
    - Verification at SoC level versus verification at IP level
    - Management of the configuration of the SCoC with IP cores coming from different sources
    - Development of modular designs
  - Develop the library of available IP cores for use in space applications
    - PTCD, PTME, 1553, CTM, AMBA bus related IP …

Conclusion

- BLADE Board used for A3M R&T :
  - VxWorks on LEON
  - Use of Spacewire for data exchange
  - Use of CTM for time synchronisation
- This activity is a good starting point
  - AMBA can be used as standard for internal busses
  - Methodology of IP integration for complex ASIC developments
- Astrium gained experience in the development of complex integrated system